19-5616; Rev 11/10

DALLAS SEMICONDUCTOR MAXIM

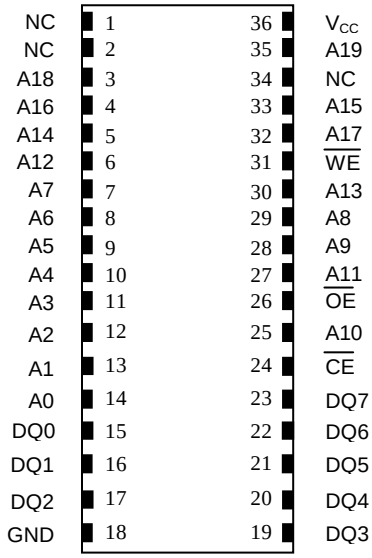
# DS1265Y/AB
# 8M Nonvolatile SRAM

www.maxim-ic.com

## FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Unlimited write cycles
- Low-power CMOS operation
- Read and write access times of 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% $V_{CC}$ operating range (DS1265Y)
- Optional ±5% $V_{CC}$ operating range (DS1265AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND

## PIN ASSIGNMENT




36-Pin ENCAPSULATED PACKAGE
740-mil EXTENDED

## PIN DESCRIPTION

| | |
|---|---|
| A0 - A19 | - Address Inputs |
| DQ0 - DQ7 | - Data In/Data Out |
| $\overline{CE}$ | - Chip Enable |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| $V_{CC}$ | - Power (+5V) |
| GND | - Ground |
| NC | - No Connect |

## DESCRIPTION

The DS1265 8M Nonvolatile SRAMs are 8,388,608-bit, fully static nonvolatile SRAMs organized as 1,048,576 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing.

## READ MODE

The DS1265 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 20 address inputs ($A_0$ - $A_{19}$) defines which of the 1,048,576 bytes of data is accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later-occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than $t_{ACC}$.

## WRITE MODE

The DS1265 devices execute a write cycle whenever $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

## DATA RETENTION MODE

The DS1265AB provides full functional capability for $V_{CC}$ greater than 4.75 volts and write protects by 4.5 volts. The DS1265Y provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The nonvolatile static RAMs constantly monitor $V_{CC}$. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become don't care, and all outputs become high-impedance. As $V_{CC}$ falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.75 volts for the DS1265AB and 4.5 volts for the DS1265Y.

## FRESHNESS SEAL

Each DS1265 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is first applied at a level greater than $V_{TP}$, the lithium energy source is enabled for battery backup operation.

## ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground -0.3V to +6.0V
Operating Temperature Range
Commercial: 0°C to +70°C
Industrial: -40°C to +85°C
Storage Temperature -40°C to +85°C
Lead Temperature (soldering, 10s) +260°C
**Note:** EDIP is wave or hand soldered only.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

## RECOMMENDED DC OPERATING CONDITIONS ($T_A$: See Note 10)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| DS1265AB Power Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V | |
| DS1265Y Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| Logic 1 Input Voltage | $V_{IH}$ | 2.2 | | $V_{CC}$ | V | |
| Logic 0 Input Voltage | $V_{IL}$ | 0 | | +0.8 | V | |

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$=5V ±5% for DS1265AB)
($T_A$: See Note 10) ($V_{CC}$=5V ±10% for DS1265Y)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | -2.0 | | +2.0 | µA | |
| I/O Leakage Current | $I_{IO}$ | -2.0 | | +2.0 | µA | |
| Output Current @ 2.4V | $I_{OH}$ | -1.0 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}$ =2.2V | $I_{CCS1}$ | | 1.0 | 1.5 | mA | |
| Standby Current $\overline{CE}$ =$V_{CC}$-0.5V | $I_{CCS2}$ | | 100 | 200 | µA | |
| Operating Current | $I_{CCO1}$ | | | 85 | mA | |
| Write Protection Voltage (DS1265AB) | $V_{TP}$ | 4.50 | 4.62 | 4.75 | V | |
| Write Protection Voltage (DS1265Y) | $V_{TP}$ | 4.25 | 4.37 | 4.5 | V | |

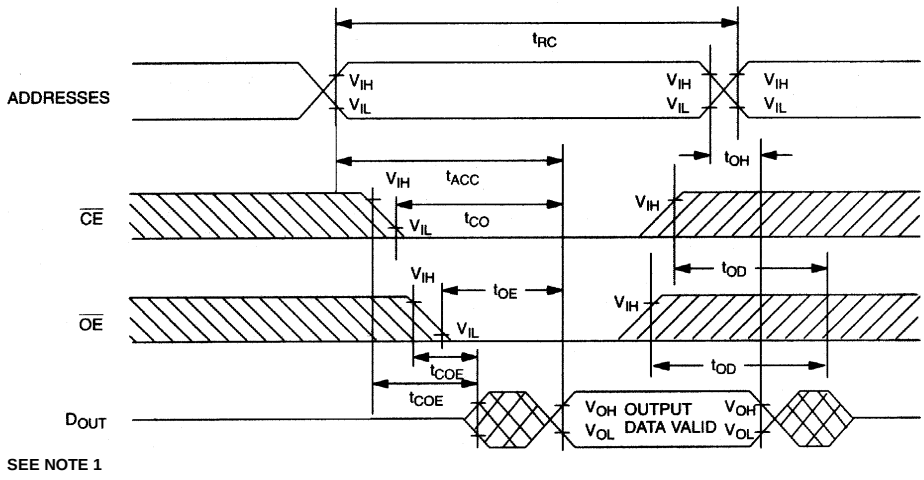
## CAPACITANCE ($T_A$ = +25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | 10 | 20 | pF | |
| Output Capacitance | $C_{I/O}$ | | 10 | 20 | pF | |

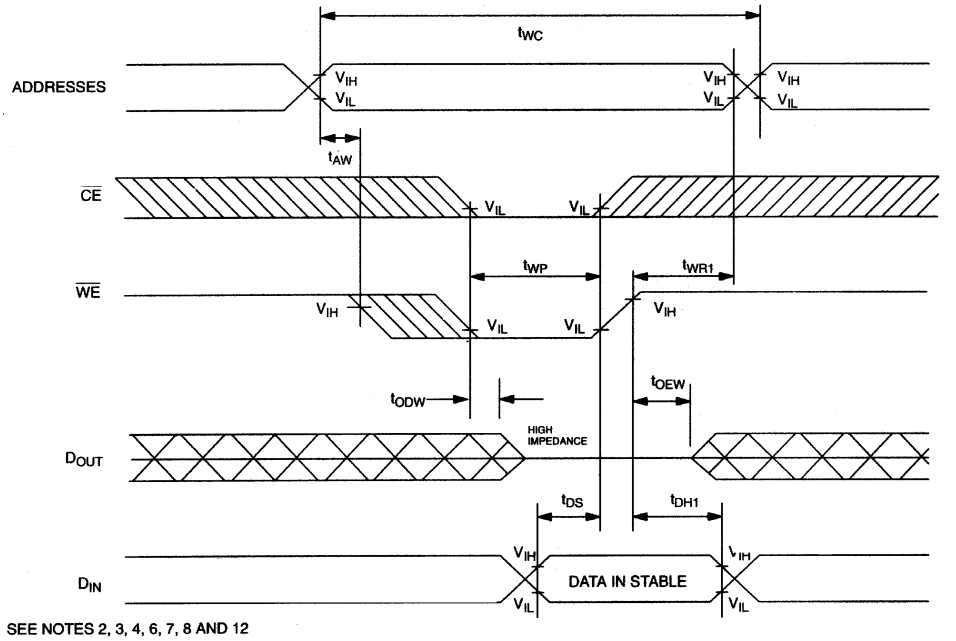
## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$=5V ±5% for DS1265AB)
($T_A$: See Note 10) ($V_{CC}$=5V ±10% for DS1265Y)

| PARAMETER | SYMBOL | DS1265AB-70 DS1265Y-70 | | UNITS | NOTES |
|---|---|---|---|---|---|
| | | MIN | MAX | | |
| Read Cycle Time | $t_{RC}$ | 70 | | ns | |
| Access Time | $t_{ACC}$ | | 70 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 35 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 70 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | ns | 5 |
| Output High Z from Deselection | $t_{OD}$ | | 25 | ns | 5 |
| Output Hold from Address Change | $t_{OH}$ | 5 | | ns | |
| Write Cycle Time | $t_{WC}$ | 70 | | ns | |
| Write Pulse Width | $t_{WP}$ | 55 | | ns | 3 |
| Address Setup Time | $t_{AW}$ | 0 | | ns | |
| Write Recovery Time | $t_{WR1}$<br>$t_{WR2}$ | 5<br>15 | | ns<br>ns | 12<br>13 |
| Output High Z from $\overline{WE}$ | $t_{ODW}$ | | 25 | ns | 5 |
| Output Active from $\overline{WE}$ | $t_{OEW}$ | 5 | | ns | 5 |
| Data Setup Time | $t_{DS}$ | 30 | | ns | 4 |
| Data Hold Time | $t_{DH1}$<br>$t_{DH2}$ | 0<br>10 | | ns<br>ns | 12<br>13 |

## TIMING DIAGRAM: READ CYCLE

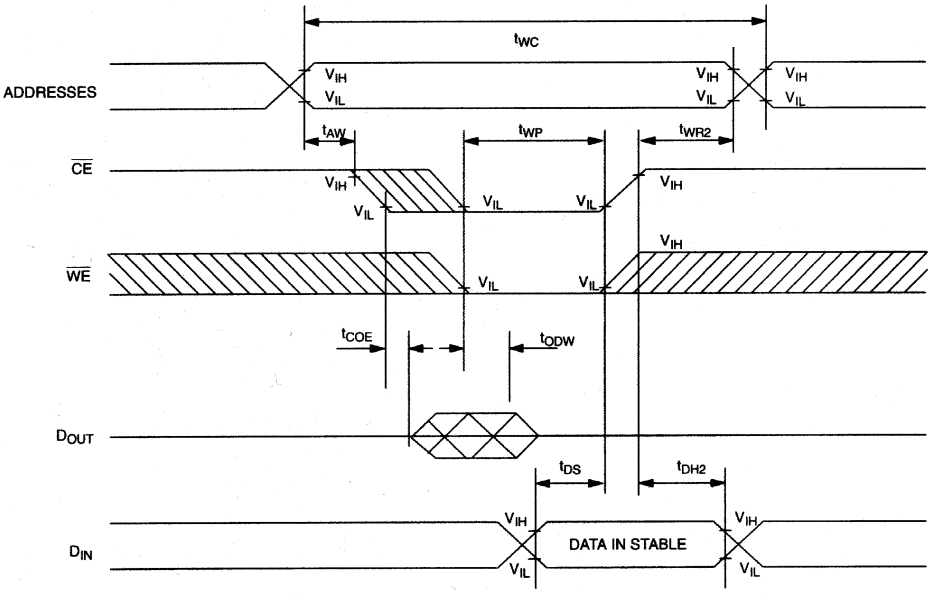


## TIMING DIAGRAM: WRITE CYCLE 1



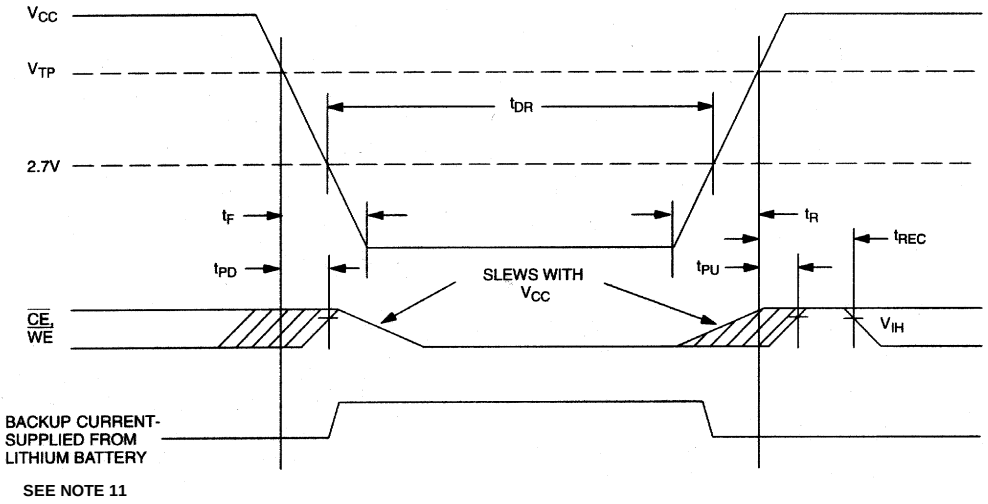

SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

## TIMING DIAGRAM: WRITE CYCLE 2




SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

## POWER-DOWN/POWER-UP CONDITION




## POWER-DOWN/POWER-UP TIMING

($T_A$: See Note 10)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{CC}$ Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive | $t_{PD}$ | | | 1.5 | µs | 11 |
| $V_{CC}$ slew from $V_{TP}$ to 0V | $t_F$ | 150 | | | µs | |
| $V_{CC}$ slew from 0V to $V_{TP}$ | $t_R$ | 150 | | | µs | |
| $V_{CC}$ Valid to $\overline{CE}$ and $\overline{WE}$ Inactive | $t_{PU}$ | | | 2 | ms | |
| $V_{CC}$ Valid to End of Write Protection | $t_{REC}$ | | | 125 | ms | |

($T_A$= +25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Expected Data Retention Time | $t_{DR}$ | 10 | | | years | 9 |

## WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

## NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = $V_{IH}$ or $V_{IL}$. If $\overline{OE}$ = $V_{IH}$ during write cycle, the output buffers remain in a high-impedance state.
3. $t_{WP}$ is specified as the logical AND of $\overline{CE}$ or $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DS}$ is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high-impedance state during this period.

8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
9. Each DS1265 has a built-in switch that disconnects the lithium source until the user first applies $V_{CC}$. The expected $t_{DR}$ is defined as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user. This parameter is assured by component selection, process control, and design. It is not measured directly during production testing.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power-down condition the voltage on any pin may not exceed the voltage on $V_{CC}$.
12. $t_{WR1}$ and $t_{DH1}$ are measured from $\overline{WE}$ going high.
13. $t_{WR2}$ and $t_{DH2}$ are measured from $\overline{CE}$ going high.
14. DS1265 modules are recognized by Underwriters Laboratories (UL) under file E99151.

## DC TEST CONDITIONS

Outputs Open
Cycle = 200ns for operating current
All voltages are referenced to ground

## AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0V to 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

## ORDERING INFORMATION

| PART | TEMP RANGE | SUPPLY TOLERANCE | PIN-PACKAGE | SPEED GRADE (ns) |
|---|---|---|---|---|
| DS1265AB-70+ | 0°C to +70°C | 5V ± 5% | 36 740 EDIP | 70 |
| DS1265AB-70IND+ | -40°C to +85°C | 5V ± 5% | 36 740 EDIP | 70 |
| DS1265Y-70+ | 0°C to +70°C | 5V ± 10% | 36 740 EDIP | 70 |
| DS1265Y-70IND+ | -40°C to +85°C | 5V ± 10% | 36 740 EDIP | 70 |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 36 EDIP | MDT36+1 | **21-0245** | — |

## REVISION HISTORY

| REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|
| 11/10 | Updated the storage information, soldering temperature, and lead temperature information in the *Absolute Maximum Ratings* section; removed the -100 MIN/MAX information from the *AC Electrical Characteristics* table; updated the *Ordering Information* table (removed -100 parts and leaded -70 parts); replaced the package outline drawing with the *Package Information* table | 1, 3, 4, 7 |