General purpose CMOS timer ICM7555

DESCRIPTION

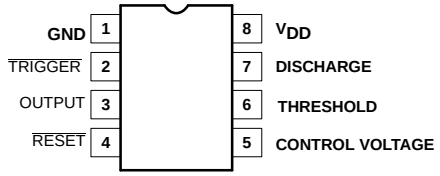
The ICM7555 is a CMOS timer providing significantly improved performance over the standard NE/SE555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$, and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

The ICM7555 is a stable controller capable of producing accurate time delays or frequencies.

In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the bipolar 555 device, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ inputs are active low. The output inverter can source or sink currents large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

PIN CONFIGURATION

D and N Packages



FEATURES

- Exact equivalent in most applications for NE/SE555
- Low supply current: 80µA (typ)
- Extremely low trigger, threshold, and reset currents: 20pA (typ)
- High-speed operation: 500kHz guaranteed
- Wide operating supply voltage range guaranteed 3 to 16V over full automotive temperatures
- Normal reset function; no crowbarring of supply during output transition
- Can be used with higher-impedance timing elements than the bipolar 555 for longer time constants
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Typical temperature stability of 0.005%/°C at 25°C
- Rail-to-rail outputs

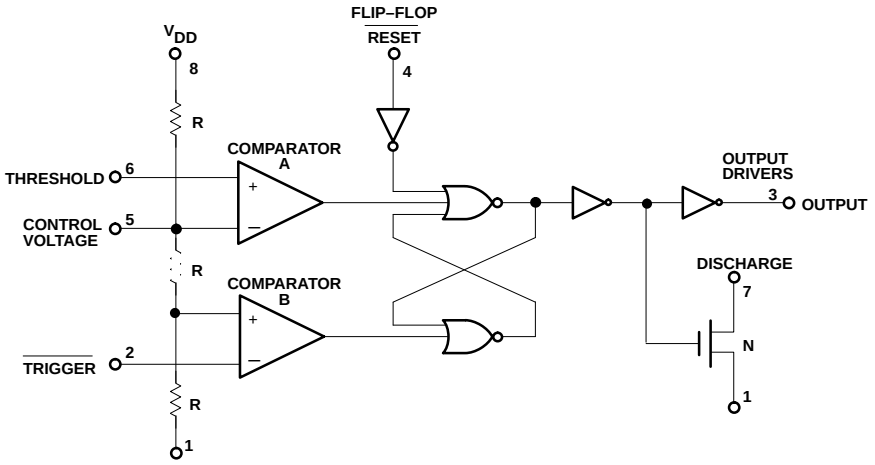
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	ICM7555CN	0404B
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	ICM7555CD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	ICM7555IN	0404B
8-Pin Plastic Small Outline (SO) Package	-40 to +85°C	ICM7555ID	0174C

EQUIVALENT BLOCK DIAGRAM



NOTE:
UNUSED INPUTS SHOULD BE CONNECTED TO APPROPRIATE VOLTAGE FROM TRUTH TABLE.

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$[1]	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V+)	> 1/3(V+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V+)	HIGH	HIGH	OFF

NOTES:
1. $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	+18	V
V_{TRIG}[1]	$\overline{\text{Trigger}}$ input voltage		
V_{CV}	Control voltage	> -0.3 to	
V_{TH}	Threshold input voltage	<V_{DD} + 0.3	V
V_{RST}	$\overline{\text{RESET}}$ input voltage		
I_{OUT}	Output current	100	mA
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still air)[2]		
	N package	1160	mW
	D package	780	mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (Soldering 60s)	300	°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} + 0.3V or less than GND -0.3V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555 must be turned on first.
2. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
3. See "Power Dissipation Considerations" section.

DC AND AC ELECTRICAL CHARACTERISTICS

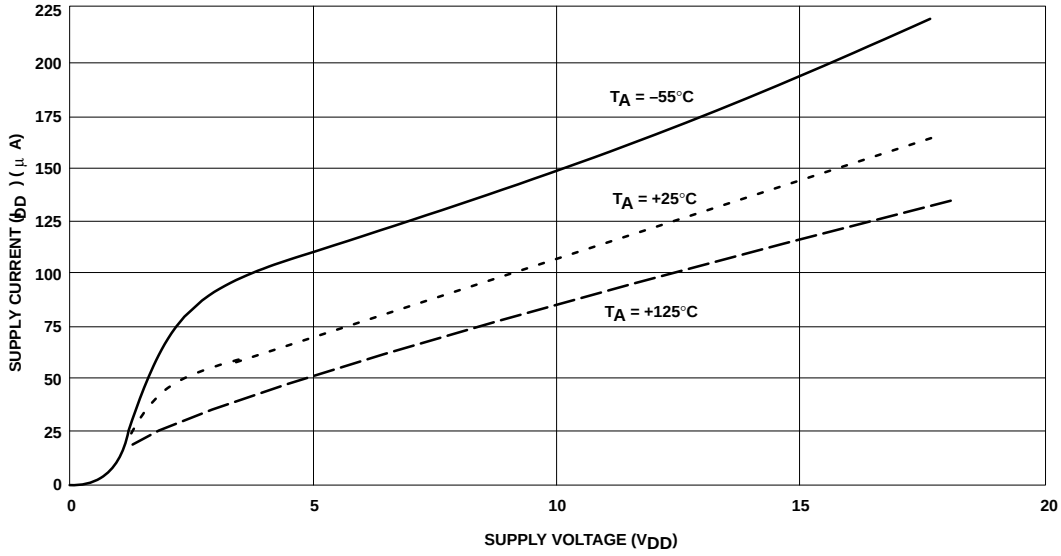
T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			ICM7555			
			MIN	TYP	MAX	
V_{DD}	Supply voltage	$T_{MIN} \le T_A \le T_{MAX}$	3		16	V
I_{DD}	Supply current[1]	$V_{DD} = V_{MIN}$ $V_{DD} = V_{MAX}$		50 180	200 300	µA µA
	Astable mode timing[2] Initial accuracy Drift with supply voltage Drift with temperature[3]	R_A, R_B = 1k to 100k, C = 0.1µF 5V <V_{DD} <15V V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 1.0 0.1 50 75 100	 5.0 3.0	 % %/V ppm/°C ppm/°C ppm/°C
V_{TH}	Threshold voltage	V_{DD} = 5V	0.63	0.65	0.67	xV_{DD}
V_{TRIG}	Trigger voltage	V_{DD} = 5V	0.29	0.31	0.34	xV_{DD}
I_{TRIG}	Trigger current	$V_{DD} = V_{TRIG} = V_{MAX}$ $V_{DD} = V_{TRIG}$ = 5V $V_{DD} = V_{TRIG} = V_{MIN}$		50 10 1		pA pA pA
I_{TH}	Threshold current	$V_{DD} = V_{TH} = V_{MAX}$ $V_{DD} = V_{TH}$ = 5V $V_{DD} = V_{TH} = V_{MIN}$		50 10 1		pA pA pA
I_{RST}	Reset current	$V_{DD} = V_{RST} = V_{MAX}$ $V_{DD} = V_{RST}$ = 5V $V_{DD} = V_{RST} = V_{MIN}$		100 20 2		pA pA pA
V_{RST}	Reset voltage	$V_{DD} = V_{MIN}$ and V_{MAX}	0.4	0.7	1.0	V
V_{CV}	Control voltage	V_{DD} = 5V	0.62	0.65	0.67	xV_{DD}
V_{OL}	Output voltage (low)	$V_{DD} = V_{MAX}$, I_{SINK} = 3.2mA V_{DD} = 5V, I_{SINK} = 3.2mA		0.1 0.2	0.4 0.4	V V
V_{OH}	Output voltage (high)	$V_{DD} = V_{MAX}$, I_{SOURCE} = -1.0mA V_{DD} = 5V, I_{SOURCE} = -1.0mA	15.25 4.0	15.7 4.5		V_{DD} V_{DD}
V_{DIS}	Discharge output voltage	V_{DD} = 5V, I_{DIS} = 10.0mA		0.2	0.4	V
t_R	Rise time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		45	75	ns
t_F	Fall time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		20	75	ns
F_{MAX}	Maximum oscillator frequency (astable mode)		500			kHz

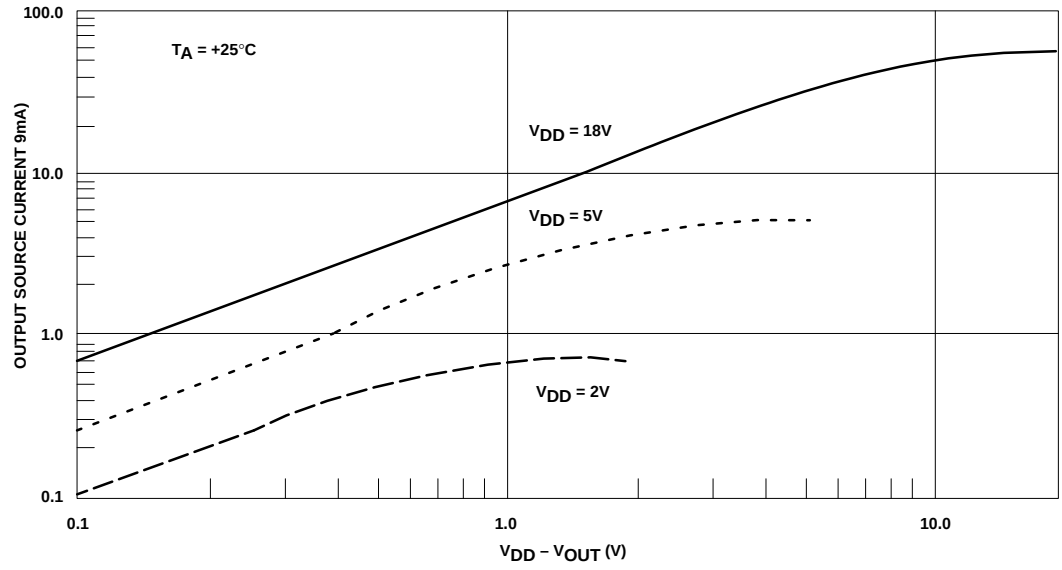
NOTES:

1. The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD, and $\overline{\text{RESET}}$ voltages.
2. Astable timing is calculated using the following equation: $f = \frac{1.38}{(R_A + 2R_B)C}$. The components are defined in Figure 2.
3. Parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

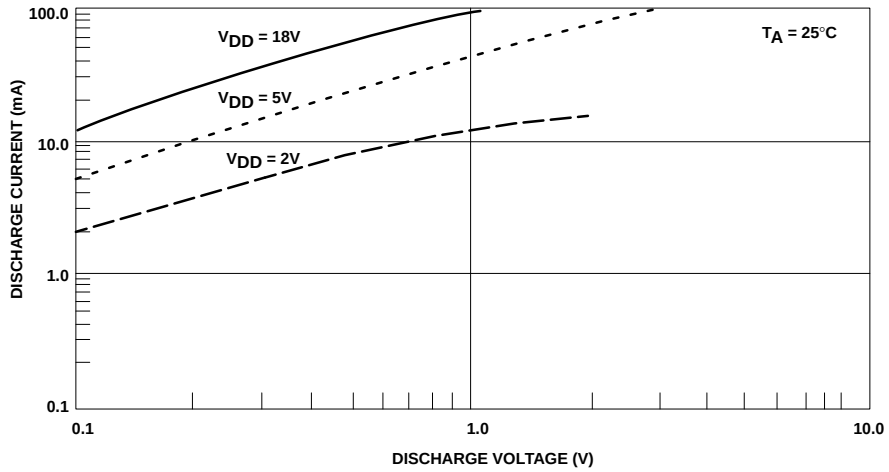


Supply Current vs Supply Voltage

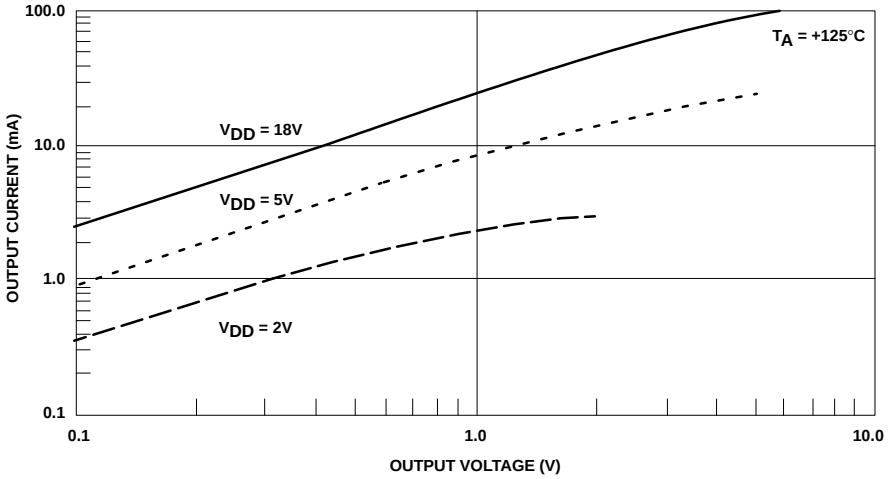


High Output Voltage Drop vs Output Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

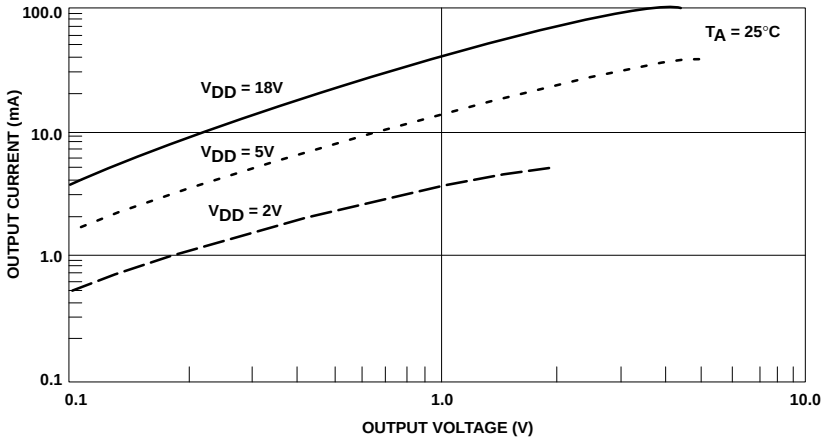


Discharge Low Output Voltage vs Discharge Sink Current

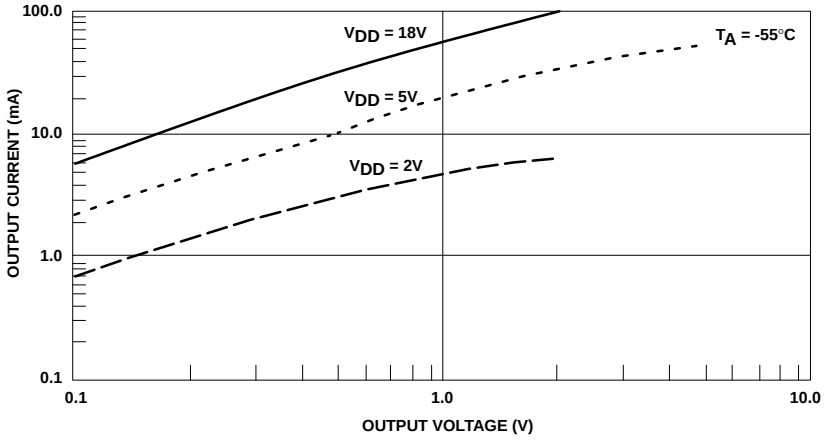


Low Output Voltage vs Output Sink Current

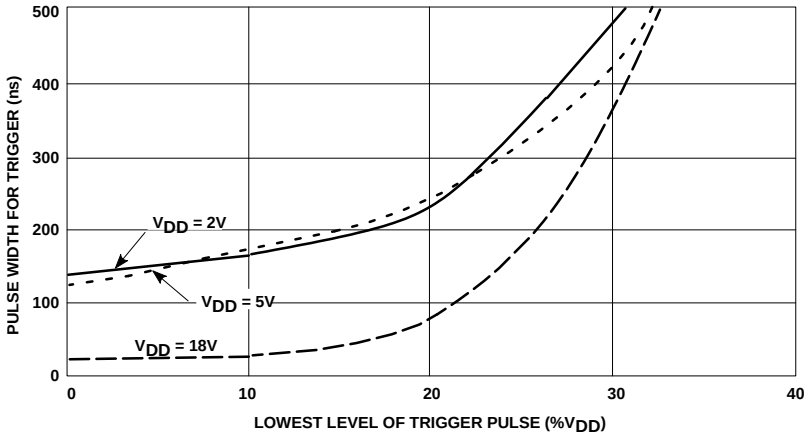
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Low Output Voltage vs Output Sink Current

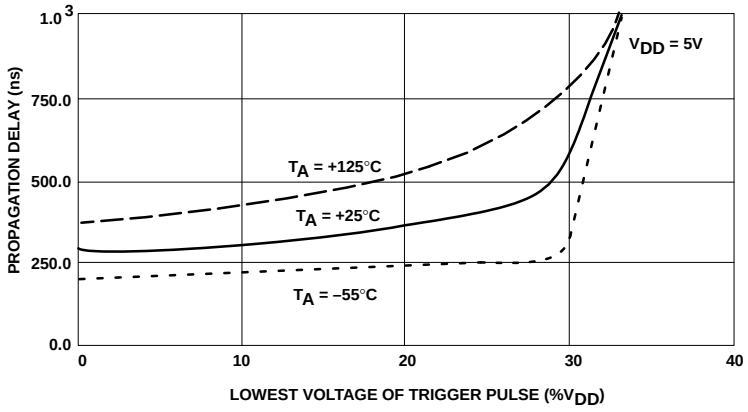


Low Output Voltage vs Output Sink Current

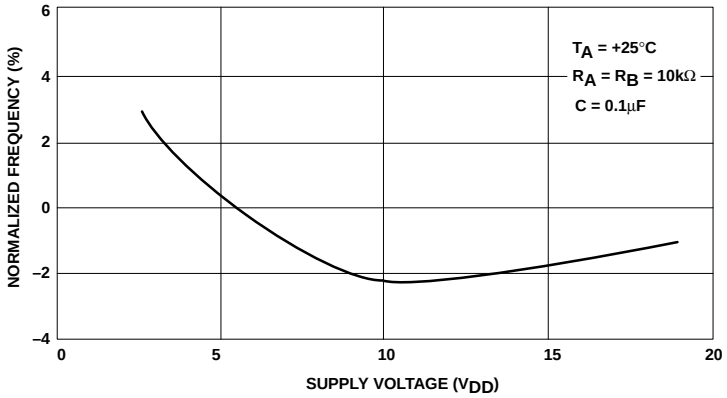


Minimum Pulse Width for Triggering

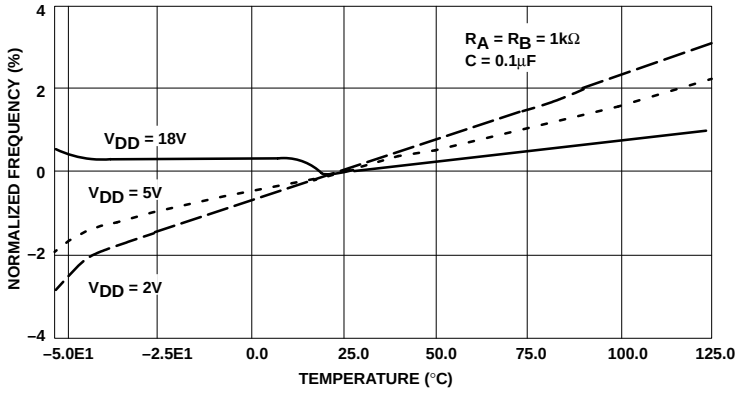
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Propagation Delay vs Voltage Level of Trigger Pulse

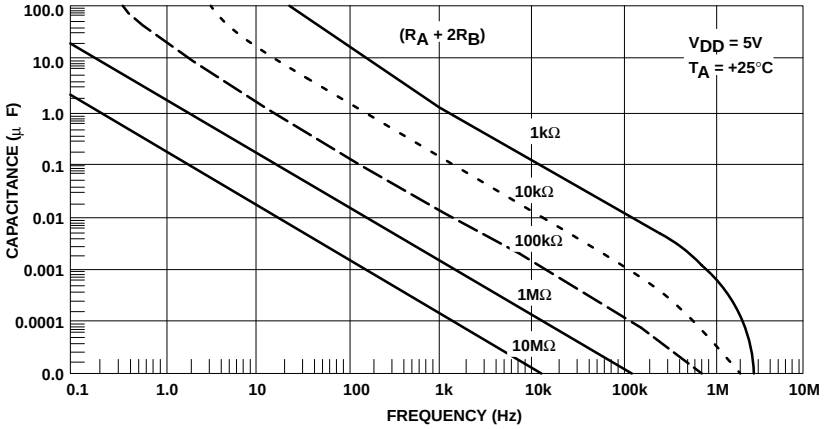


Normalized Frequency Stability as a Function of Supply Voltage (Astable Mode)

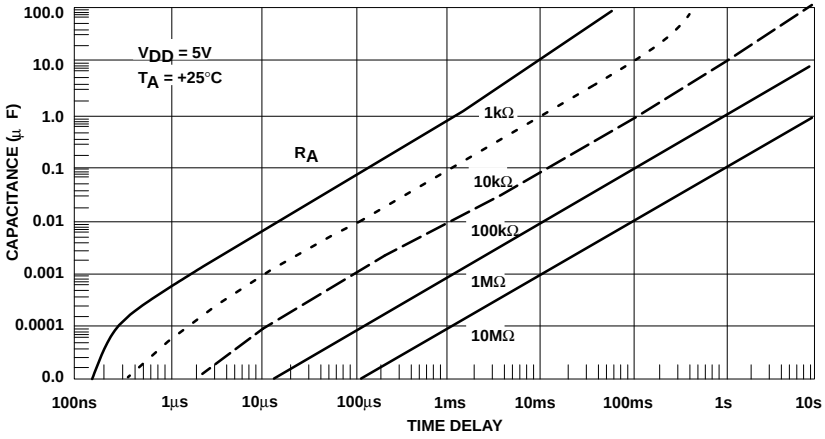


Normalized Frequency Stability as a Function of Temperature (Astable Mode)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Free-Running Frequency as a Function of R_A, R_B, and C



Monostable Time Delay vs R_A and C

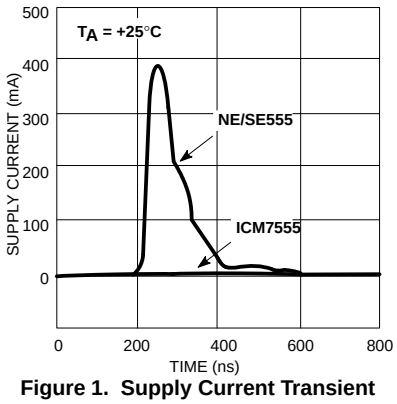


Figure 1. Supply Current Transient Compared With a Standard Bipolar 555 During an Output Transition

APPLICATION NOTES

General

The ICM7555 device is, in most instances, a direct replacement for the NE/SE555 device. However, it is possible to effect economies in the external component count using the ICM7555. Because the bipolar 555 device produces large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555 device produces no such transients. See Figure 1.

The ICM7555 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, 2 capacitors can be saved using an ICM7555.

Power Supply Considerations

Although the supply current consumed by the ICM7555 device is very low, the total system supply can be high unless the timing components are high impedance. Therefore, high values for R and low values for C in Figures 2 and 3 are recommended.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the ICM7555 will drive at least 2 standard TTL loads.

Astable Operation

If the circuit is connected as shown in Figure 2, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus, the duty cycle (D) may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{DD} and 2/3 V_{DD}. Since the charge rate and the threshold levels are directly proportional to the supply voltage, the frequency of oscillation is independent of the supply voltage.

$$F = \frac{1.38}{(R_A + 2R_B)\,C} \qquad D = \frac{R_A + R_B}{R_A + 2R_B}$$

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Initially, the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative pulse to Pin 2, $\overline{\text{TRIGGER}}$, the internal flip-flop is set which releases the low impedance on DISCHARGE; the external capacitor charges and drives the OUTPUT High. The voltage across the capacitor increases exponentially with a time constant $t = R_A C$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode, or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555, i.e., 0.6 to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

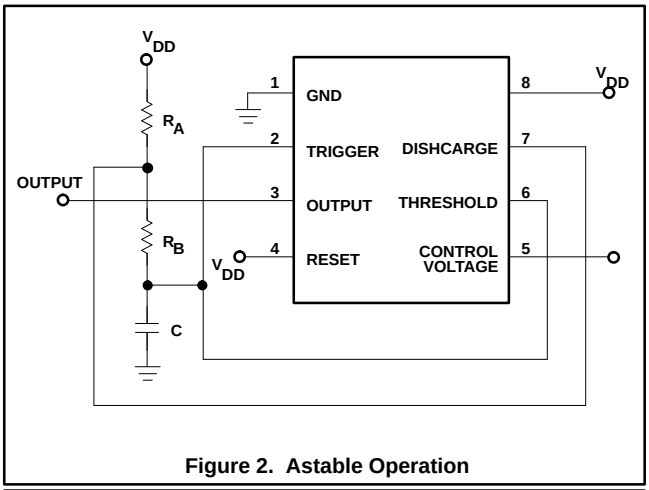


Figure 2. Astable Operation

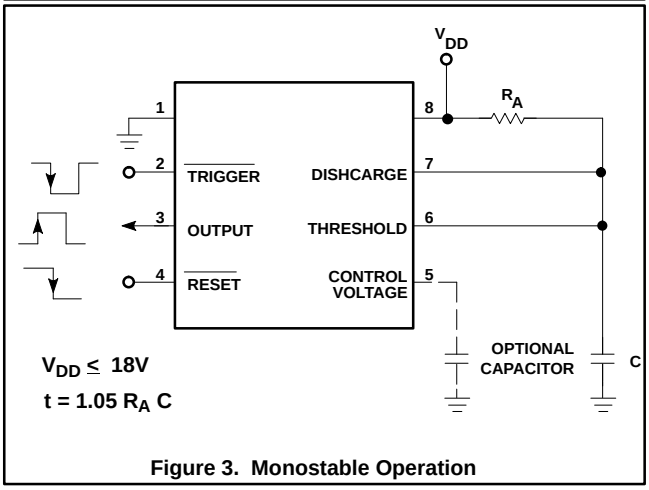


Figure 3. Monostable Operation