

DTC114EXV3T1 Series

Digital Transistors (BRT)

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The digital transistor contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The digital transistor eliminates these individual components by integrating them into a single device. The use of a digital transistor can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape & Reel
- Lead-Free Solder Plating (Pure Sn)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

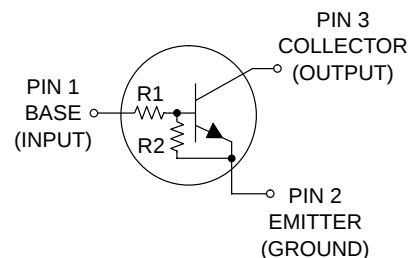
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB0}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc



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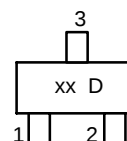
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NPN SILICON DIGITAL TRANSISTORS



SC-89
CASE 463C
STYLE 1

MARKING DIAGRAM



xx = Specific Device Code
(See Marking Table on page 2)
D = Date Code

DTC114EXV3T1 Series

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping†
DTC114EXV3T1	8A	10	10	3000/Tape & Reel
DTC124EXV3T1	8B	22	22	
DTC144EXV3T1	8C	47	47	
DTC114YXV3T1	8D	10	47	
DTC114TXV3T1	94	10	∞	
DTC143TXV3T1	8F	4.7	∞	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, FR-4 Board (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.6	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	600	$^\circ\text{C/W}$
Total Device Dissipation, FR-4 Board (Note 2) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	400	$^\circ\text{C/W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0×1.0 Inch Pad.

DTC114EXV3T1 Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	100	nAdc
Collector–Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	–	–	500	nAdc
Emitter–Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	–	–	0.5	mAdc
DTC114EXV3T1		–	–	0.2	
DTC124EXV3T1		–	–	0.1	
DTC144EXV3T1		–	–	0.2	
DTC114YXV3T1		–	–	0.9	
DTC114TXV3T1		–	–	1.9	
DTC143TXV3T1		–	–		
Collector–Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 3) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc

ON CHARACTERISTICS (Note 3)

DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	DTC114EXV3T1 DTC124EXV3T1 DTC144EXV3T1 DTC114YXV3T1 DTC114TXV3T1 DTC143TXV3T1	h_{FE}	35 60 80 80 160 160	60 100 140 140 350 350	– – – – – –	
Collector–Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$) ($I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$)	DTC143TXV3T1/DTC114TXV3T1	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	DTC114EXV3T1 DTC124EXV3T1 DTC114YXV3T1 DTC114TXV3T1 DTC143TXV3T1 DTC144EXV3T1	V_{OL}	– – – – – –	– – – – – –	0.2 0.2 0.2 0.2 0.2 0.2	Vdc
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.25\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	DTC143TXV3T1 DTC114TXV3T1	V_{OH}	4.9	–	–	Vdc
Input Resistor	DTC114EXV3T1 DTC124EXV3T1 DTC144EXV3T1 DTC114YXV3T1 DTC114TXV3T1 DTC143TXV3T1	R_1	7.0 15.4 32.9 7.0 7.0 3.3	10 22 47 10 10 4.7	13 28.6 61.1 13 13 6.1	k Ω
Resistor Ratio	DTC114EXV3T1/DTC124EXV3T1/ DTC144EXV3T1 DTC114YXV3T1 DTC143TXV3T1/DTC114TXV3T1	R_1/R_2	0.8 0.17 –	1.0 0.21 –	1.2 0.25 –	

3. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

DTC114EXV3T1 Series

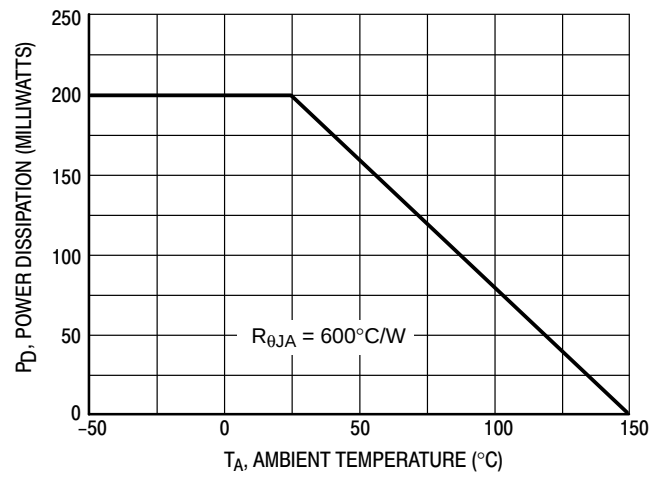


Figure 1. Derating Curve

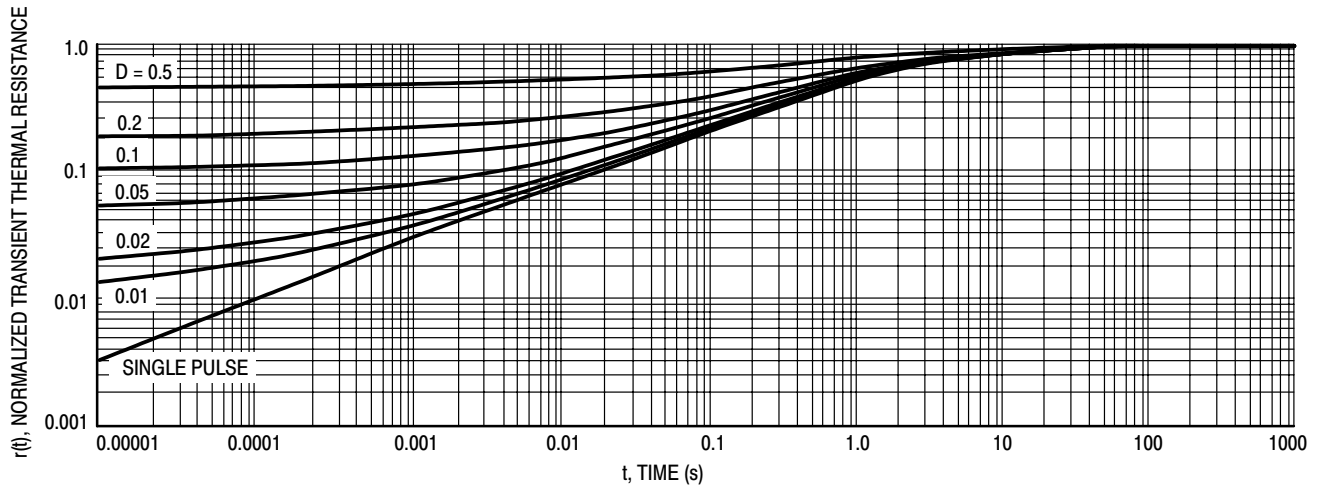


Figure 2. Normalized Thermal Response

DTC114EXV3T1 Series

TYPICAL ELECTRICAL CHARACTERISTICS – DTC114EXV3T1

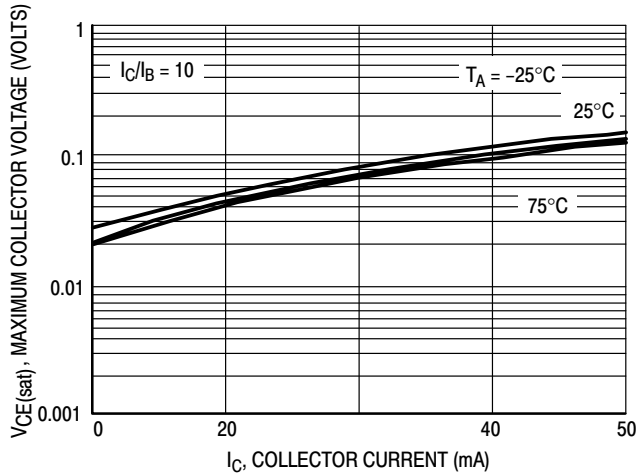


Figure 3. $V_{CE(sat)}$ versus I_C

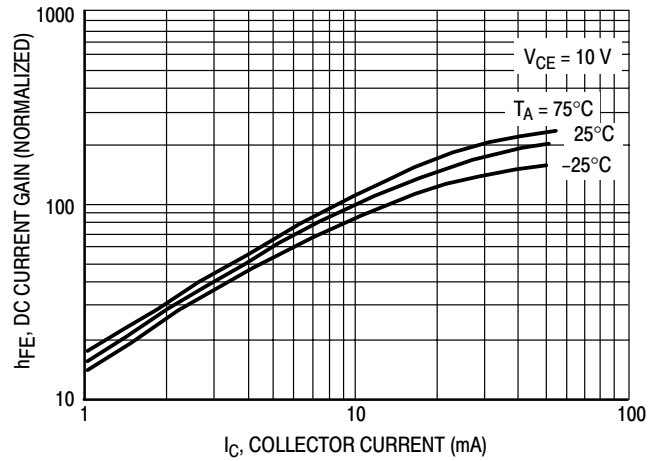


Figure 4. DC Current Gain

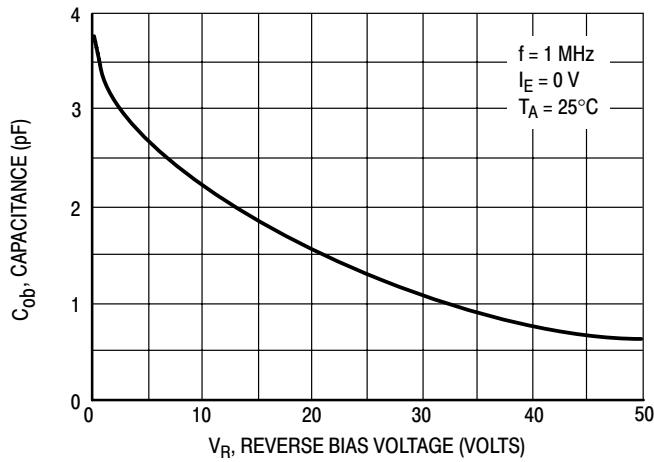


Figure 5. Output Capacitance

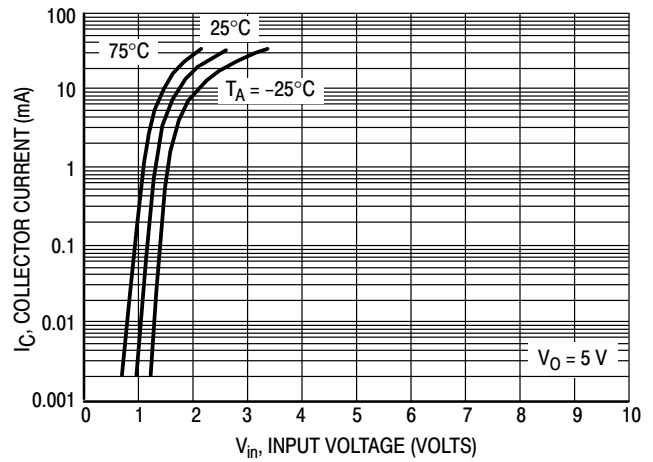


Figure 6. Output Current versus Input Voltage

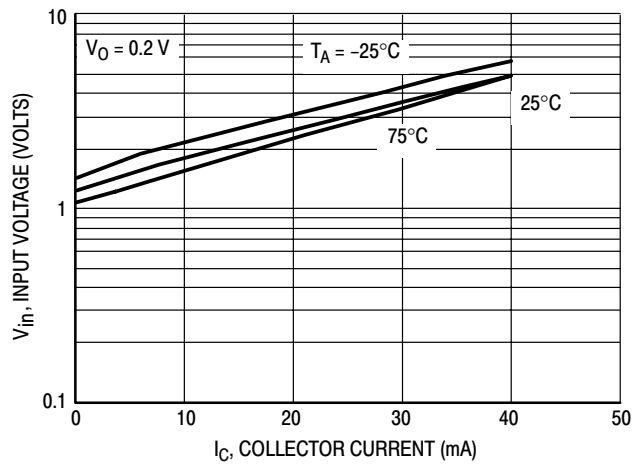


Figure 7. Input Voltage versus Output Current

DTC114EXV3T1 Series

TYPICAL ELECTRICAL CHARACTERISTICS – DTC124EXV3T1

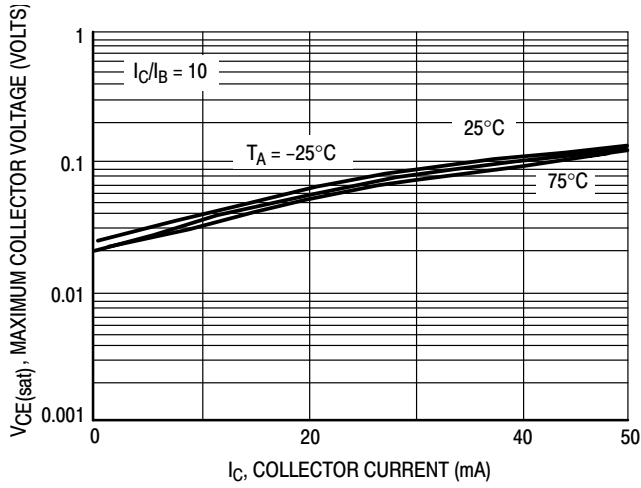


Figure 8. $V_{CE(sat)}$ versus I_C

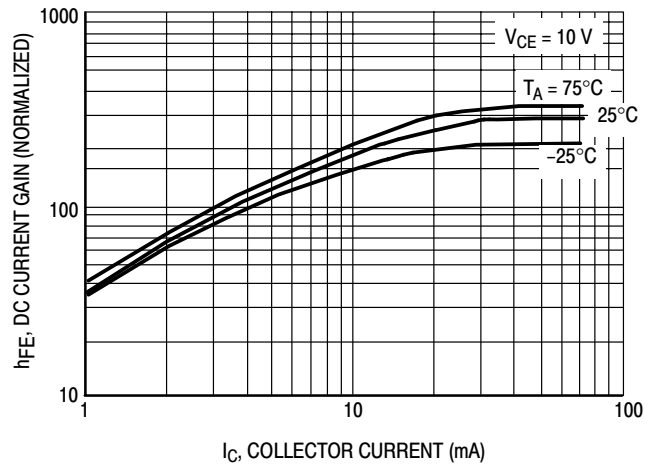


Figure 9. DC Current Gain

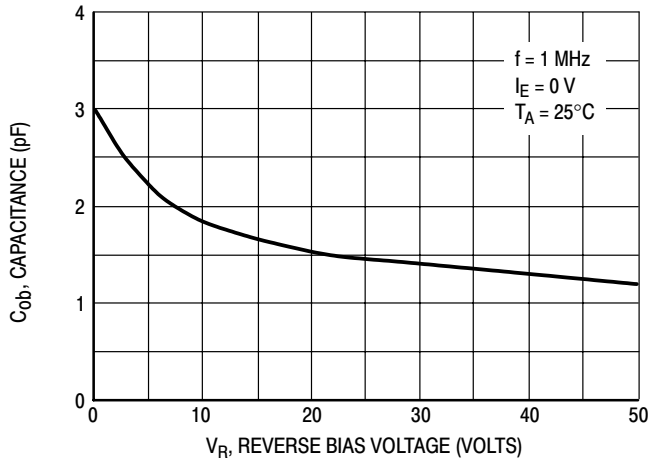


Figure 10. Output Capacitance

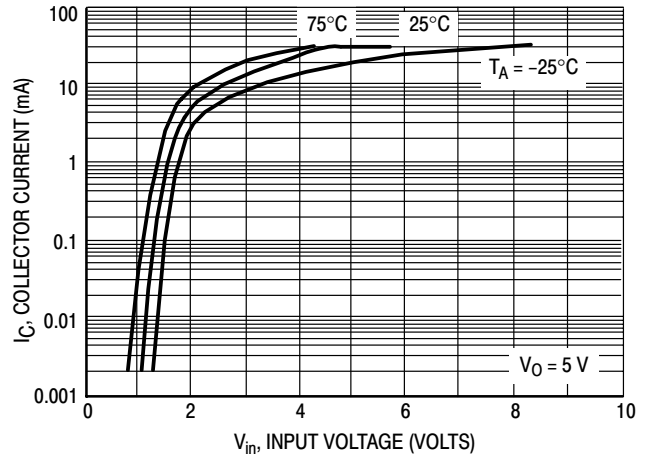


Figure 11. Output Current versus Input Voltage

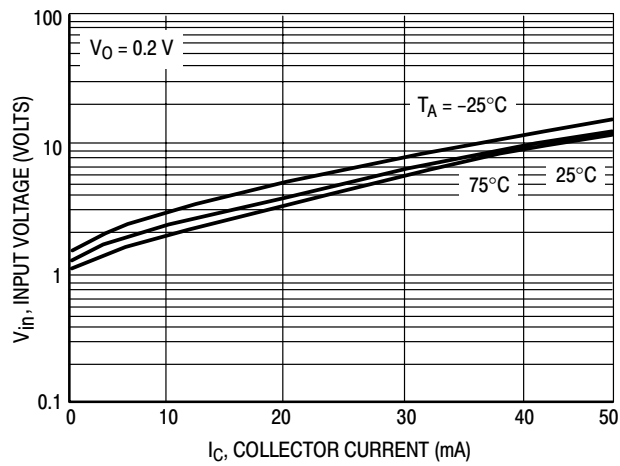


Figure 12. Input Voltage versus Output Current

DTC114EXV3T1 Series

TYPICAL ELECTRICAL CHARACTERISTICS – DTC144EXV3T1

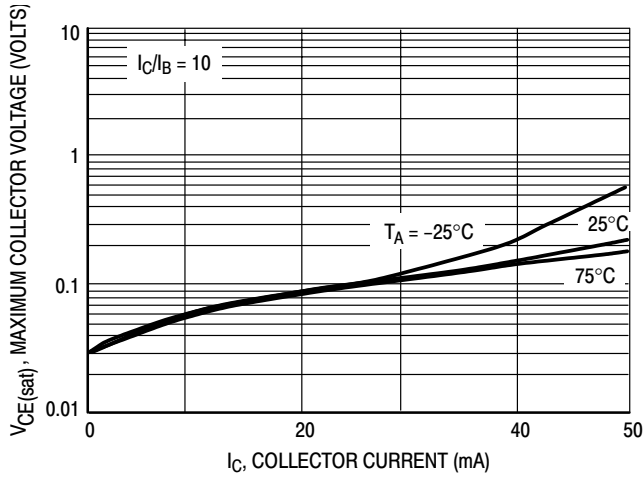


Figure 13. $V_{CE(sat)}$ versus I_C

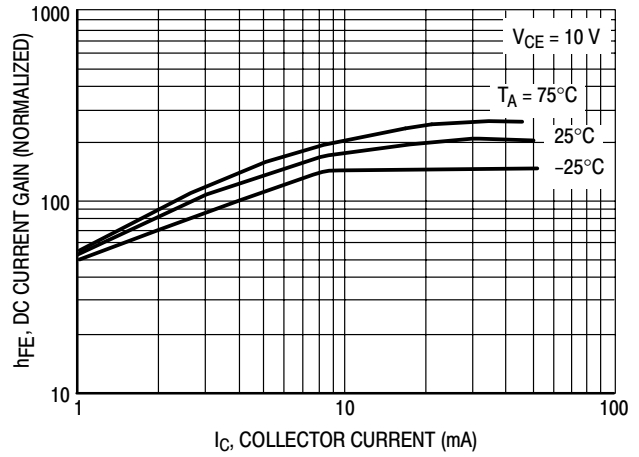


Figure 14. DC Current Gain

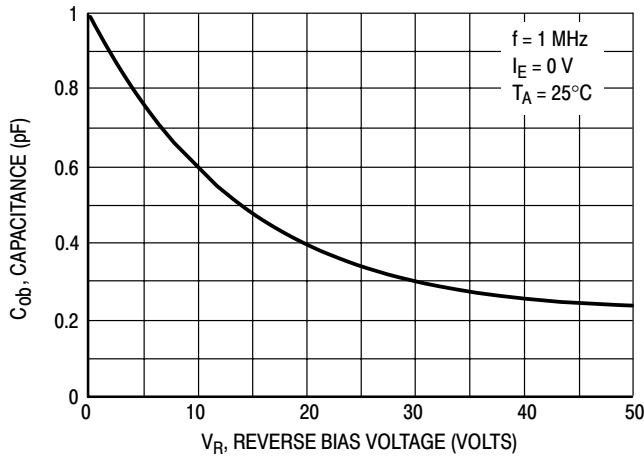


Figure 15. Output Capacitance

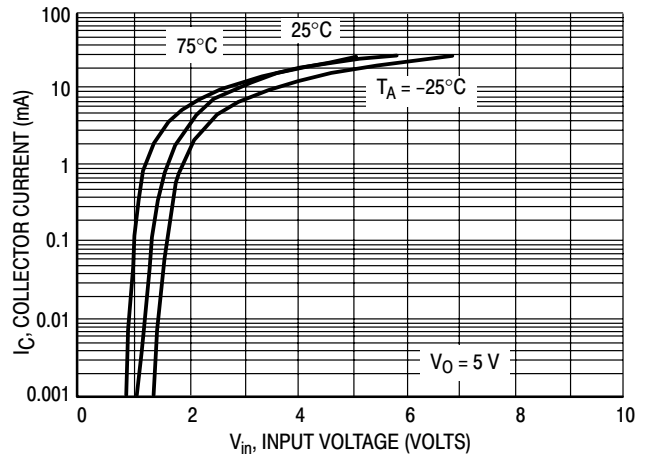


Figure 16. Output Current versus Input Voltage

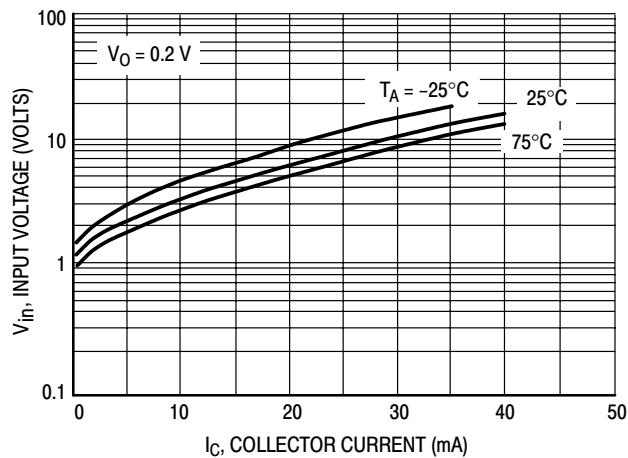


Figure 17. Input Voltage versus Output Current

DTC114EXV3T1 Series

TYPICAL ELECTRICAL CHARACTERISTICS – DTC114YXV3T1

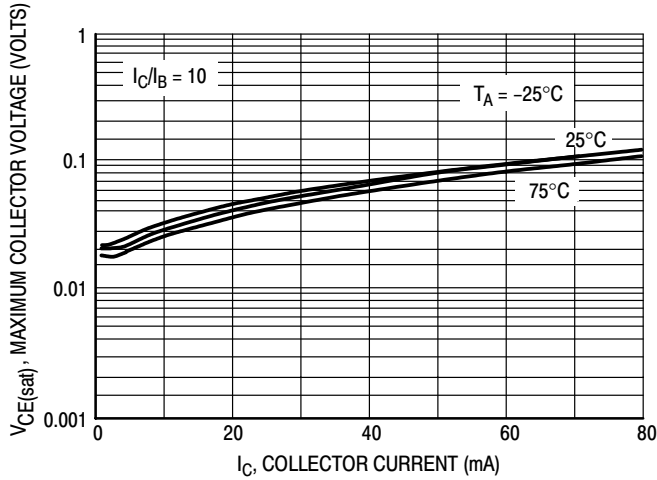


Figure 18. $V_{CE(sat)}$ versus I_C

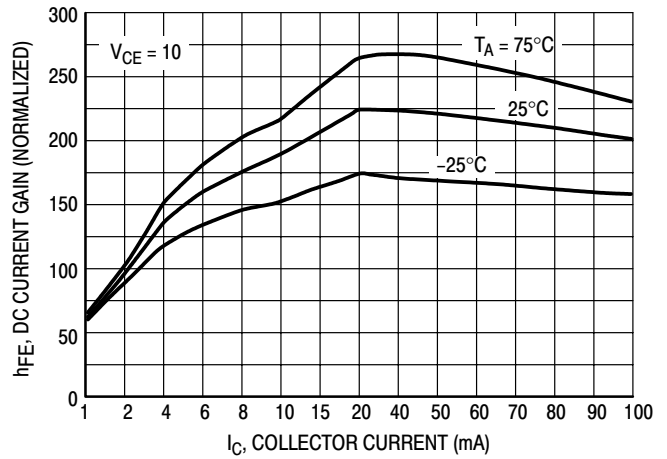


Figure 19. DC Current Gain

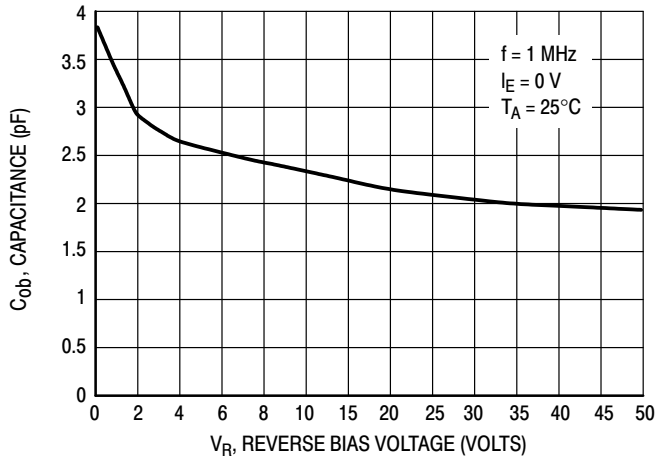


Figure 20. Output Capacitance

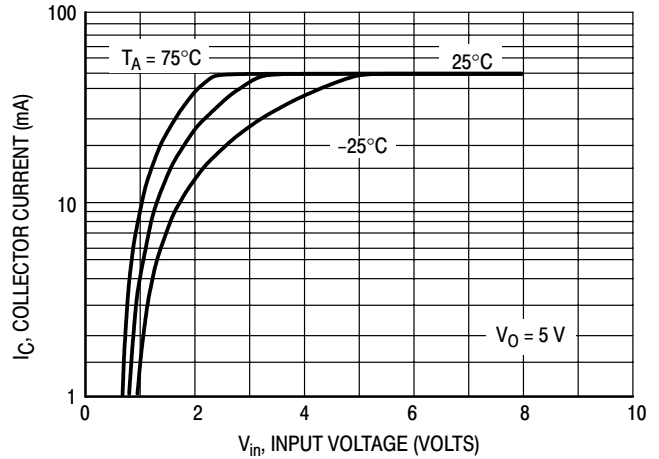


Figure 21. Output Current versus Input Voltage

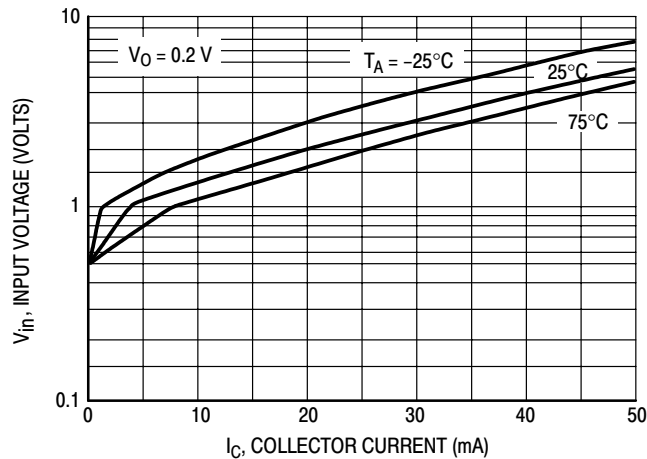


Figure 22. Input Voltage versus Output Current

DTC114EXV3T1 Series

TYPICAL APPLICATIONS FOR NPN BRTs

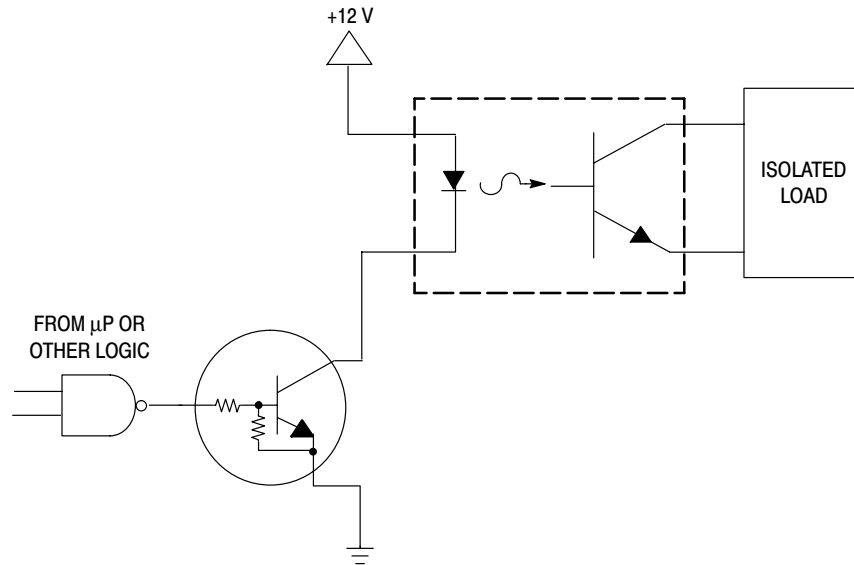


Figure 23. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

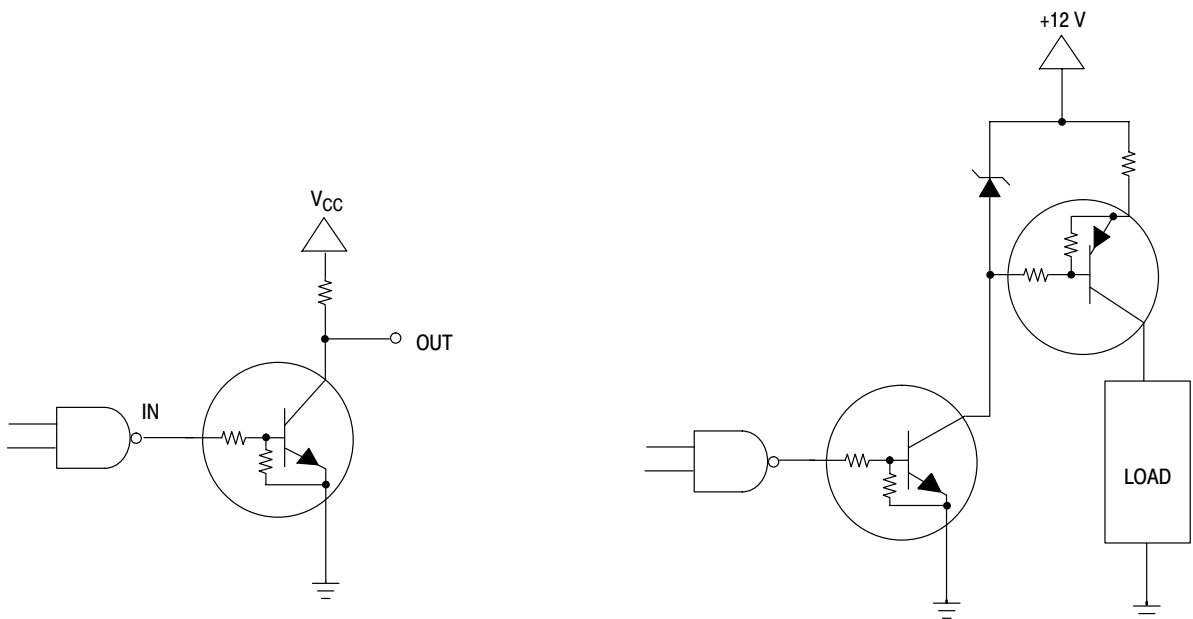


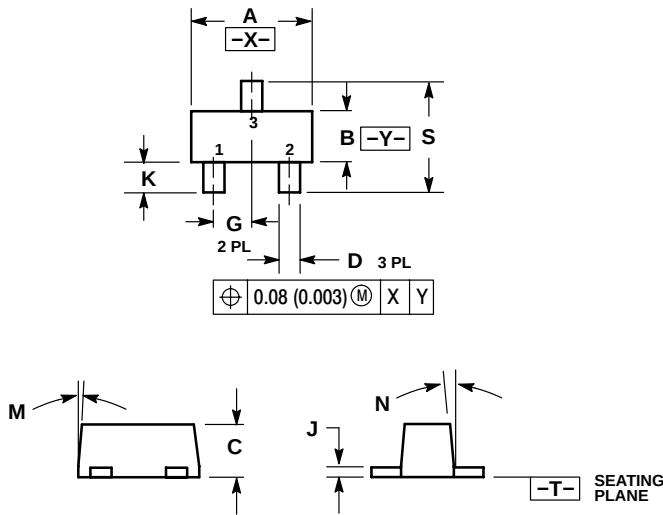
Figure 24. Open Collector Inverter:
Inverts the Input Signal

Figure 25. Inexpensive, Unregulated Current Source

DTC114EXV3T1 Series

PACKAGE DIMENSIONS

SC-89
CASE 463C-03
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10	---	---	10
N	---	---	10	---	---	10
S	1.50	1.60	1.70	0.059	0.063	0.067

STYLE 1:

1. BASE
2. EMITTER
3. COLLECTOR

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