# CBT3384

## 10-bit bus switch with 5-bit output enables

Rev. 06 — 2 November 2009 Product data sheet

## 1. General description

The CBT3384 provides ten bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3384 device is organized as two 5-bit bus switches with two separate output enable ($1\overline{OE}$, $2\overline{OE}$) inputs. When $n\overline{OE}$ is LOW, the switch is on and port A is connected to the B port. When $n\overline{OE}$ is HIGH, each switch is disabled.

The CBT3384 is characterized for operation from –40 °C to +85 °C.

## 2. Features

- 5 Ω switch connection between two ports
- TTL-compatible control input levels
- Multiple package options
- See CBTD3384 for CBT3384 with level shifting diodes
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - CDM JESD22-C101C exceeds 1000 V

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| CBT3384D | –40 °C to +85 °C | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| CBT3384DB | –40 °C to +85 °C | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 |
| CBT3384DK | –40 °C to +85 °C | SSOP24[1] | plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm | SOT556-1 |
| CBT3384PW | –40 °C to +85 °C | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |

[1] Also known as QSOP24 package

# 4. Functional diagram

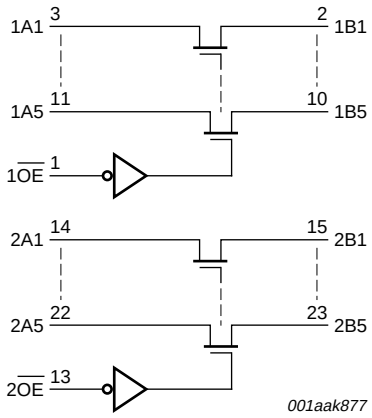



**Fig 1. Logic diagram**

# 5. Pinning information

## 5.1 Pinning

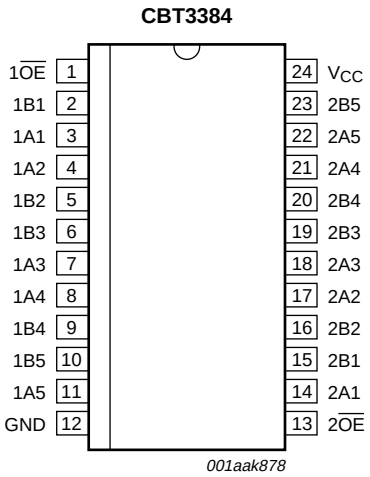



**Fig 2. Pin configuration for SO24 (SOT137-1)**

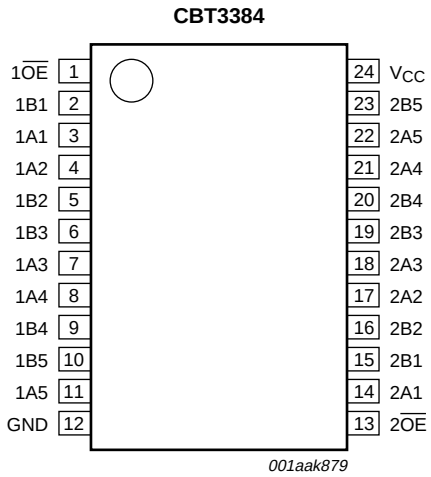



**Fig 3. Pin configuration for SSOP24 (SOT340-1) and TSSOP24 (SOT355-1)**

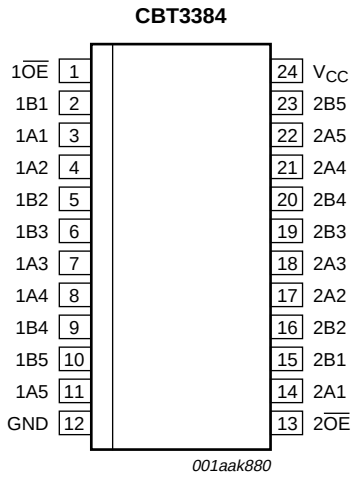



**Fig 4. Pin configuration for SSOP24 (SOT556-1)**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1$\overline{OE}$, 2$\overline{OE}$ | 1, 13 | output enable input (active LOW) |
| 1A1 to 1A5 | 3, 4, 7, 8, 11 | data input/output (A port) |
| 2A1 to 2A5 | 14, 17, 18, 21, 22 | data input/output (A port) |
| 1B1 to 1B5 | 2, 5, 6, 9, 10 | data input/output (B port) |
| 2B1 to 2B5 | 15, 16, 19, 20, 23 | data input/output (B port) |
| GND | 12 | ground (0 V) |
| $V_{CC}$ | 24 | positive supply voltage |

# 6. Functional description

**Table 3. Function selection[1]**

| Input | | Input/output | |
|---|---|---|---|
| **1$\overline{OE}$** | **2$\overline{OE}$** | **1An, 1Bn** | **2An, 2Bn** |
| L | L | 1An = 1Bn | 2An = 2Bn |
| L | H | 1An = 1Bn | Z |
| H | L | Z | 2An = 2Bn |
| H | H | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]
*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +7.0 | V |
| $V_I$ | input voltage | | [2] | −0.5 | +7.0 | V |
| $I_O$ | output current | $V_O$ < 0 V | | - | ±128 | mA |
| $I_{IK}$ | input clamping current | $V_{I/O}$ = 0 V | | −50 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 8. is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# 8. Recommended operating conditions

**Table 5. Operating conditions**

*All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 4.5 | - | 5.5 | V |
| $V_{IH}$ | HIGH-state input voltage | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-state input voltage | | - | - | 0.8 | V |
| $T_{amb}$ | ambient temperature | operating in free air | −40 | - | +85 | °C |

# 9. Static characteristics

**Table 6. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | $T_{amb}$ = −40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 4.5 V; $I_I$ = −18 mA | | - | - | −1.2 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 5.5 V; $V_I$ = GND or 5.5 V | | - | - | ±1 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 5.5 V; $I_O$ = 0 mA; $V_I$ = $V_{CC}$ or GND | | - | - | 3 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 5.5 V; one input at 3.4 V, other inputs at $V_{CC}$ or GND | [2] | - | - | 2.5 | mA |
| $V_{pass}$ | pass voltage | output HIGH; $V_I$ = $V_{CC}$ = 5.0 V; $I_O$ = −100 µA | | 3.6 | 3.9 | 4.2 | V |
| $C_I$ | input capacitance | control pins; $V_I$ = 3 V or 0 V | | - | 4.0 | - | pF |
| $C_{io(off)}$ | off-state input/output capacitance | port off; $V_I$ = 3 V or 0 V; $n\overline{OE}$ = $V_{CC}$ | | - | 10.0 | - | pF |

**Table 6. Static characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | $T_{amb}$ = –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $R_{ON}$ | ON resistance | $V_{CC}$ = 4.5 V; $V_I$ = 0 V; $I_I$ = 64 mA | [3] | - | 5 | 7 | Ω |
| | | $V_{CC}$ = 4.5 V; $V_I$ = 0 V; $I_I$ = 30 mA | [3] | - | 5 | 7 | Ω |
| | | $V_{CC}$ = 4.5 V; $V_I$ = 2.4 V; $I_I$ = –15 mA | [3] | - | 10 | 15 | Ω |

[1] All typical values are at $V_{CC}$ = 5 V, $T_{amb}$ = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

[3] Measured by the voltage drop between the nAn and the nBn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nAn or nBn) terminals.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

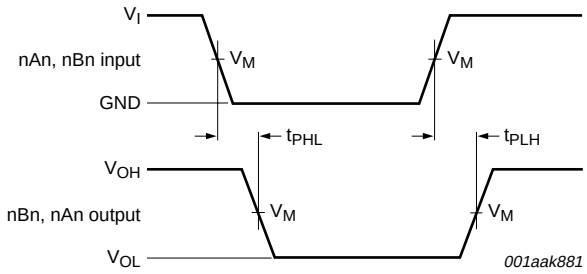
*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = 25 °C | | | $T_{amb}$ = –40 °C to +85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nAn, nBn to nBn, nAn; see Figure 5 | [1][2] | | | | | | |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | | - | - | 0.25 | - | 0.25 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $n\overline{OE}$ to nAn or nBn; see Figure 6 | | | | | | | |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | | 1.2 | 2.3 | 5.7 | 1.2 | 5.6 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | $n\overline{OE}$ to nAn or nBn; see Figure 6 | | | | | | | |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | | 1.2 | 2.3 | 5.7 | 1.2 | 6.0 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $n\overline{OE}$ to nAn or nBn; see Figure 6 | | | | | | | |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | | 1.7 | 3.6 | 5.2 | 1.7 | 5.5 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | $n\overline{OE}$ to nAn or nBn; see Figure 6 | | | | | | | |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | | 1.7 | 2.7 | 5.2 | 1.7 | 6.6 | ns |

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

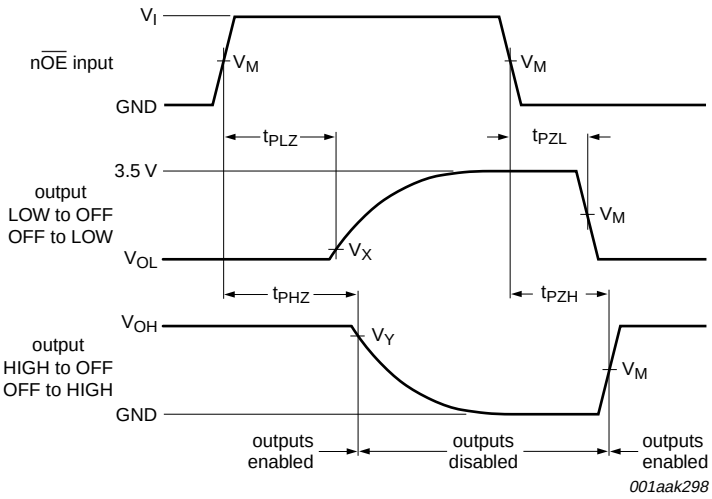
## 11. Waveforms




Measurement points are given in Table 8.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 5. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**




Measurement points are given in Table 8.

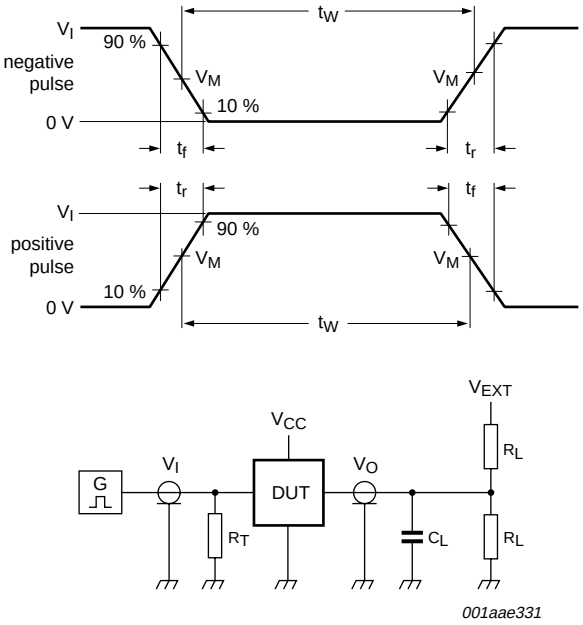
Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 6. Enable and disable times**

**Table 8. Measurement points**

| Supply voltage | Input | | Output | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| $V_{CC}$ = 5.0 V ± 0.5 V | GND to 3.0 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |

## 12. Test information




Test data is given in Table 9.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; $Z_o$ = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

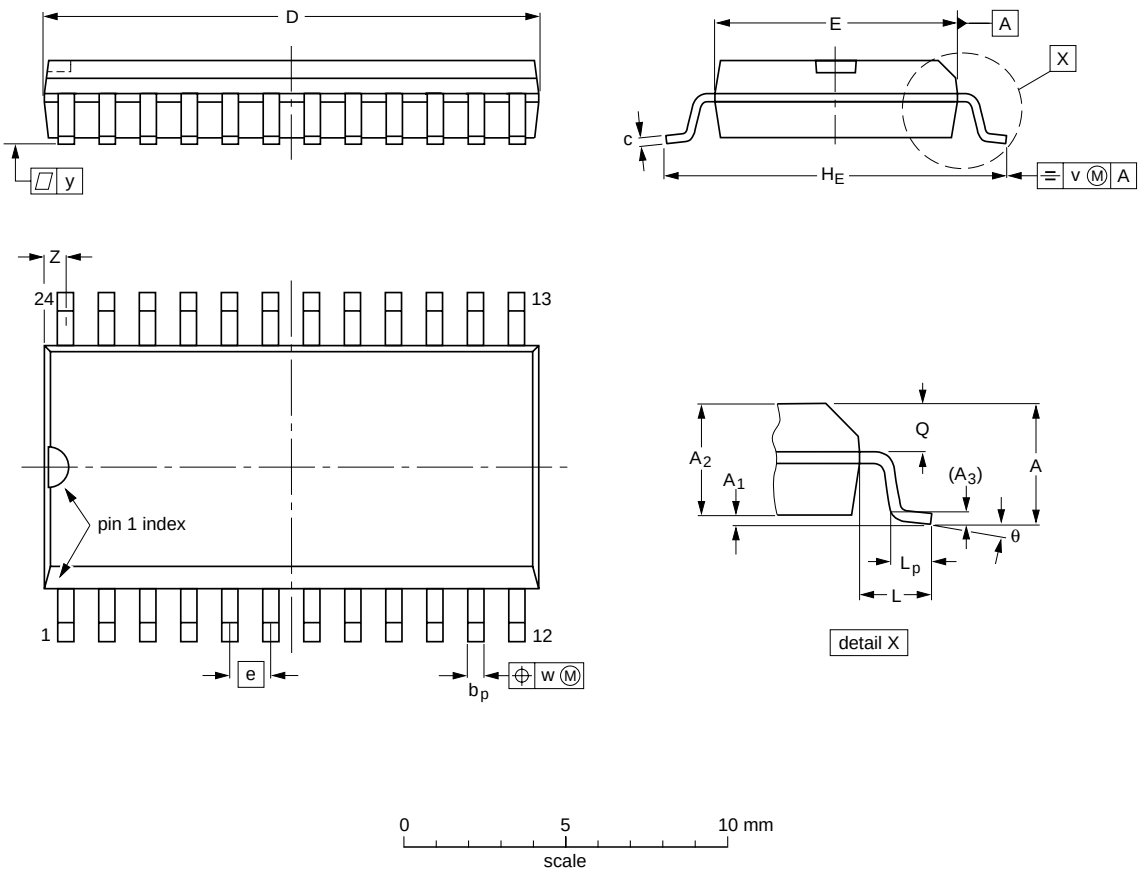
**Fig 7. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| $V_{CC}$ = 5.0 V ± 0.5 V | GND to 3.0 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 7.0 V | open |

## 13. Package outline

**SO24: plastic small outline package; 24 leads; body width 7.5 mm** **SOT137-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 15.6<br>15.2 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

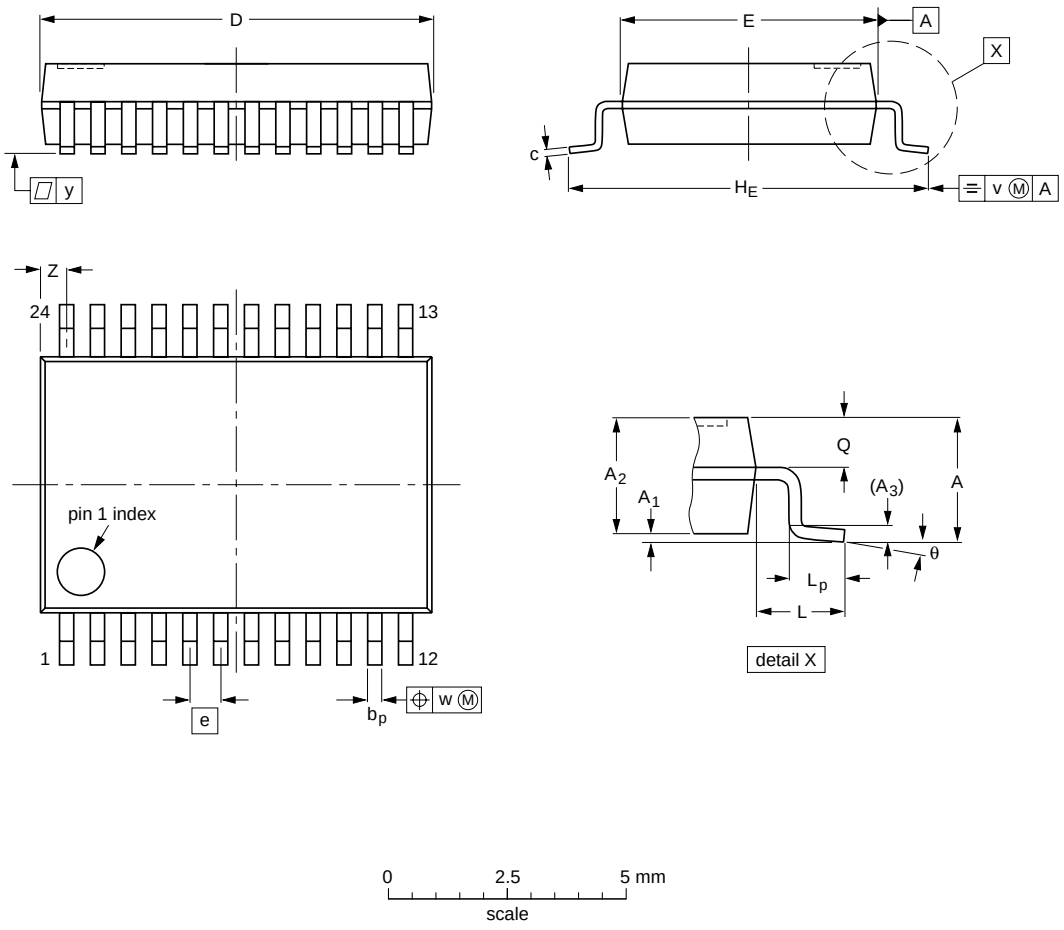
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT137-1 | 075E05 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 8. Package outline SOT137-1 (SO24)**

**SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm** **SOT340-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 8.4<br>8.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.8<br>0.4 | $8^o$<br>$0^o$ |

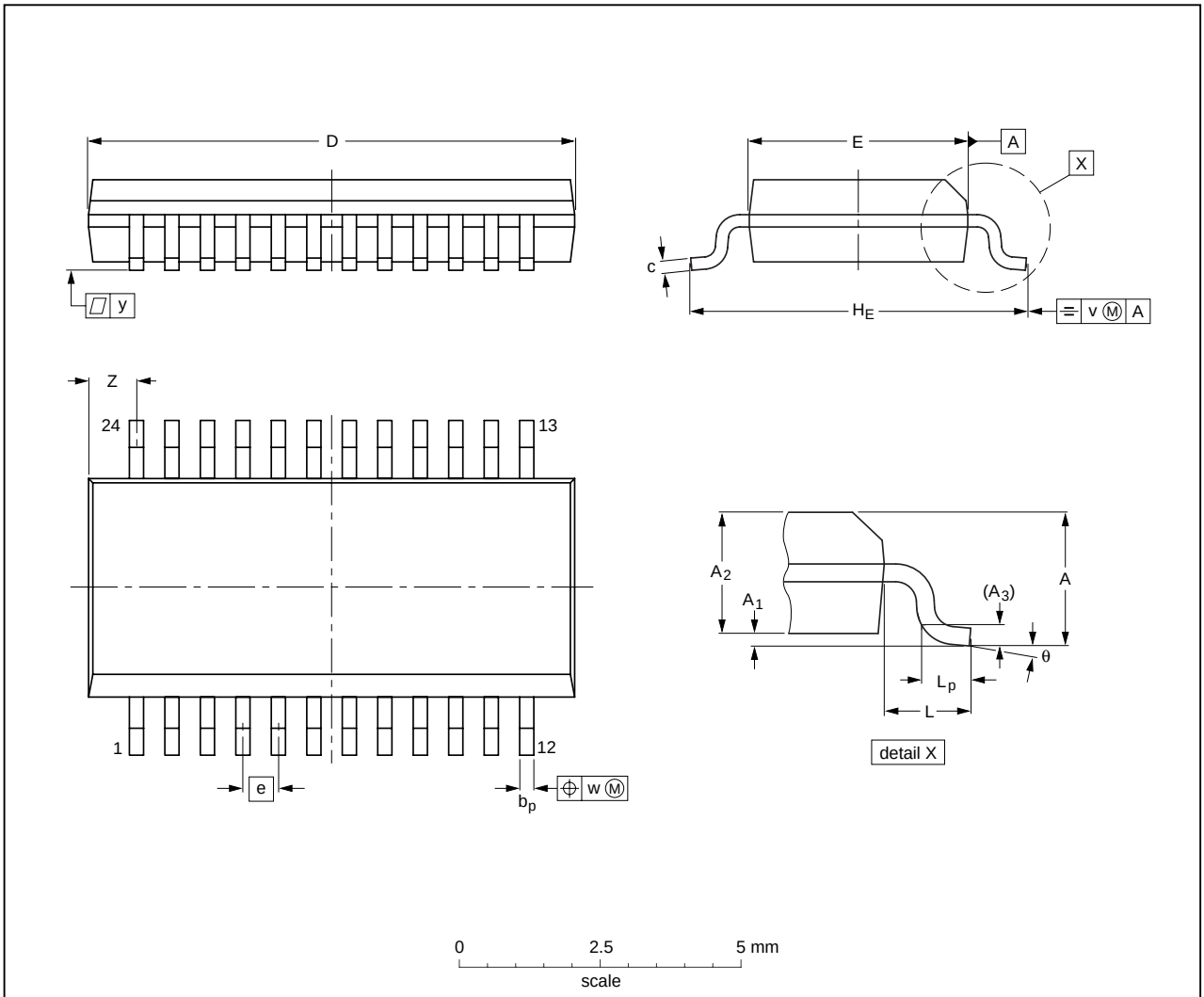
**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT340-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT340-1 (SSOP24)**

**SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm** **SOT556-1**




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.73 | 0.25<br>0.10 | 1.55<br>1.40 | 0.25 | 0.31<br>0.20 | 0.25<br>0.18 | 8.8<br>8.6 | 4.0<br>3.8 | 0.635 | 6.2<br>5.8 | 1 | 0.89<br>0.41 | 0.25 | 0.18 | 0.1 | 1.05<br>0.66 | $8^o$<br>$0^o$ |
| inches | 0.068 | 0.0098<br>0.0040 | 0.061<br>0.055 | 0.01 | 0.012<br>0.008 | 0.0098<br>0.0075 | 0.344<br>0.337 | 0.157<br>0.150 | 0.025 | 0.244<br>0.228 | 0.041 | 0.035<br>0.016 | 0.01 | 0.007 | 0.004 | 0.040<br>0.026 | $8^o$<br>$0^o$ |

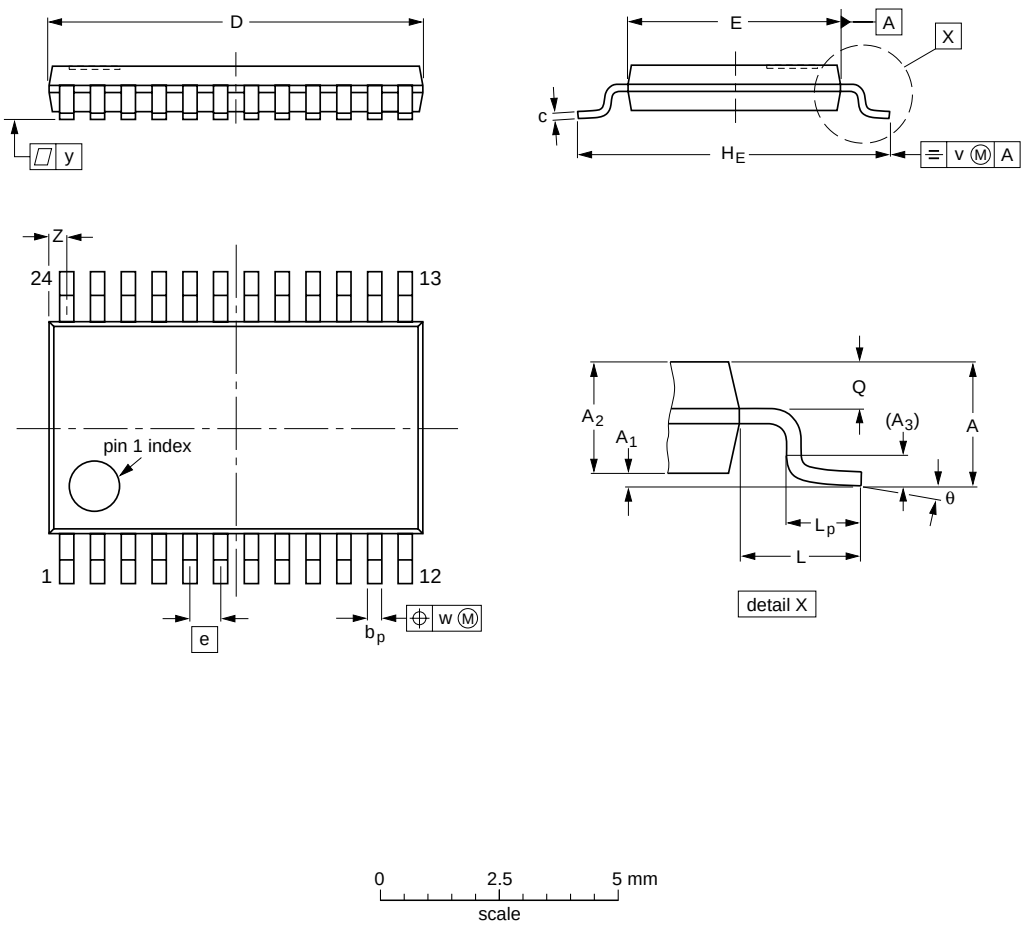
**Note**

1. Plastic or metal protrusions of 0.2 mm (0.008 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT556-1 | | MO-137 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 10. Package outline SOT556-1 (SSOP24)**

**TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm** **SOT355-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 7.9<br>7.7 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT355-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 11. Package outline SOT355-1 (TSSOP24)**

## 14. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| FET | Field Effect Transistor |
| HBM | Human Body Model |
| PRR | Pulse Rate Repetition |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| CBT3384_6 | 20091102 | Product data sheet | - | CBT3384_5 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Changed: Table 6 “Static characteristics”<br>a. Pass voltage values have changed.<br>b. Undershoot static current protection removed.<br>• Changed: Table 7 “Dynamic characteristics”<br>a. Enable and disable times values have changed. | | | |
| CBT3384_5 | 20011220 | Product specification | - | CBT3384_4 |
| CBT3384_4 | 20010319 | Product specification | - | CBT3384_3 |
| CBT3384_3 | 20001113 | Product specification | - | CBT3384_2 |
| CBT3384_2 | 20000128 | Product specification | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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