

POWER MANAGEMENT

Description

The SC1592 is a 3A low dropout high performance linear voltage regulator, that provides a low voltage, high current output with a minimum of external components, utilizing dual supply configuration.

The SC1592 offers a wide input voltage range from 1.25V to 16V and is ideal for applications that need to convert down to 0.8V.

Additionally, the SC1592 is fully protected with an externally programmable current limit, and thermal shutdown. Also, there is an EN input which enables or shuts down the device.

The SC1592 voltage regulator is available in 7-lead DDPAK and SOIC-8L EDP packages.

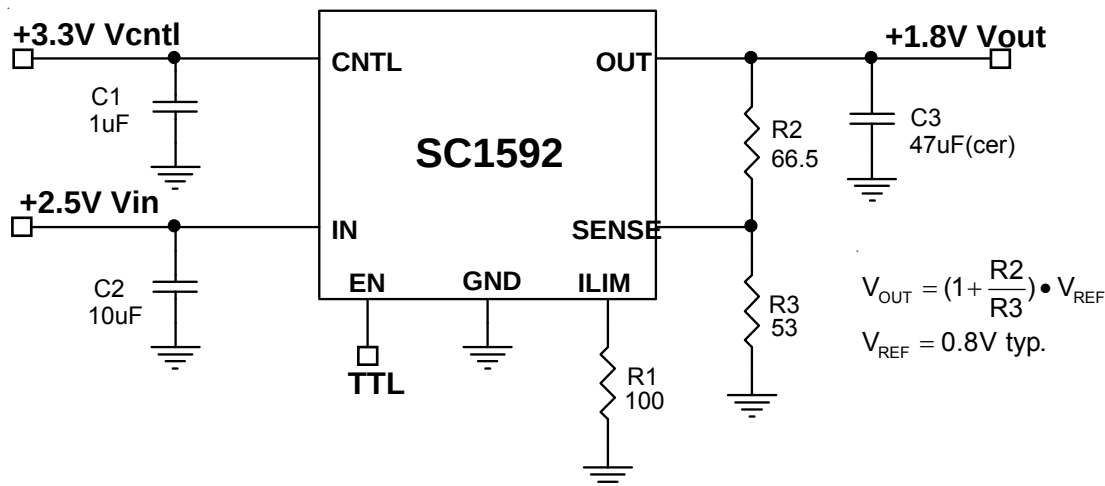
Features

- ◆ Wide input range, $V_{IN} = 1.25V$ to $16V$,
 $V_{CNTL} = 3V$ to $16V$
- ◆ 3A Guaranteed Output Current
- ◆ 260mV (typ) @ 3A dropout voltage in dual supply mode
- ◆ 1% Initial Accuracy
- ◆ Adjustable output voltage, down to 0.8V
- ◆ Programmable current limiting and thermal shutdown
- ◆ Fast transient response
- ◆ Excellent line and load regulation
- ◆ Power SO-8 and 7-lead DDPAK

Applications

- ◆ Low voltage logic supplies
- ◆ Microprocessor and chipset supplies
- ◆ Split plane microprocessor supplies
- ◆ Advanced graphics cards supplies
- ◆ Sound cards and auxiliary power supplies
- ◆ SMPS post regulator

Typical Application Circuit



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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Power Input Voltage	V_{IN}	18	V
Control Input Voltage	V_{CNTL}	18	V
Output Current	I_{OUT}	5	A
Power Dissipation	P_D	Internally Limited	W
Thermal Resistance Junction to Ambient DDPAK (1sq. in.) SOIC-8L EDP (1sq. in.)	θ_{JA}	29 36.5	°C/W
Thermal Resistance Junction to Case DDPAK SOIC-8L EDP	θ_{JC}	3 5.5	°C/W
Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

Unless specified: $V_{IN} = 2.5V$, $V_{EN} = V_{CNTL} = 3.3V$, $V_{OUT} = 1.8V$, $I_{OUT} = 10mA$, $R_{LIM} = 100\Omega$, $T_J = T_A = 25^\circ C$.
Values in **bold** indicate $-40^\circ C < T_J < +125^\circ C$.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Control Voltage	V_{CNTL}	$V_{OUT} = V_{REF}$	3		16	V
Reference Voltage	V_{REF}	$V_{OUT} = V_{REF}$	792	800	808	mV
Control Pin Current	I_{CNTL_EN}	$V_{CNTL} = V_{IN} = V_{EN} = 16V$ $V_{OUT} = V_{REF}$; $I_O = 0$		3	8	mA
		$V_{CNTL} = V_{IN} = V_{EN} = 16V$ $V_{OUT} = V_{REF}$; $I_O = 3A$		24		
Control Pin Current in Shutdown	I_{CNTL_DIS}	$V_{CNTL} = V_{IN} = 16V$ $V_{EN} = 0$		1	5	μA
V_{IN} Line Regulation	$REG_{(LINE)}$	$2.5V \leq V_{IN} \leq 16V$		0.01	0.1	%/V
V_{CNTL} Line Regulation	$REG_{(CNTL)}$	$3.3V \leq V_{CNTL} \leq 16V$, $V_{OUT} = V_{REF}$		0.1	0.4	%/V
Load Regulation ⁽¹⁾	$REG_{(LOAD)}$	$10mA \leq I_{OUT} \leq 2A$, $T_J = 25^\circ C$		0.8	1.5	%
		$10mA \leq I_{OUT} \leq 3A$, $-40 < T_J < 125^\circ C$		1.4	3	%
Dropout Voltage	V_{DO}	$I_{OUT} = 2A$; $V_{OUT} = 0.98 V_{nom}$		160	320	mV
		$I_{OUT} = 3A$; $V_{OUT} = 0.98 V_{nom}$		260	520	

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Electrical Characteristics (Cont.)

Unless specified: $V_{IN} = 2.5V$, $V_{EN} = V_{CNTL} = 3.3V$, $V_{OUT} = 1.8V$, $I_{OUT} = 10mA$, $R_{LIM} = 100\Omega$, $T_J = T_A = 25^\circ C$.
 Values in **bold** indicate $-40^\circ C < T_J < +125^\circ C$.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Thermal Shutdown	T_{SHUT}			150		$^\circ C$
Thermal Shutdown Hysteresis				10		$^\circ C$
SENSE Input Current				1		μA
Low Level EN					0.8	V
High Level EN			2			V
EN Input Current		$V_{EN} = V_{CNTL} = 5V$		55	100	μA
EN Impedance				65		$K\Omega$
Current Limit Accuracy ⁽²⁾	I_{LIM}		-20		+20	%

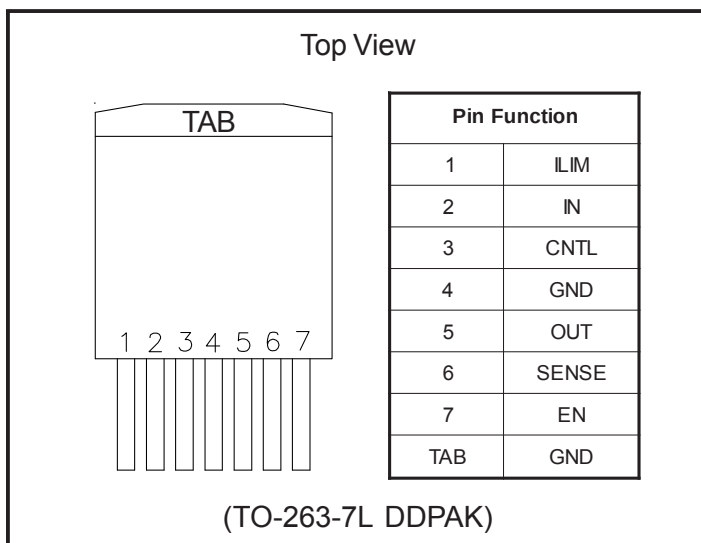
Notes:

(1) For load regulation use a 1ms current pulse width, d.c. $\leq 10\%$ when measuring VOUT.

(2) Current limit is programmable, $I_{LIM} \approx \frac{240 \cdot V_{OUT}}{R_{LIM}}$

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Pin Configurations



Ordering Information

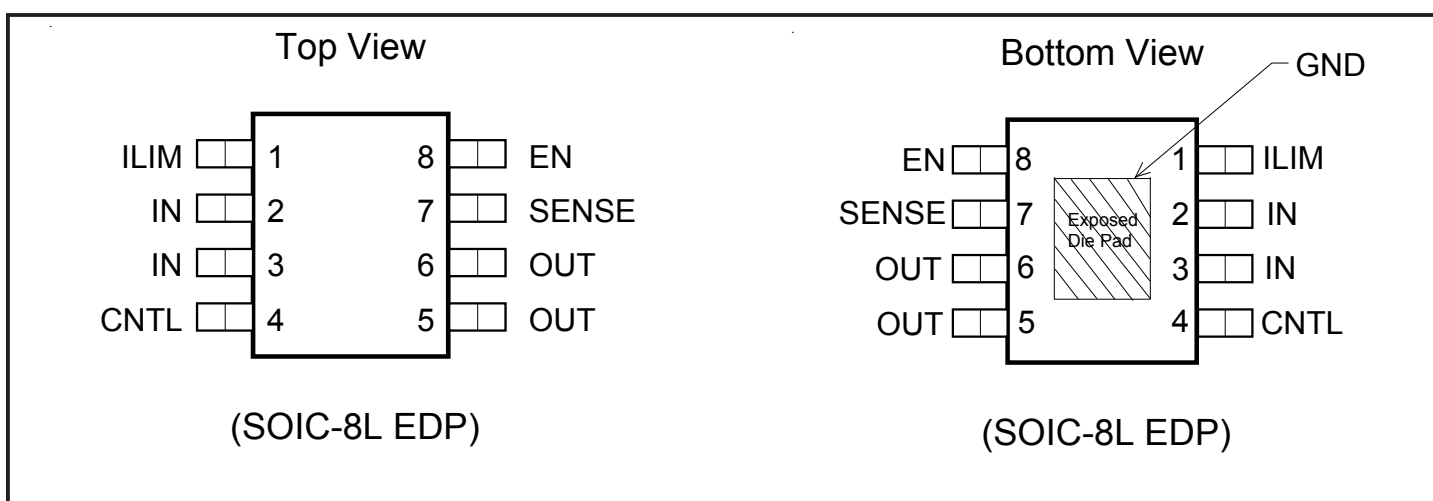
Part Number	Package ⁽¹⁾	Temp. Range (T _J)
SC1592IMTR	TO-263-7L	-40°C to +125°C
SC1592IMTRT ⁽³⁾		
SC1592ISTR	SOIC-8L EDP	
SC1592ISTR ⁽³⁾		
SC1592EVB ⁽²⁾	Evaluation Board	

Notes:

(1) Only available in tape and reel packaging. A reel contains 800 devices for TO-263 package and 2500 devices for SOIC package.

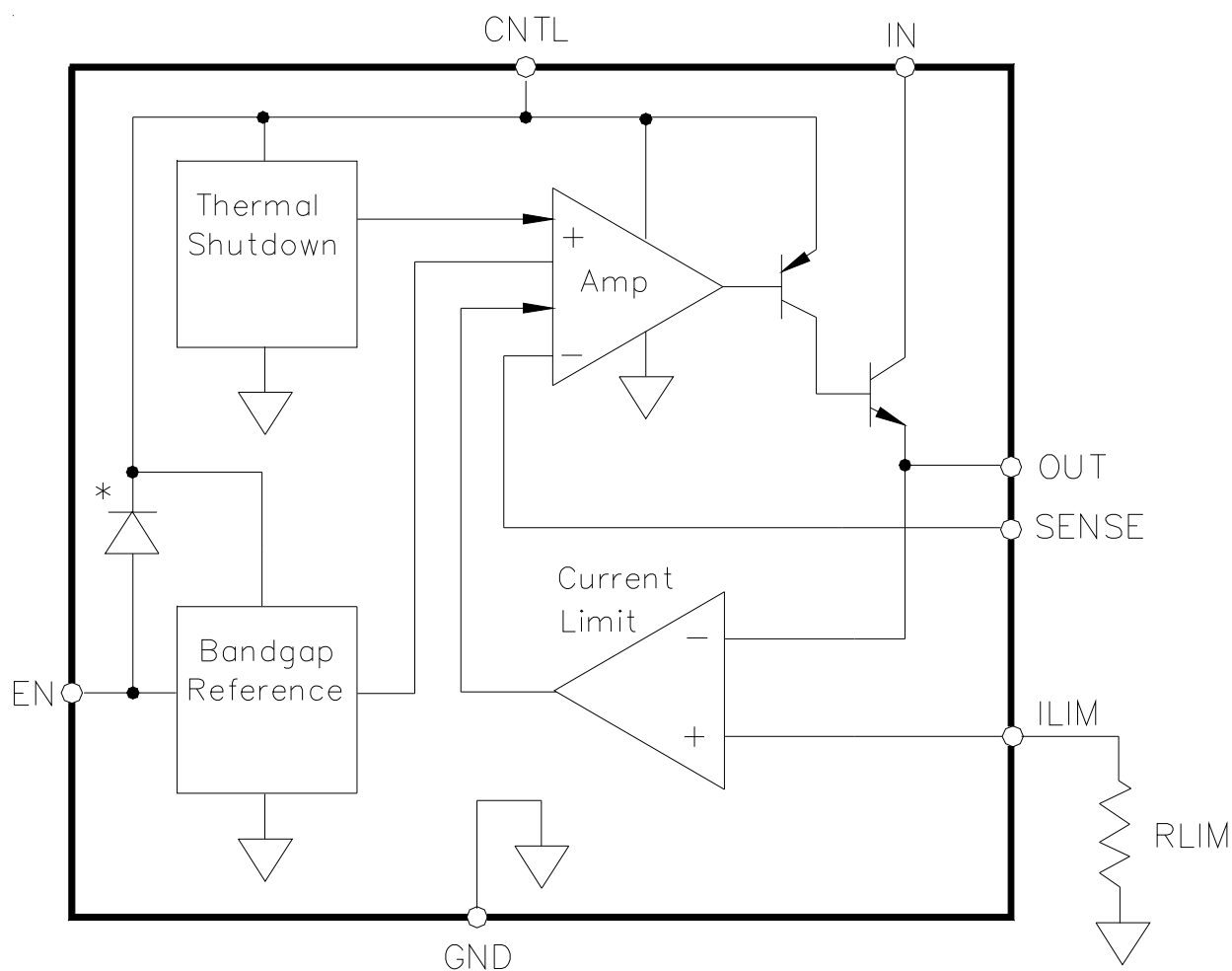
(2) When ordering Evaluation Board please specify package needed (TO-263(DDPAK) or SOIC(EDP)).

(3) Lead free product.



Pin Descriptions

Pin # DDPAK	Pin # SOIC	Pin Name	Pin Function
1	1	ILIM	Externally programmable current limit should be set at < 5A.
2	2, 3	IN	This is the collector input to the power device. The output load current is supplied through this pin.
3	4	CNTL	This pin is the bias supply for the control circuitry. The current flow into this pin will be approximately 1% of the output current. For the device to regulate, the voltage on this pin must be at least 1.5V greater than the output voltage, but no less than V _{CNTL_MIN} .
4, TAB	PAD	GND	Ground.
5	5, 6	OUT	This is the power output of the device.
6	7	SENSE	This is a feedback input.
7	8	EN	Enable input. When high, should be less or equal to V _{CNTL} .

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Block Diagram

Figure 1

$$R_{LIM} \approx 240 \times \left[\frac{V_{OUT}}{I_{LIM}} \right]$$

I_{LIM} = Selected current limit value

V_{OUT} = Regulated output voltage

R_{LIM} = Externally programmable current limit resistor.

Accuracy of the current limit setting is better than $\pm 20\%$ over full operating temperature range.

*Internal ESD structure. In cases where EN is permanently tied to V_{IN} , it's recommended that a 10-20k resistor should be inserted in the link between EN and V_{IN} .

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Application Information

The SC1592 is a 3A low dropout high performance linear voltage regulator. The SC1592 can be used for voltage applications as low as 0.8V and is ideal for down conversion utilizing dual supply configuration. This allows for extremely low dropout voltages with excellent load and line regulation. The SC1592 can be utilized in high voltage applications, with V_{IN} and V_{CNTL} up to 16V, providing there is adequate thermal management.

SC1592 is designed to meet stringent requirements of current generation microprocessors and other sensitive electronic devices. This is possible by employing an additional bias source, V_{CNTL} . The voltage of this supply needs to be at least 1.5V greater than the output voltage in order to achieve low dropout, typically less than 300mV.

Unlike most of the other high current linear regulators, the SC1592 provides a programmable current limit which can be set with a single resistor. The value of the programming resistor is:

$$I_{LIM} \approx \frac{240 \cdot V_{OUT}}{R_{LIM}}$$

where I_{LIM} = selected current limit value
 V_{OUT} = regulated output voltage
 R_{LIM} = programmable current limit resistor

The SC1592 has a fast transient response that allows it to handle large load changes associated with high current applications. Proper selection of the of the output capacitor and it's ESR value determines stable operation and optimizes performance.

The typical application shown in Figure 2 was tested with a wide range of different capacitors. The circuit was found to be unconditionally stable with capacitor values from 47 μ F to 330 μ F and ESR ranging from 0.5m Ω to greater than 75m Ω .

It's recommended to maintain 5-10mA through the output divider network in order to have a tight load and line regulation. Initial accuracy of the internal voltage reference $V_{REF} = 0.8V \pm 1\%$ over full temperature range. This commands the use of 0.5% or better accuracy resistors to build a precision power supply.

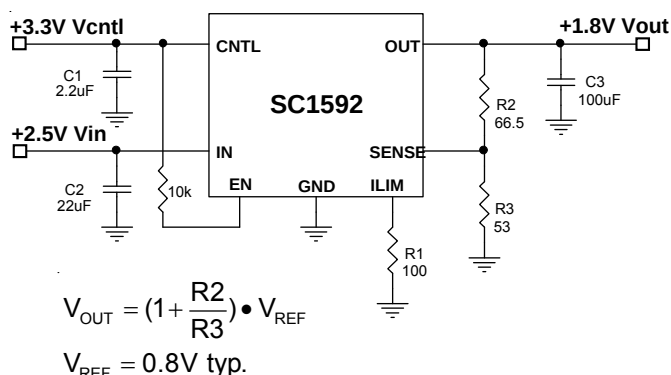


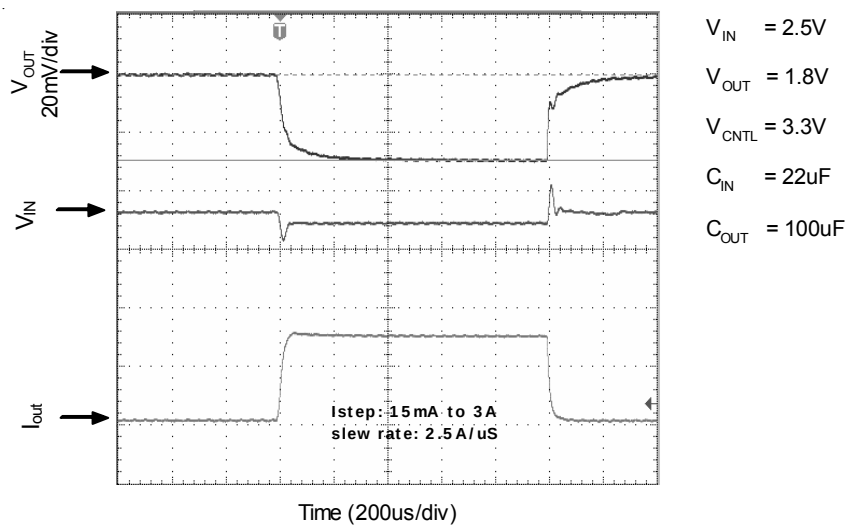
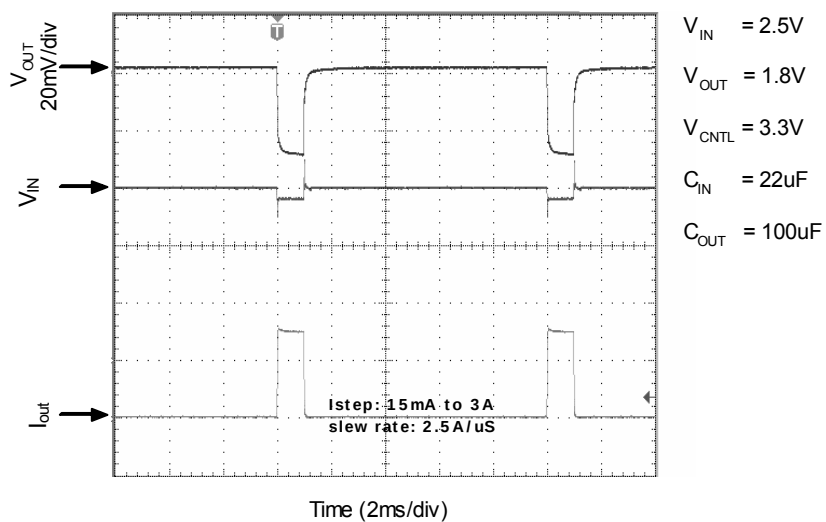
Figure 2

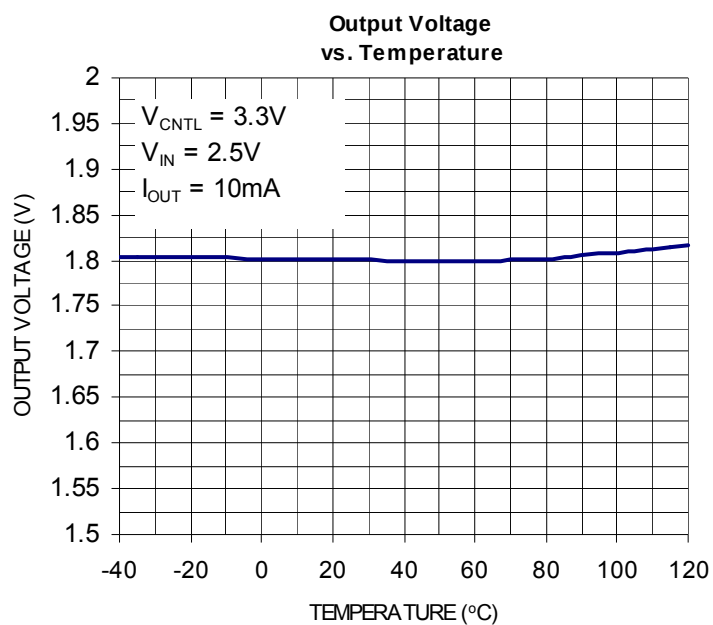
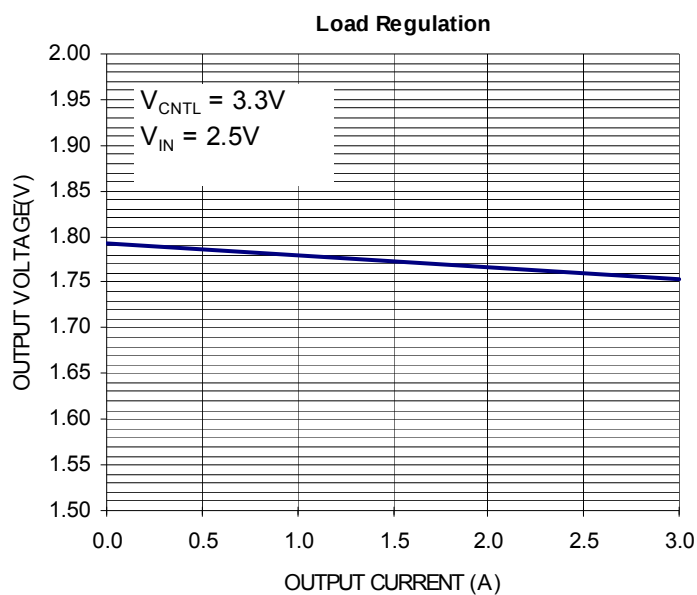
The circuit in Figure 2 shows a typical application of 2.5V to 1.8V conversion with a 3.3V control supply and the load range of up to 3A steady state. Considering the approximate 2W power being dissipated by the pass element of the SC1592, we are still able to choose an SO-8 EDP package with $T_{JA} = 36.5^\circ\text{C/W}$ mount on the 1sq.in. copper pad allocated for adequate heat transfer.

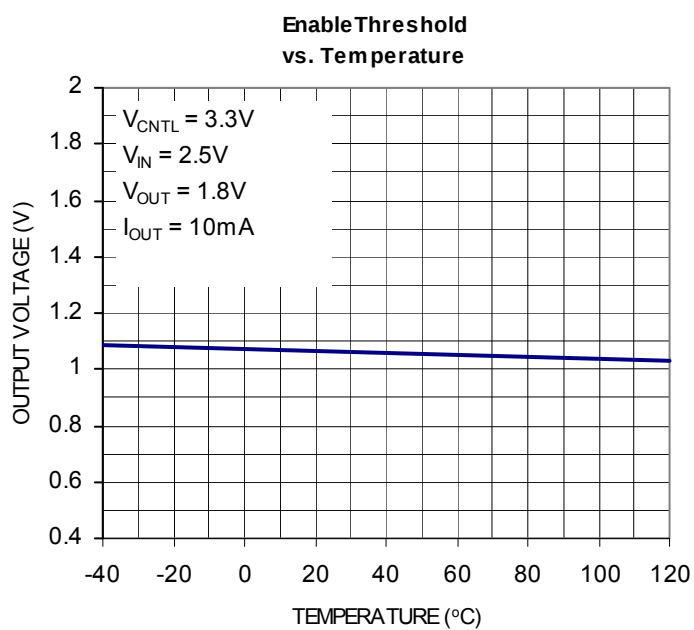
The ambient temperature in this case should not exceed 50°C. If this temperature range is too restrictive, then the DPAK can be utilized, having $T_{JA} = 29^\circ\text{C/W}$ mount on the same size copper pad.

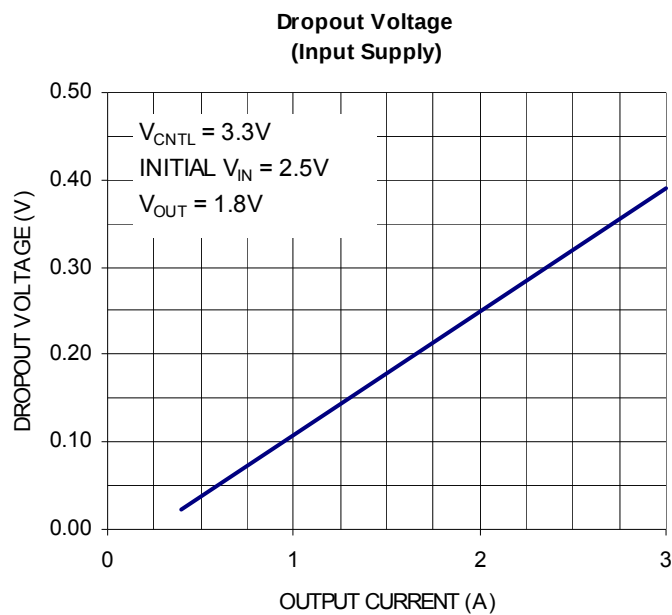
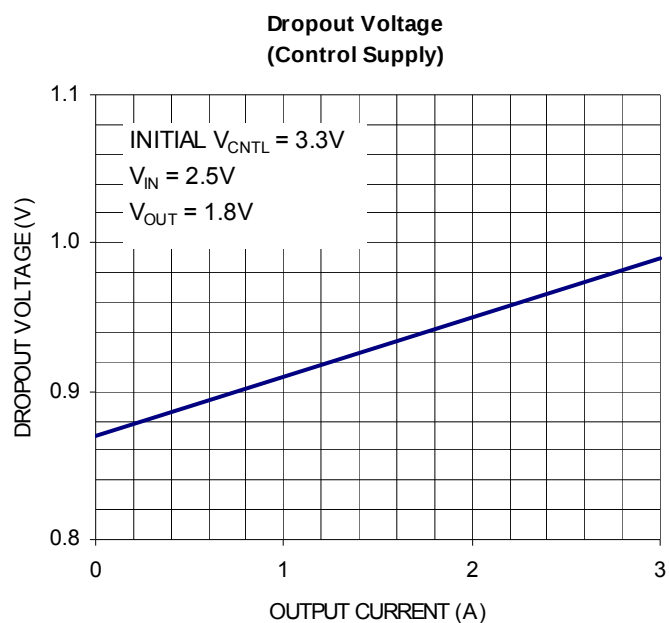
Input capacitor: A minimum of 10 μ F ceramic capacitor is recommended to be placed directly next to the Vin pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance may be added closely to the input supply pin of the SC1592 to ensure that Vin does not sag, improving load transient response.

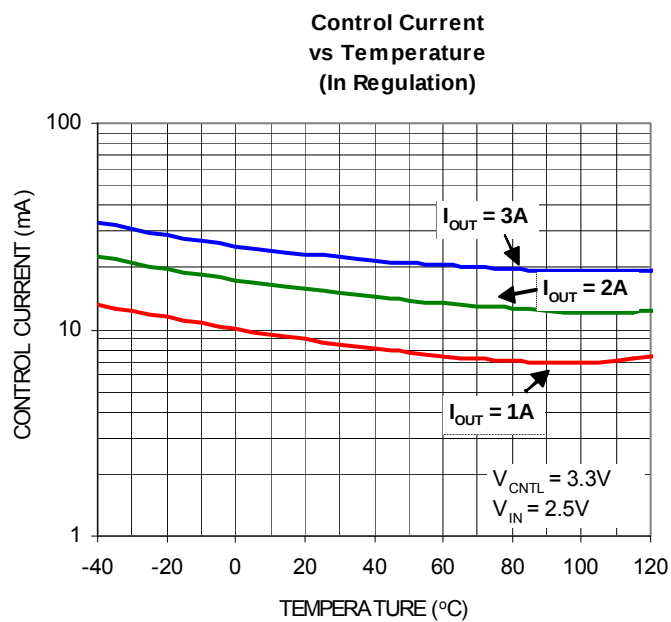
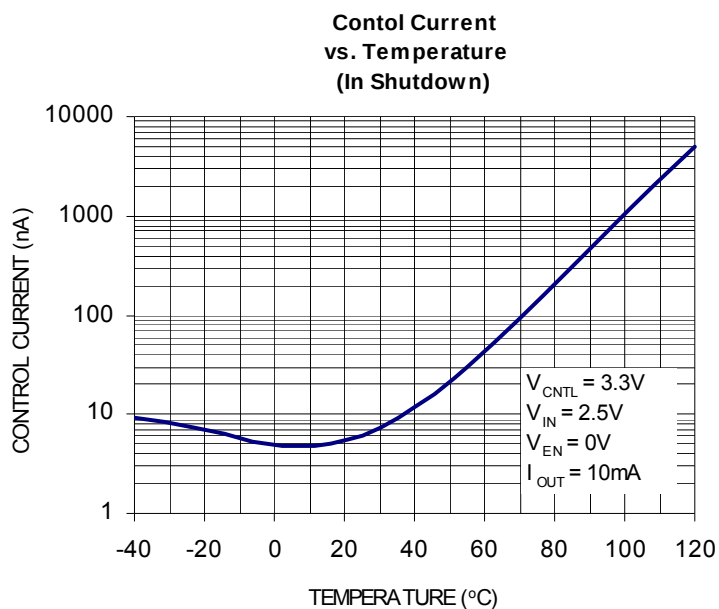
Output capacitor: A minimum bulk capacitance of 33 μ F, along with a 0.1 μ F ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the SC1592 is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

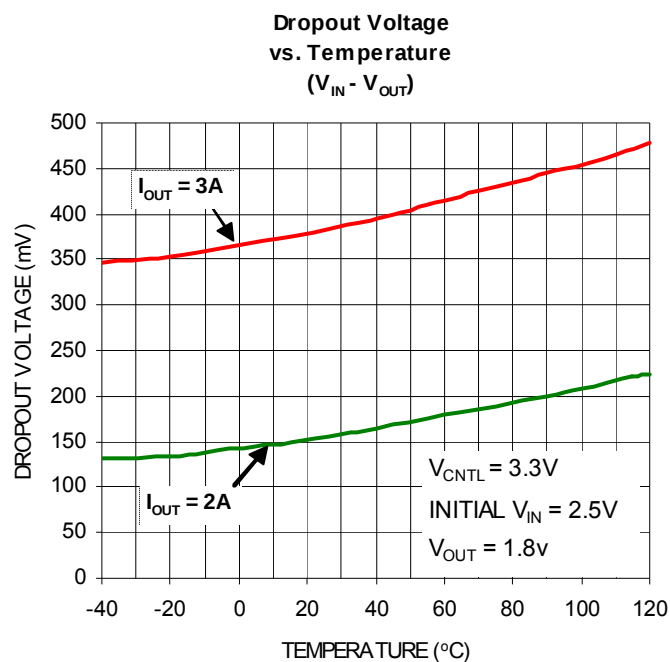
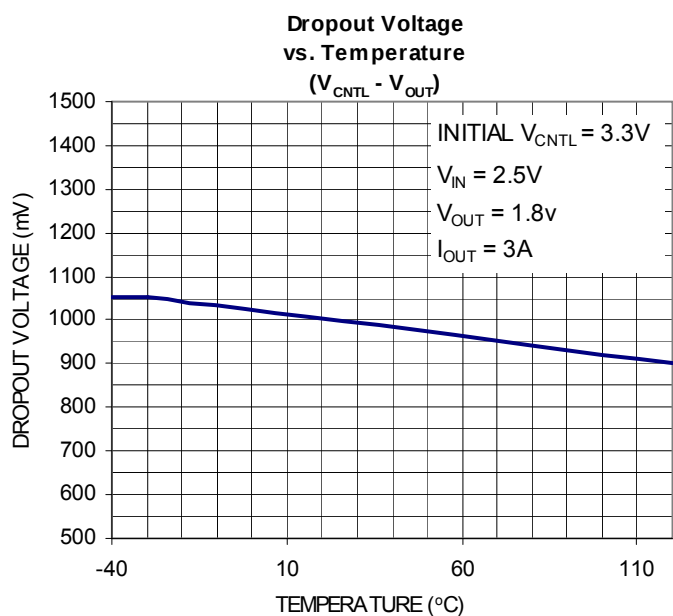
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Typical Characteristics
Load Transient Response


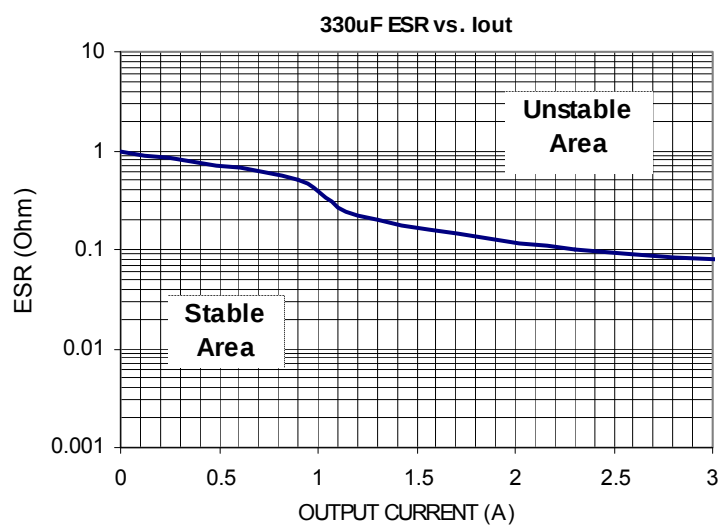
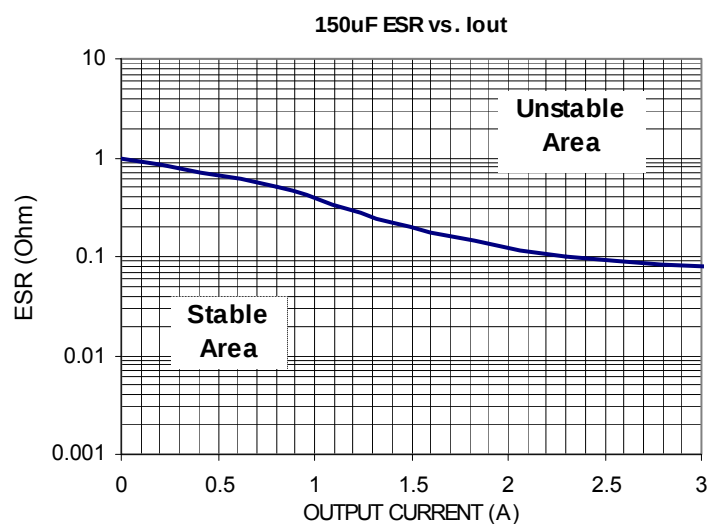
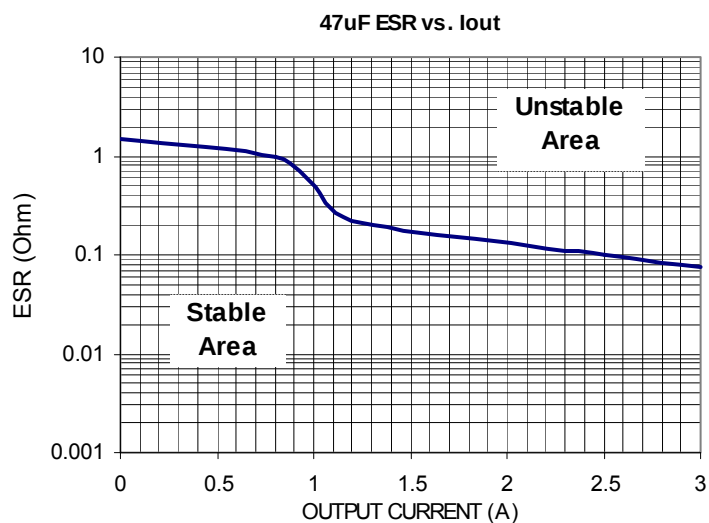
POWER MANAGEMENT
Typical Characteristics (Cont.)


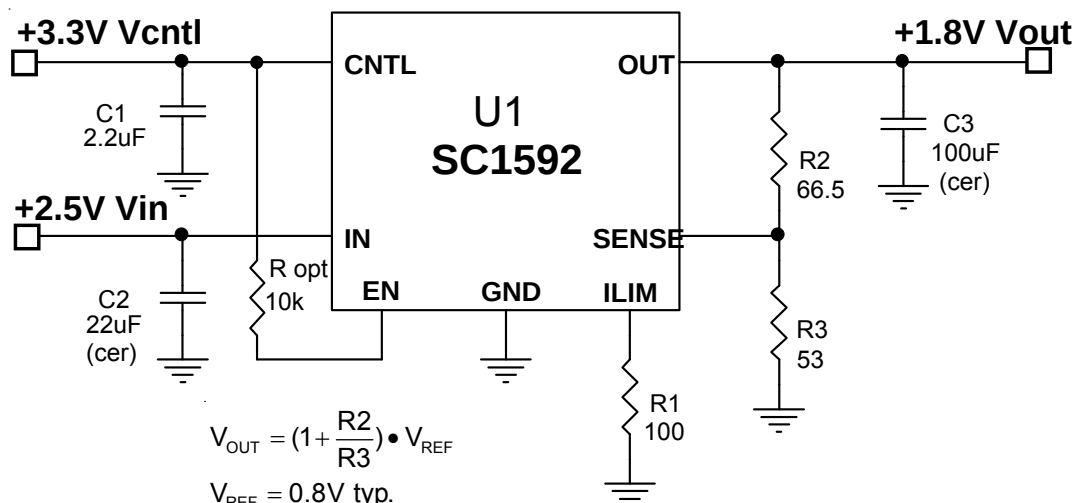
POWER MANAGEMENT**Typical Characteristics (Cont.)**

POWER MANAGEMENT
Typical Characteristics (Cont.)


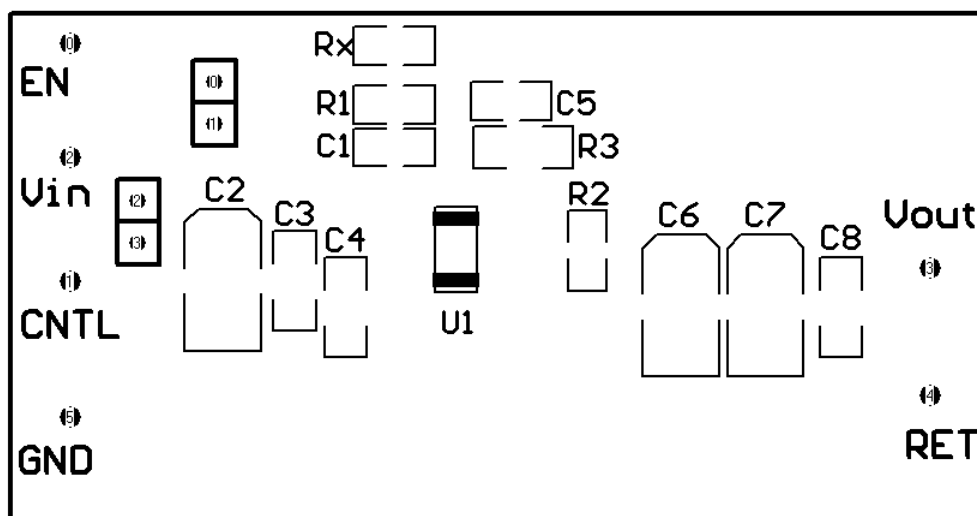
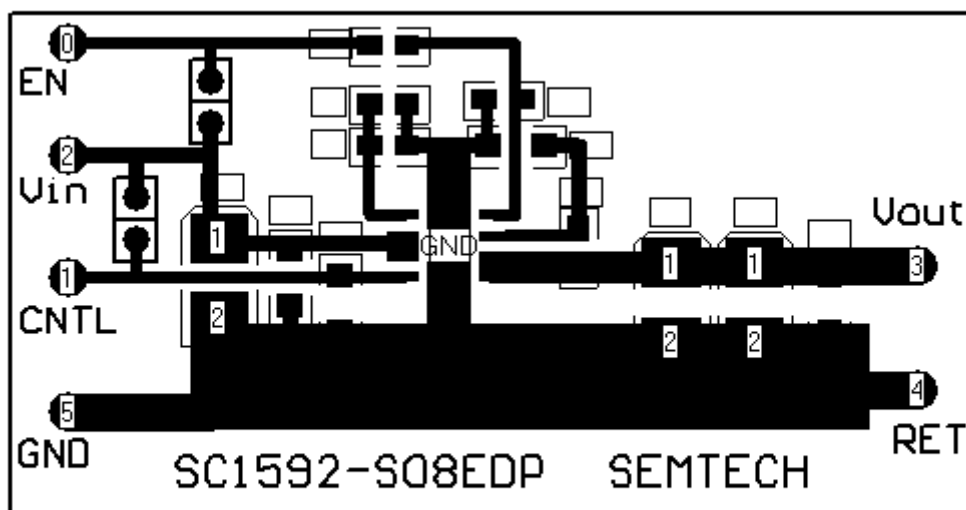
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Typical Characteristics (Cont.)


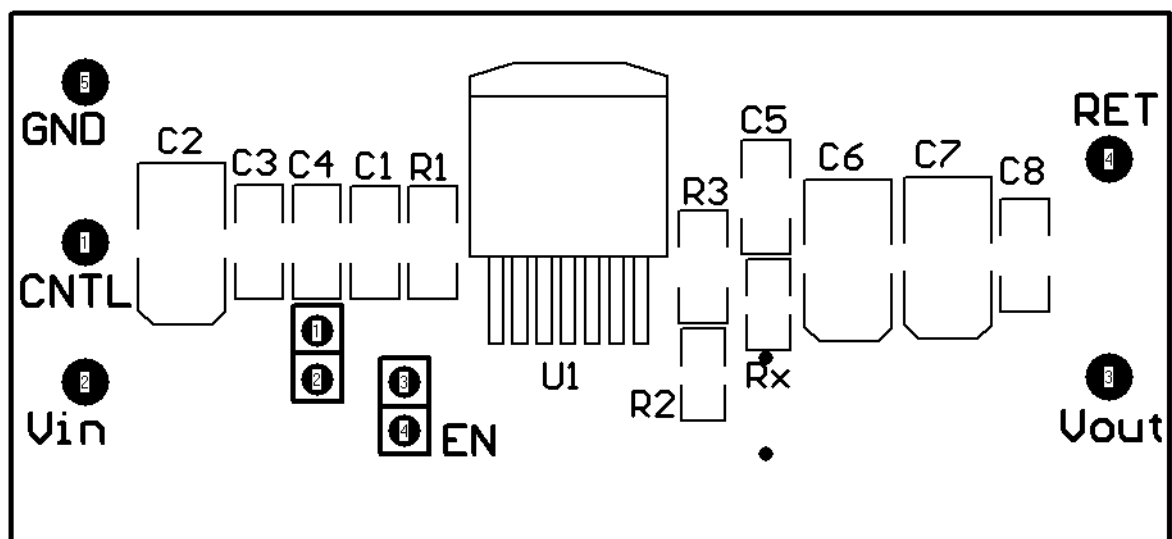
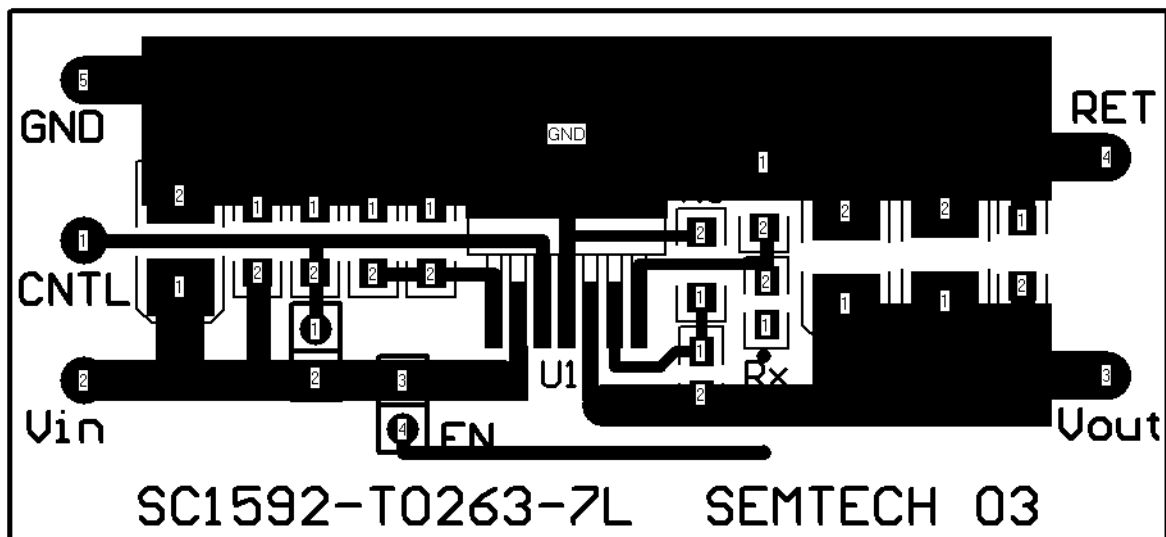
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Typical Characteristics (Cont.)


POWER MANAGEMENT
Typical Characteristics (Cont.)


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Evaluation Board Schematic

Evaluation Board Schematic - Bill of Material

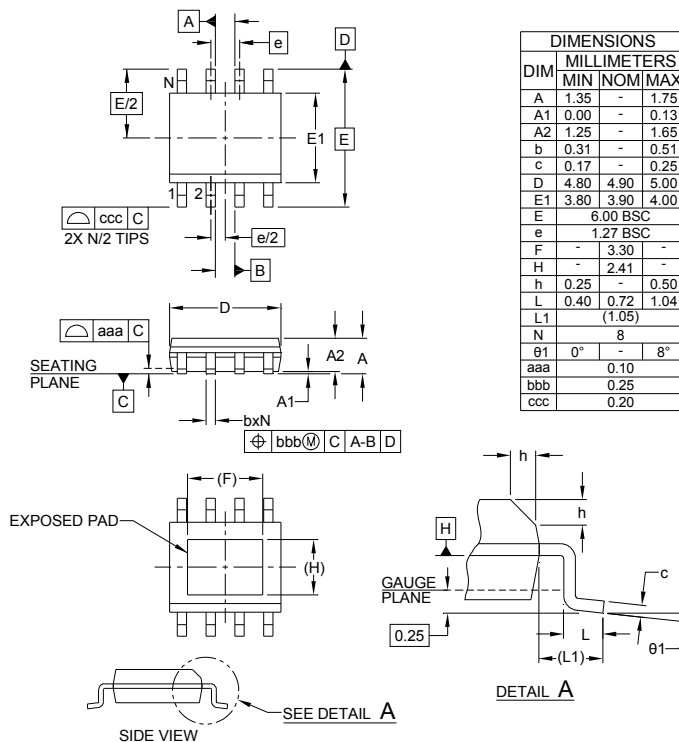
Ref	Qty	Reference	Part Number/Value	Manufacturer
1	1	C1	2.2uF, 16V, Ceramic, 1206	Murata or similar
2	1	C2	22uF, 10V, Ceramic, 1210	Murata or similar
3	1	C3	100uF, 6.3V, Ceramic, 1812	Murata or similar
4	1	R1	100, ±5%, 0805	Any
5	1	R2	66.5, ±0.5%, 0805	Any
6	1	R3	53, ±0.5%, 0805	Any
7	1	Ropt	10K, ±10%, 0805	Any
8	1	U1	SC1592	Semtech Corp.

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Evaluation Board - SOIC-8 EDP


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Evaluation Board - TO-263-7L (DDPAK)


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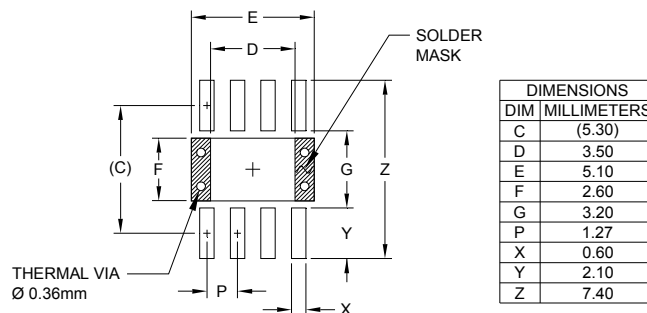
Outline Drawing - SOIC-8L EDP



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS $\boxed{-A-}$ AND $\boxed{-B-}$ TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$.
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE MEASUREMENT OF DIMENSION "F" DOES NOT INCLUDE EXPOSED TIE BAR.

Land Pattern - SOIC-8L EDP

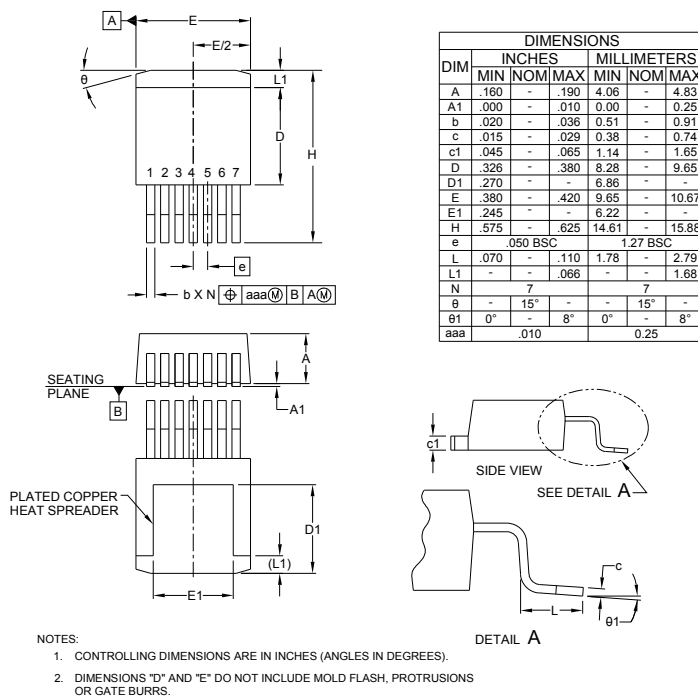


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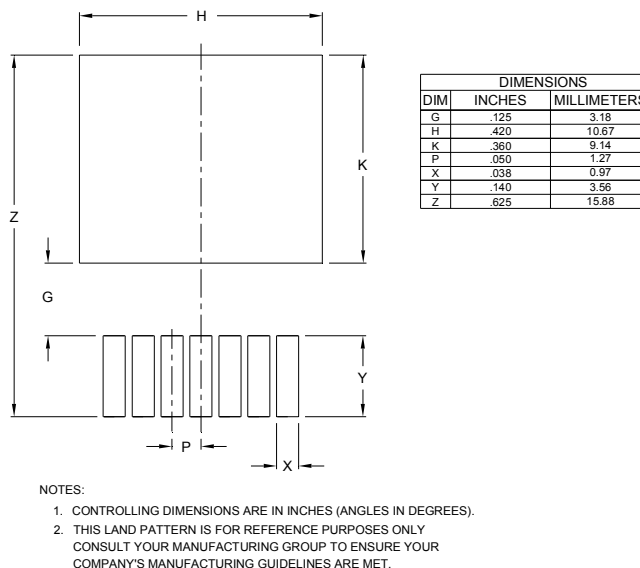
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSE ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. REFERENCE IPC-SM-782A, SECTION 9.1, RLP NO. 300A.

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Outline Drawing - TO-263-7L (DDPAK)



Recommended Land Pattern - TO-263-7L (DDPAK)



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