

(128+2) x RGB-Segment, 128-common 4096-Color STN LCD DRIVER

■ GENERAL DESCRIPTION

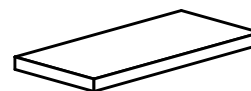
The **NJU6824** is a (128+2) x RGB segment, 128-common 4096-color STN LCD driver consisted of 384(128xRGB)-segment + 6(2xRGB)-icon segment and 128-common drivers, serial and parallel MPU interface circuits, internal power supply circuits, color palettes and 196,608-bit for graphic display data RAM.

Each of the 128-RGB segment drivers outputs 16 gradation levels out of 32-gradation level of color palette.

The display rotate function makes easily rotated display without original display data change.

Since the **NJU6824** provides a low operating voltage of 1.7V and low operating current, it is ideally suited for battery-powered handheld applications.

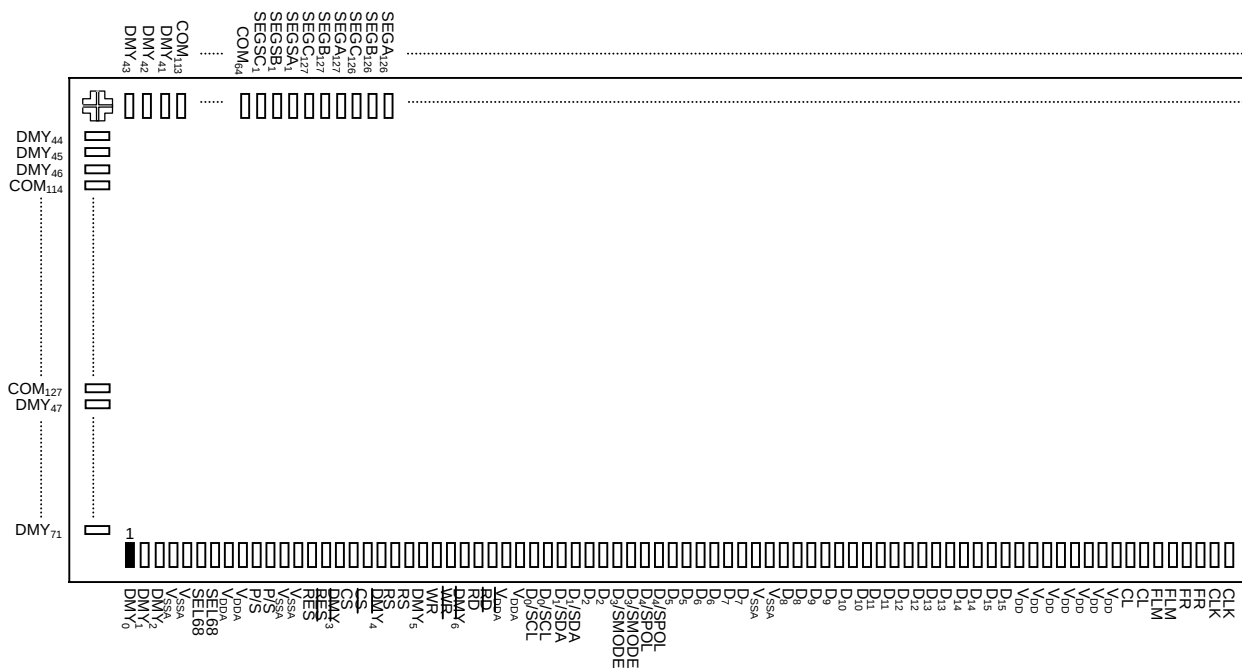
■ PACKAGE OUTLINE



NJU6824CJ

■ FEATURES

- 4096-color STN LCD driver
- LCD drivers 128 x 3(RGB) segments, 2 x 3(RGB) icon segments, 128 commons
- Display data RAM (DDRAM) 196,608-bit for graphic display
- Color display mode 16 gradation levels out of 32 gradation levels of color palette
- Black & white display mode 128 x 384 pixels 16 gradation levels or 128 x 384 pixels in B&W display
- 256-color driving mode
- 8/16bit Parallel interface direct connection to 68/80 series MPU
- Programmable 8- or 16-bit data bus length for display data
- Serial interface 3-/4-line
- Programmable duty and bias ratios
- Programmable internal voltage booster (6-times maximum)
- Programmable clock frequency for internal voltage booster operation (1/2, 1, 2, 4times)
- Programmable contrast control using 128-step EVR
- Display Rotate Function / Display Mirror Inverse Function
- Various instructions
 - Display data read/write, Display ON/OFF, Reverse display ON/OFF, All pixels ON/OFF, column address, row address, N-line inversion, Initial display line, Initial COM line, Read-modify-write, Gradation mode control, Increment control, Data bus length, Discharge ON/OFF, Duty cycle ratio, LCD bias ratio, Boost level, EVR control, Power save ON/OFF, etc
- Low operating current
- Low logic supply voltage 1.7V to 3.3V
- LCD driving supply voltage 5.0V to 18.0V
- C-MOS technology
- Package Bumped chip / TCP

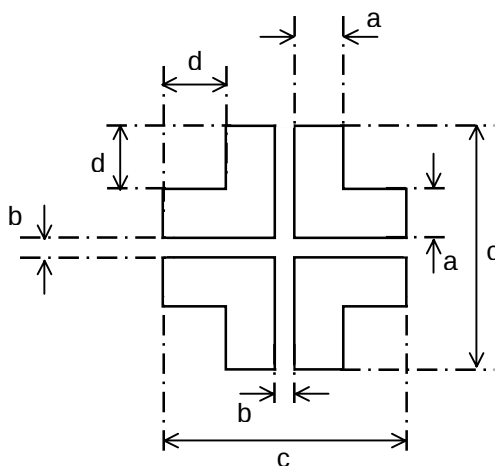


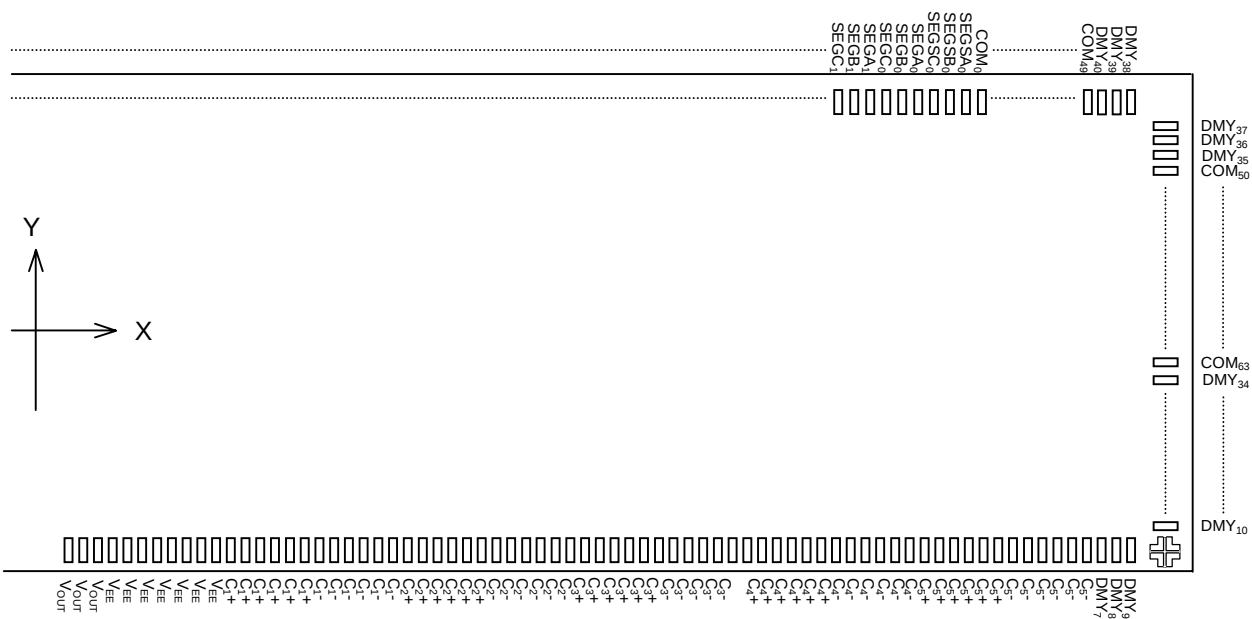
Note2) The DMY PADS are electrically open.

Chip Center	:X= 0μm, Y= 0μm
Chip Size	:22.07mm x 2.55mm
Chip Thickness	:625μm ± 25μm
Bump Size	:28μm x 110μm(COM/SEG Output, DMY ₁₀ ~ DMY ₇₁), 60μm x 100μm(Interface), 28μm x 100μm(DMY ₀ ~ DMY ₉)
Bump Pitch	:43μm(Min)
Bump Height	:14.0~22.5μm (Typical 18μm) <tolerance : ±3μm >
Bump Material	:Au

- a: $30\mu\text{m}$
b: $6\mu\text{m}$
c: $120\mu\text{m}$
d: $27\mu\text{m}$

X=-10866μm, Y= 1106μm
X= 10866μm, Y=-1106μm





■ PAD COORDINATES 1

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
1	DMY ₀	-10642.5	-1090.0	52	D ₁₀	-5584.5	-1090.0	103	V ₄ A ₂	-292.0	-1090.0
2	DMY ₁	-10599.5	-1090.0	53	D ₁₀	-5511.5	-1090.0	104	V _{SSA}	-182.5	-1090.0
3	DMY ₂	-10556.5	-1090.0	54	D ₁₁	-5365.5	-1090.0	105	V _{SSA}	-109.5	-1090.0
4	V _{SSA}	-10475.5	-1090.0	55	D ₁₁	-5292.5	-1090.0	106	V _{LCD}	0.0	-1090.0
5	V _{SSA}	-10402.5	-1090.0	56	D ₁₂	-5146.5	-1090.0	107	V _{LCD}	73.0	-1090.0
6	SEL68	-10293.0	-1090.0	57	D ₁₂	-5073.5	-1090.0	108	V _{LCD}	146.0	-1090.0
7	SEL68	-10220.0	-1090.0	58	D ₁₃	-4927.5	-1090.0	109	V _{LCD}	219.0	-1090.0
8	V _{DDA}	-10110.5	-1090.0	59	D ₁₃	-4854.5	-1090.0	110	V _{LCD}	292.0	-1090.0
9	V _{DDA}	-10037.5	-1090.0	60	D ₁₄	-4708.5	-1090.0	111	V _{LCD}	365.0	-1090.0
10	P/S	-9928.0	-1090.0	61	D ₁₄	-4635.5	-1090.0	112	V ₁	511.0	-1090.0
11	P/S	-9855.0	-1090.0	62	D ₁₅	-4489.5	-1090.0	113	V ₁	584.0	-1090.0
12	V _{SSA}	-9745.5	-1090.0	63	D ₁₅	-4416.5	-1090.0	114	V ₁	657.0	-1090.0
13	V _{SSA}	-9672.5	-1090.0	64	V _{DD}	-4197.5	-1090.0	115	V ₁	730.0	-1090.0
14	RES	-9563.0	-1090.0	65	V _{DD}	-4124.5	-1090.0	116	V ₁	803.0	-1090.0
15	RES	-9490.0	-1090.0	66	V _{DD}	-4051.5	-1090.0	117	V ₁	876.0	-1090.0
16	DMY ₃	-9380.5	-1090.0	67	V _{DD}	-3978.5	-1090.0	118	V ₂	1022.0	-1090.0
17	CS	-9271.0	-1090.0	68	V _{DD}	-3905.5	-1090.0	119	V ₂	1095.0	-1090.0
18	CS	-9198.0	-1090.0	69	V _{DD}	-3832.5	-1090.0	120	V ₂	1168.0	-1090.0
19	DMY ₄	-9088.5	-1090.0	70	V _{DD}	-3759.5	-1090.0	121	V ₂	1241.0	-1090.0
20	RS	-8979.0	-1090.0	71	CL	-3613.5	-1090.0	122	V ₂	1314.0	-1090.0
21	RS	-8906.0	-1090.0	72	CL	-3540.5	-1090.0	123	V ₂	1387.0	-1090.0
22	DMY ₅	-8796.5	-1090.0	73	FLM	-3394.5	-1090.0	124	V ₃	1533.0	-1090.0
23	WR	-8687.0	-1090.0	74	FLM	-3321.5	-1090.0	125	V ₃	1606.0	-1090.0
24	WR	-8614.0	-1090.0	75	FR	-3175.5	-1090.0	126	V ₃	1679.0	-1090.0
25	DMY ₆	-8504.5	-1090.0	76	FR	-3102.5	-1090.0	127	V ₃	1752.0	-1090.0
26	RD	-8395.0	-1090.0	77	CLK	-2956.5	-1090.0	128	V ₃	1825.0	-1090.0
27	RD	-8322.0	-1090.0	78	CLK	-2883.5	-1090.0	129	V ₃	1898.0	-1090.0
28	V _{DDA}	-8212.5	-1090.0	79	OSC ₁	-2701.0	-1090.0	130	V ₄	2044.0	-1090.0
29	V _{DDA}	-8139.5	-1090.0	80	OSC ₁	-2628.0	-1090.0	131	V ₄	2117.0	-1090.0
30	D ₀ /SCL	-7993.5	-1090.0	81	OSC ₂	-2409.0	-1090.0	132	V ₄	2190.0	-1090.0
31	D ₀ /SCL	-7920.5	-1090.0	82	OSC ₂	-2336.0	-1090.0	133	V ₄	2263.0	-1090.0
32	D ₁ /SDA	-7774.5	-1090.0	83	V _{SS}	-2044.0	-1090.0	134	V ₄	2336.0	-1090.0
33	D ₁ /SDA	-7701.5	-1090.0	84	V _{SS}	-1971.0	-1090.0	135	V ₄	2409.0	-1090.0
34	D ₂	-7555.5	-1090.0	85	V _{SS}	-1898.0	-1090.0	136	V _{REG}	2555.0	-1090.0
35	D ₂	-7482.5	-1090.0	86	V _{SS}	-1825.0	-1090.0	137	V _{REG}	2628.0	-1090.0
36	D ₃ /SMODE	-7336.5	-1090.0	87	V _{SS}	-1752.0	-1090.0	138	V _{REG}	2701.0	-1090.0
37	D ₃ /SMODE	-7263.5	-1090.0	88	V _{SS}	-1679.0	-1090.0	139	V _{REG}	2774.0	-1090.0
38	D ₄ /SPOL	-7117.5	-1090.0	89	V _{SS}	-1606.0	-1090.0	140	V _{REG}	2847.0	-1090.0
39	D ₄ /SPOL	-7044.5	-1090.0	90	V ₁ A ₁	-1460.0	-1090.0	141	V _{REG}	2920.0	-1090.0
40	D ₅	-6898.5	-1090.0	91	V ₁ A ₁	-1387.0	-1090.0	142	V _{REF}	3029.5	-1090.0
41	D ₅	-6825.5	-1090.0	92	V _{DDA}	-1277.5	-1090.0	143	V _{REF}	3102.5	-1090.0
42	D ₆	-6679.5	-1090.0	93	V _{DDA}	-1204.5	-1090.0	144	V _{REF}	3175.5	-1090.0
43	D ₆	-6606.5	-1090.0	94	V ₁ A ₂	-1095.0	-1090.0	145	V _{REF}	3248.5	-1090.0
44	D ₇	-6460.5	-1090.0	95	V ₁ A ₂	-1022.0	-1090.0	146	V _{REF}	3321.5	-1090.0
45	D ₇	-6387.5	-1090.0	96	V _{SSA}	-912.5	-1090.0	147	V _{REF}	3394.5	-1090.0
46	V _{SSA}	-6241.5	-1090.0	97	V _{SSA}	-839.5	-1090.0	148	V _{BA}	3504.0	-1090.0
47	V _{SSA}	-6168.5	-1090.0	98	V ₄ A ₁	-730.0	-1090.0	149	V _{BA}	3577.0	-1090.0
48	D ₈	-6022.5	-1090.0	99	V ₄ A ₁	-657.0	-1090.0	150	V _{BA}	3650.0	-1090.0
49	D ₈	-5949.5	-1090.0	100	V _{DDA}	-547.5	-1090.0	151	V _{BA}	3723.0	-1090.0
50	D ₉	-5803.5	-1090.0	101	V _{DDA}	-474.5	-1090.0	152	V _{BA}	3796.0	-1090.0
51	D ₉	-5730.5	-1090.0	102	V ₄ A ₂	-365.0	-1090.0	153	V _{BA}	3869.0	-1090.0

■ PAD COORDINATES 2

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
154	V _{SSH}	4051.5	-1090.0	205	C ₃₋	8212.5	-1090.0	256	DMY ₂₈	10845.0	-107.5
155	V _{SSH}	4124.5	-1090.0	206	C ₃₋	8285.5	-1090.0	257	DMY ₂₉	10845.0	-64.5
156	V _{SSH}	4197.5	-1090.0	207	C ₃₋	8358.5	-1090.0	258	DMY ₃₀	10845.0	-21.5
157	V _{SSH}	4270.5	-1090.0	208	C ₃₋	8431.5	-1090.0	259	DMY ₃₁	10845.0	21.5
158	V _{SSH}	4343.5	-1090.0	209	C ₃₋	8504.5	-1090.0	260	DMY ₃₂	10845.0	64.5
159	V _{SSH}	4416.5	-1090.0	210	C ₃₋	8577.5	-1090.0	261	DMY ₃₃	10845.0	107.5
160	V _{SSH}	4489.5	-1090.0	211	C ₄₊	8687.0	-1090.0	262	DMY ₃₄	10845.0	150.5
161	V _{OUT}	4672.0	-1090.0	212	C ₄₊	8760.0	-1090.0	263	COM ₆₃	10845.0	193.5
162	V _{OUT}	4745.0	-1090.0	213	C ₄₊	8833.0	-1090.0	264	COM ₆₂	10845.0	236.5
163	V _{OUT}	4818.0	-1090.0	214	C ₄₊	8906.0	-1090.0	265	COM ₆₁	10845.0	279.5
164	V _{OUT}	4891.0	-1090.0	215	C ₄₊	8979.0	-1090.0	266	COM ₆₀	10845.0	322.5
165	V _{OUT}	4964.0	-1090.0	216	C ₄₊	9052.0	-1090.0	267	COM ₅₉	10845.0	365.5
166	V _{OUT}	5037.0	-1090.0	217	C ₄₋	9161.5	-1090.0	268	COM ₅₈	10845.0	408.5
167	V _{OUT}	5110.0	-1090.0	218	C ₄₋	9234.5	-1090.0	269	COM ₅₇	10845.0	451.5
168	V _{EE}	5292.5	-1090.0	219	C ₄₋	9307.5	-1090.0	270	COM ₅₆	10845.0	494.5
169	V _{EE}	5365.5	-1090.0	220	C ₄₋	9380.5	-1090.0	271	COM ₅₅	10845.0	537.5
170	V _{EE}	5438.5	-1090.0	221	C ₄₋	9453.5	-1090.0	272	COM ₅₄	10845.0	580.5
171	V _{EE}	5511.5	-1090.0	222	C ₄₋	9526.5	-1090.0	273	COM ₅₃	10845.0	623.5
172	V _{EE}	5584.5	-1090.0	223	C ₅₊	9636.0	-1090.0	274	COM ₅₂	10845.0	666.5
173	V _{EE}	5657.5	-1090.0	224	C ₅₊	9709.0	-1090.0	275	COM ₅₁	10845.0	709.5
174	V _{EE}	5730.5	-1090.0	225	C ₅₊	9782.0	-1090.0	276	COM ₅₀	10845.0	752.5
175	C ₁₊	5840.0	-1090.0	226	C ₅₊	9855.0	-1090.0	277	DMY ₃₅	10845.0	795.5
176	C ₁₊	5913.0	-1090.0	227	C ₅₊	9928.0	-1090.0	278	DMY ₃₆	10845.0	838.5
177	C ₁₊	5986.0	-1090.0	228	C ₅₊	10001.0	-1090.0	279	DMY ₃₇	10845.0	881.5
178	C ₁₊	6059.0	-1090.0	229	C ₅₋	10110.5	-1090.0	280	DMY ₃₈	10642.5	1085.0
179	C ₁₊	6132.0	-1090.0	230	C ₅₋	10183.5	-1090.0	281	DMY ₃₉	10599.5	1085.0
180	C ₁₊	6205.0	-1090.0	231	C ₅₋	10256.5	-1090.0	282	DMY ₄₀	10556.5	1085.0
181	C ₁₋	6314.5	-1090.0	232	C ₅₋	10329.5	-1090.0	283	COM ₄₉	10513.5	1085.0
182	C ₁₋	6387.5	-1090.0	233	C ₅₋	10402.5	-1090.0	284	COM ₄₈	10470.5	1085.0
183	C ₁₋	6460.5	-1090.0	234	C ₅₋	10475.5	-1090.0	285	COM ₄₇	10427.5	1085.0
184	C ₁₋	6533.5	-1090.0	235	DMY ₇	10556.5	-1090.0	286	COM ₄₆	10384.5	1085.0
185	C ₁₋	6606.5	-1090.0	236	DMY ₈	10599.5	-1090.0	287	COM ₄₅	10341.5	1085.0
186	C ₁₋	6679.5	-1090.0	237	DMY ₉	10642.5	-1090.0	288	COM ₄₄	10298.5	1085.0
187	C ₂₊	6789.0	-1090.0	238	DMY ₁₀	10845.0	-881.5	289	COM ₄₃	10255.5	1085.0
188	C ₂₊	6862.0	-1090.0	239	DMY ₁₁	10845.0	-838.5	290	COM ₄₂	10212.5	1085.0
189	C ₂₊	6935.0	-1090.0	240	DMY ₁₂	10845.0	-795.5	291	COM ₄₁	10169.5	1085.0
190	C ₂₊	7008.0	-1090.0	241	DMY ₁₃	10845.0	-752.5	292	COM ₄₀	10126.5	1085.0
191	C ₂₊	7081.0	-1090.0	242	DMY ₁₄	10845.0	-709.5	293	COM ₃₉	10083.5	1085.0
192	C ₂₊	7154.0	-1090.0	243	DMY ₁₅	10845.0	-666.5	294	COM ₃₈	10040.5	1085.0
193	C ₂₋	7263.5	-1090.0	244	DMY ₁₆	10845.0	-623.5	295	COM ₃₇	9997.5	1085.0
194	C ₂₋	7336.5	-1090.0	245	DMY ₁₇	10845.0	-580.5	296	COM ₃₆	9954.5	1085.0
195	C ₂₋	7409.5	-1090.0	246	DMY ₁₈	10845.0	-537.5	297	COM ₃₅	9911.5	1085.0
196	C ₂₋	7482.5	-1090.0	247	DMY ₁₉	10845.0	-494.5	298	COM ₃₄	9868.5	1085.0
197	C ₂₋	7555.5	-1090.0	248	DMY ₂₀	10845.0	-451.5	299	COM ₃₃	9825.5	1085.0
198	C ₂₋	7628.5	-1090.0	249	DMY ₂₁	10845.0	-408.5	300	COM ₃₂	9782.5	1085.0
199	C ₃₊	7738.0	-1090.0	250	DMY ₂₂	10845.0	-365.5	301	COM ₃₁	9739.5	1085.0
200	C ₃₊	7811.0	-1090.0	251	DMY ₂₃	10845.0	-322.5	302	COM ₃₀	9696.5	1085.0
201	C ₃₊	7884.0	-1090.0	252	DMY ₂₄	10845.0	-279.5	303	COM ₂₉	9653.5	1085.0
202	C ₃₊	7957.0	-1090.0	253	DMY ₂₅	10845.0	-236.5	304	COM ₂₈	9610.5	1085.0
203	C ₃₊	8030.0	-1090.0	254	DMY ₂₆	10845.0	-193.5	305	COM ₂₇	9567.5	1085.0
204	C ₃₊	8103.0	-1090.0	255	DMY ₂₇	10845.0	-150.5	306	COM ₂₆	9524.5	1085.0

■ PAD COORDINATES 3

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
307	COM ₂₅	9481.5	1085.0	358	SEGB ₇	7288.5	1085.0	409	SEGB ₂₄	5095.5	1085.0
308	COM ₂₄	9438.5	1085.0	359	SEGC ₇	7245.5	1085.0	410	SEGC ₂₄	5052.5	1085.0
309	COM ₂₃	9395.5	1085.0	360	SEGA ₈	7202.5	1085.0	411	SEGA ₂₅	5009.5	1085.0
310	COM ₂₂	9352.5	1085.0	361	SEGB ₈	7159.5	1085.0	412	SEGB ₂₅	4966.5	1085.0
311	COM ₂₁	9309.5	1085.0	362	SEGC ₈	7116.5	1085.0	413	SEGC ₂₅	4923.5	1085.0
312	COM ₂₀	9266.5	1085.0	363	SEGA ₉	7073.5	1085.0	414	SEGA ₂₆	4880.5	1085.0
313	COM ₁₉	9223.5	1085.0	364	SEGB ₉	7030.5	1085.0	415	SEGB ₂₆	4837.5	1085.0
314	COM ₁₈	9180.5	1085.0	365	SEGC ₉	6987.5	1085.0	416	SEGC ₂₆	4794.5	1085.0
315	COM ₁₇	9137.5	1085.0	366	SEGA ₁₀	6944.5	1085.0	417	SEGA ₂₇	4751.5	1085.0
316	COM ₁₆	9094.5	1085.0	367	SEGB ₁₀	6901.5	1085.0	418	SEGB ₂₇	4708.5	1085.0
317	COM ₁₅	9051.5	1085.0	368	SEGC ₁₀	6858.5	1085.0	419	SEGC ₂₇	4665.5	1085.0
318	COM ₁₄	9008.5	1085.0	369	SEGA ₁₁	6815.5	1085.0	420	SEGA ₂₈	4622.5	1085.0
319	COM ₁₃	8965.5	1085.0	370	SEGB ₁₁	6772.5	1085.0	421	SEGB ₂₈	4579.5	1085.0
320	COM ₁₂	8922.5	1085.0	371	SEGC ₁₁	6729.5	1085.0	422	SEGC ₂₈	4536.5	1085.0
321	COM ₁₁	8879.5	1085.0	372	SEGA ₁₂	6686.5	1085.0	423	SEGA ₂₉	4493.5	1085.0
322	COM ₁₀	8836.5	1085.0	373	SEGB ₁₂	6643.5	1085.0	424	SEGB ₂₉	4450.5	1085.0
323	COM ₉	8793.5	1085.0	374	SEGC ₁₂	6600.5	1085.0	425	SEGC ₂₉	4407.5	1085.0
324	COM ₈	8750.5	1085.0	375	SEGA ₁₃	6557.5	1085.0	426	SEGA ₃₀	4364.5	1085.0
325	COM ₇	8707.5	1085.0	376	SEGB ₁₃	6514.5	1085.0	427	SEGB ₃₀	4321.5	1085.0
326	COM ₆	8664.5	1085.0	377	SEGC ₁₃	6471.5	1085.0	428	SEGC ₃₀	4278.5	1085.0
327	COM ₅	8621.5	1085.0	378	SEGA ₁₄	6428.5	1085.0	429	SEGA ₃₁	4235.5	1085.0
328	COM ₄	8578.5	1085.0	379	SEGB ₁₄	6385.5	1085.0	430	SEGB ₃₁	4192.5	1085.0
329	COM ₃	8535.5	1085.0	380	SEGC ₁₄	6342.5	1085.0	431	SEGC ₃₁	4149.5	1085.0
330	COM ₂	8492.5	1085.0	381	SEGA ₁₅	6299.5	1085.0	432	SEGA ₃₂	4106.5	1085.0
331	COM ₁	8449.5	1085.0	382	SEGB ₁₅	6256.5	1085.0	433	SEGB ₃₂	4063.5	1085.0
332	COM ₀	8406.5	1085.0	383	SEGC ₁₅	6213.5	1085.0	434	SEGC ₃₂	4020.5	1085.0
333	SEGA ₀	8363.5	1085.0	384	SEGA ₁₆	6170.5	1085.0	435	SEGA ₃₃	3977.5	1085.0
334	SEGSB ₀	8320.5	1085.0	385	SEGB ₁₆	6127.5	1085.0	436	SEGB ₃₃	3934.5	1085.0
335	SEGSC ₀	8277.5	1085.0	386	SEGC ₁₆	6084.5	1085.0	437	SEGC ₃₃	3891.5	1085.0
336	SEGA ₀	8234.5	1085.0	387	SEGA ₁₇	6041.5	1085.0	438	SEGA ₃₄	3848.5	1085.0
337	SEGB ₀	8191.5	1085.0	388	SEGB ₁₇	5998.5	1085.0	439	SEGB ₃₄	3805.5	1085.0
338	SEGC ₀	8148.5	1085.0	389	SEGC ₁₇	5955.5	1085.0	440	SEGC ₃₄	3762.5	1085.0
339	SEGA ₁	8105.5	1085.0	390	SEGA ₁₈	5912.5	1085.0	441	SEGA ₃₅	3719.5	1085.0
340	SEGB ₁	8062.5	1085.0	391	SEGB ₁₈	5869.5	1085.0	442	SEGB ₃₅	3676.5	1085.0
341	SEGC ₁	8019.5	1085.0	392	SEGC ₁₈	5826.5	1085.0	443	SEGC ₃₅	3633.5	1085.0
342	SEGA ₂	7976.5	1085.0	393	SEGA ₁₉	5783.5	1085.0	444	SEGA ₃₆	3590.5	1085.0
343	SEGB ₂	7933.5	1085.0	394	SEGB ₁₉	5740.5	1085.0	445	SEGB ₃₆	3547.5	1085.0
344	SEGC ₂	7890.5	1085.0	395	SEGC ₁₉	5697.5	1085.0	446	SEGC ₃₆	3504.5	1085.0
345	SEGA ₂	7847.5	1085.0	396	SEGA ₂₀	5654.5	1085.0	447	SEGA ₃₇	3461.5	1085.0
346	SEGB ₃	7804.5	1085.0	397	SEGB ₂₀	5611.5	1085.0	448	SEGB ₃₇	3418.5	1085.0
347	SEGC ₃	7761.5	1085.0	398	SEGC ₂₀	5568.5	1085.0	449	SEGC ₃₇	3375.5	1085.0
348	SEGA ₄	7718.5	1085.0	399	SEGA ₂₁	5525.5	1085.0	450	SEGA ₃₈	3332.5	1085.0
349	SEGB ₄	7675.5	1085.0	400	SEGB ₂₁	5482.5	1085.0	451	SEGB ₃₈	3289.5	1085.0
350	SEGC ₄	7632.5	1085.0	401	SEGC ₂₁	5439.5	1085.0	452	SEGC ₃₈	3246.5	1085.0
351	SEGA ₅	7589.5	1085.0	402	SEGA ₂₂	5396.5	1085.0	453	SEGA ₃₉	3203.5	1085.0
352	SEGB ₅	7546.5	1085.0	403	SEGB ₂₂	5353.5	1085.0	454	SEGB ₃₉	3160.5	1085.0
353	SEGC ₅	7503.5	1085.0	404	SEGC ₂₂	5310.5	1085.0	455	SEGC ₃₉	3117.5	1085.0
354	SEGA ₆	7460.5	1085.0	405	SEGA ₂₃	5267.5	1085.0	456	SEGA ₄₀	3074.5	1085.0
355	SEGB ₆	7417.5	1085.0	406	SEGB ₂₃	5224.5	1085.0	457	SEGB ₄₀	3031.5	1085.0
356	SEGC ₆	7374.5	1085.0	407	SEGC ₂₃	5181.5	1085.0	458	SEGC ₄₀	2988.5	1085.0
357	SEGA ₇	7331.5	1085.0	408	SEGA ₂₄	5138.5	1085.0	459	SEGA ₄₁	2945.5	1085.0

■ PAD COORDINATES 4

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
460	SEGB ₄₁	2902.5	1085.0	511	SEGB ₅₈	709.5	1085.0	562	SEGB ₇₅	-1483.5	1085.0
461	SEGC ₄₁	2859.5	1085.0	512	SEGC ₅₈	666.5	1085.0	563	SEGC ₇₅	-1526.5	1085.0
462	SEGA ₄₂	2816.5	1085.0	513	SEGA ₅₉	623.5	1085.0	564	SEGA ₇₆	-1569.5	1085.0
463	SEGB ₄₂	2773.5	1085.0	514	SEGB ₅₉	580.5	1085.0	565	SEGB ₇₆	-1612.5	1085.0
464	SEGC ₄₂	2730.5	1085.0	515	SEGC ₅₉	537.5	1085.0	566	SEGC ₇₆	-1655.5	1085.0
465	SEGA ₄₃	2687.5	1085.0	516	SEGA ₆₀	494.5	1085.0	567	SEGA ₇₇	-1698.5	1085.0
466	SEGB ₄₃	2644.5	1085.0	517	SEGB ₆₀	451.5	1085.0	568	SEGB ₇₇	-1741.5	1085.0
467	SEGC ₄₃	2601.5	1085.0	518	SEGC ₆₀	408.5	1085.0	569	SEGC ₇₇	-1784.5	1085.0
468	SEGA ₄₄	2558.5	1085.0	519	SEGA ₆₁	365.5	1085.0	570	SEGA ₇₈	-1827.5	1085.0
469	SEGB ₄₄	2515.5	1085.0	520	SEGB ₆₁	322.5	1085.0	571	SEGB ₇₈	-1870.5	1085.0
470	SEGC ₄₄	2472.5	1085.0	521	SEGC ₆₁	279.5	1085.0	572	SEGC ₇₈	-1913.5	1085.0
471	SEGA ₄₅	2429.5	1085.0	522	SEGA ₆₂	236.5	1085.0	573	SEGA ₇₉	-1956.5	1085.0
472	SEGB ₄₅	2386.5	1085.0	523	SEGB ₆₂	193.5	1085.0	574	SEGB ₇₉	-1999.5	1085.0
473	SEGC ₄₅	2343.5	1085.0	524	SEGC ₆₂	150.5	1085.0	575	SEGC ₇₉	-2042.5	1085.0
474	SEGA ₄₆	2300.5	1085.0	525	SEGA ₆₃	107.5	1085.0	576	SEGA ₈₀	-2085.5	1085.0
475	SEGB ₄₆	2257.5	1085.0	526	SEGB ₆₃	64.5	1085.0	577	SEGB ₈₀	-2128.5	1085.0
476	SEGC ₄₆	2214.5	1085.0	527	SEGC ₆₃	21.5	1085.0	578	SEGC ₈₀	-2171.5	1085.0
477	SEGA ₄₇	2171.5	1085.0	528	SEGA ₆₄	-21.5	1085.0	579	SEGA ₈₁	-2214.5	1085.0
478	SEGB ₄₇	2128.5	1085.0	529	SEGB ₆₄	-64.5	1085.0	580	SEGB ₈₁	-2257.5	1085.0
479	SEGC ₄₇	2085.5	1085.0	530	SEGC ₆₄	-107.5	1085.0	581	SEGC ₈₁	-2300.5	1085.0
480	SEGA ₄₈	2042.5	1085.0	531	SEGA ₆₅	-150.5	1085.0	582	SEGA ₈₂	-2343.5	1085.0
481	SEGB ₄₈	1999.5	1085.0	532	SEGB ₆₅	-193.5	1085.0	583	SEGB ₈₂	-2386.5	1085.0
482	SEGC ₄₈	1956.5	1085.0	533	SEGC ₆₅	-236.5	1085.0	584	SEGC ₈₂	-2429.5	1085.0
483	SEGA ₄₉	1913.5	1085.0	534	SEGA ₆₆	-279.5	1085.0	585	SEGA ₈₃	-2472.5	1085.0
484	SEGB ₄₉	1870.5	1085.0	535	SEGB ₆₆	-322.5	1085.0	586	SEGB ₈₃	-2515.5	1085.0
485	SEGC ₄₉	1827.5	1085.0	536	SEGC ₆₆	-365.5	1085.0	587	SEGC ₈₃	-2558.5	1085.0
486	SEGA ₅₀	1784.5	1085.0	537	SEGA ₆₇	-408.5	1085.0	588	SEGA ₈₄	-2601.5	1085.0
487	SEGB ₅₀	1741.5	1085.0	538	SEGB ₆₇	-451.5	1085.0	589	SEGB ₈₄	-2644.5	1085.0
488	SEGC ₅₀	1698.5	1085.0	539	SEGC ₆₇	-494.5	1085.0	590	SEGC ₈₄	-2687.5	1085.0
489	SEGA ₅₁	1655.5	1085.0	540	SEGA ₆₈	-537.5	1085.0	591	SEGA ₈₅	-2730.5	1085.0
490	SEGB ₅₁	1612.5	1085.0	541	SEGB ₆₈	-580.5	1085.0	592	SEGB ₈₅	-2773.5	1085.0
491	SEGC ₅₁	1569.5	1085.0	542	SEGC ₆₈	-623.5	1085.0	593	SEGC ₈₅	-2816.5	1085.0
492	SEGA ₅₂	1526.5	1085.0	543	SEGA ₆₉	-666.5	1085.0	594	SEGA ₈₆	-2859.5	1085.0
493	SEGB ₅₂	1483.5	1085.0	544	SEGB ₆₉	-709.5	1085.0	595	SEGB ₈₆	-2902.5	1085.0
494	SEGC ₅₂	1440.5	1085.0	545	SEGC ₆₉	-752.5	1085.0	596	SEGC ₈₆	-2945.5	1085.0
495	SEGA ₅₃	1397.5	1085.0	546	SEGA ₇₀	-795.5	1085.0	597	SEGA ₈₇	-2988.5	1085.0
496	SEGB ₅₃	1354.5	1085.0	547	SEGB ₇₀	-838.5	1085.0	598	SEGB ₈₇	-3031.5	1085.0
497	SEGC ₅₃	1311.5	1085.0	548	SEGC ₇₀	-881.5	1085.0	599	SEGC ₈₇	-3074.5	1085.0
498	SEGA ₅₄	1268.5	1085.0	549	SEGA ₇₁	-924.5	1085.0	600	SEGA ₈₈	-3117.5	1085.0
499	SEGB ₅₄	1225.5	1085.0	550	SEGB ₇₁	-967.5	1085.0	601	SEGB ₈₈	-3160.5	1085.0
500	SEGC ₅₄	1182.5	1085.0	551	SEGC ₇₁	-1010.5	1085.0	602	SEGC ₈₈	-3203.5	1085.0
501	SEGA ₅₅	1139.5	1085.0	552	SEGA ₇₂	-1053.5	1085.0	603	SEGA ₈₉	-3246.5	1085.0
502	SEGB ₅₅	1096.5	1085.0	553	SEGB ₇₂	-1096.5	1085.0	604	SEGB ₈₉	-3289.5	1085.0
503	SEGC ₅₅	1053.5	1085.0	554	SEGC ₇₂	-1139.5	1085.0	605	SEGC ₈₉	-3332.5	1085.0
504	SEGA ₅₆	1010.5	1085.0	555	SEGA ₇₃	-1182.5	1085.0	606	SEGA ₉₀	-3375.5	1085.0
505	SEGB ₅₆	967.5	1085.0	556	SEGB ₇₃	-1225.5	1085.0	607	SEGB ₉₀	-3418.5	1085.0
506	SEGC ₅₆	924.5	1085.0	557	SEGC ₇₃	-1268.5	1085.0	608	SEGC ₉₀	-3461.5	1085.0
507	SEGA ₅₇	881.5	1085.0	558	SEGA ₇₄	-1311.5	1085.0	609	SEGA ₉₁	-3504.5	1085.0
508	SEGB ₅₇	838.5	1085.0	559	SEGB ₇₄	-1354.5	1085.0	610	SEGB ₉₁	-3547.5	1085.0
509	SEGC ₅₇	795.5	1085.0	560	SEGC ₇₄	-1397.5	1085.0	611	SEGC ₉₁	-3590.5	1085.0
510	SEGA ₅₈	752.5	1085.0	561	SEGA ₇₅	-1440.5	1085.0	612	SEGA ₉₂	-3633.5	1085.0

■ PAD COORDINATES 5

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

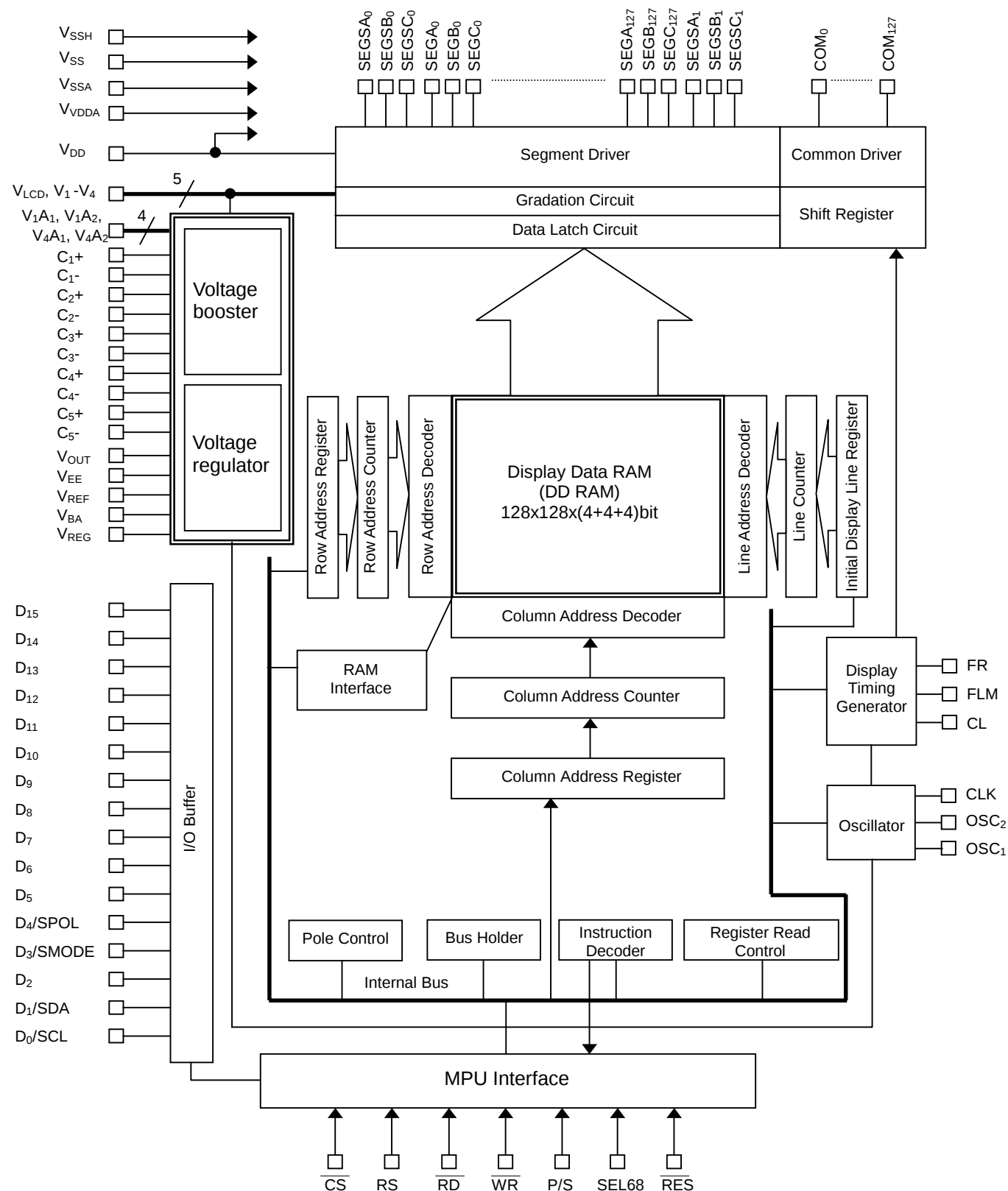
PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
613	SEGB ₉₂	-3676.5	1085.0	664	SEGB ₁₀₉	-5869.5	1085.0	715	SEGB ₁₂₆	-8062.5	1085.0
614	SEGC ₉₂	-3719.5	1085.0	665	SEGC ₁₀₉	-5912.5	1085.0	716	SEGC ₁₂₆	-8105.5	1085.0
615	SEGA ₉₃	-3762.5	1085.0	666	SEGA ₁₁₀	-5955.5	1085.0	717	SEGA ₁₂₇	-8148.5	1085.0
616	SEGB ₉₃	-3805.5	1085.0	667	SEGB ₁₁₀	-5998.5	1085.0	718	SEGB ₁₂₇	-8191.5	1085.0
617	SEGC ₉₃	-3848.5	1085.0	668	SEGC ₁₁₀	-6041.5	1085.0	719	SEGC ₁₂₇	-8234.5	1085.0
618	SEGA ₉₄	-3891.5	1085.0	669	SEGA ₁₁₁	-6084.5	1085.0	720	SEGSA ₁	-8277.5	1085.0
619	SEGB ₉₄	-3934.5	1085.0	670	SEGB ₁₁₁	-6127.5	1085.0	721	SEGSB ₁	-8320.5	1085.0
620	SEGC ₉₄	-3977.5	1085.0	671	SEGC ₁₁₁	-6170.5	1085.0	722	SEGSC ₁	-8363.5	1085.0
621	SEGA ₉₅	-4020.5	1085.0	672	SEGA ₁₁₂	-6213.5	1085.0	723	COM ₆₄	-8406.5	1085.0
622	SEGB ₉₅	-4063.5	1085.0	673	SEGB ₁₁₂	-6256.5	1085.0	724	COM ₆₅	-8449.5	1085.0
623	SEGC ₉₅	-4106.5	1085.0	674	SEGC ₁₁₂	-6299.5	1085.0	725	COM ₆₆	-8492.5	1085.0
624	SEGA ₉₆	-4149.5	1085.0	675	SEGA ₁₁₃	-6342.5	1085.0	726	COM ₆₇	-8535.5	1085.0
625	SEGB ₉₆	-4192.5	1085.0	676	SEGB ₁₁₃	-6385.5	1085.0	727	COM ₆₈	-8578.5	1085.0
626	SEGC ₉₆	-4235.5	1085.0	677	SEGC ₁₁₃	-6428.5	1085.0	728	COM ₆₉	-8621.5	1085.0
627	SEGA ₉₇	-4278.5	1085.0	678	SEGA ₁₁₄	-6471.5	1085.0	729	COM ₇₀	-8664.5	1085.0
628	SEGB ₉₇	-4321.5	1085.0	679	SEGB ₁₁₄	-6514.5	1085.0	730	COM ₇₁	-8707.5	1085.0
629	SEGC ₉₇	-4364.5	1085.0	680	SEGC ₁₁₄	-6557.5	1085.0	731	COM ₇₂	-8750.5	1085.0
630	SEGA ₉₈	-4407.5	1085.0	681	SEGA ₁₁₅	-6600.5	1085.0	732	COM ₇₃	-8793.5	1085.0
631	SEGB ₉₈	-4450.5	1085.0	682	SEGB ₁₁₅	-6643.5	1085.0	733	COM ₇₄	-8836.5	1085.0
632	SEGC ₉₈	-4493.5	1085.0	683	SEGC ₁₁₅	-6686.5	1085.0	734	COM ₇₅	-8879.5	1085.0
633	SEGA ₉₉	-4536.5	1085.0	684	SEGA ₁₁₆	-6729.5	1085.0	735	COM ₇₆	-8922.5	1085.0
634	SEGB ₉₉	-4579.5	1085.0	685	SEGB ₁₁₆	-6772.5	1085.0	736	COM ₇₇	-8965.5	1085.0
635	SEGC ₉₉	-4622.5	1085.0	686	SEGC ₁₁₆	-6815.5	1085.0	737	COM ₇₈	-9008.5	1085.0
636	SEGA ₁₀₀	-4665.5	1085.0	687	SEGA ₁₁₇	-6858.5	1085.0	738	COM ₇₉	-9051.5	1085.0
637	SEGB ₁₀₀	-4708.5	1085.0	688	SEGB ₁₁₇	-6901.5	1085.0	739	COM ₈₀	-9094.5	1085.0
638	SEGC ₁₀₀	-4751.5	1085.0	689	SEGC ₁₁₇	-6944.5	1085.0	740	COM ₈₁	-9137.5	1085.0
639	SEGA ₁₀₁	-4794.5	1085.0	690	SEGA ₁₁₈	-6987.5	1085.0	741	COM ₈₂	-9180.5	1085.0
640	SEGB ₁₀₁	-4837.5	1085.0	691	SEGB ₁₁₈	-7030.5	1085.0	742	COM ₈₃	-9223.5	1085.0
641	SEGC ₁₀₁	-4880.5	1085.0	692	SEGC ₁₁₈	-7073.5	1085.0	743	COM ₈₄	-9266.5	1085.0
642	SEGA ₁₀₂	-4923.5	1085.0	693	SEGA ₁₁₉	-7116.5	1085.0	744	COM ₈₅	-9309.5	1085.0
643	SEGB ₁₀₂	-4966.5	1085.0	694	SEGB ₁₁₉	-7159.5	1085.0	745	COM ₈₆	-9352.5	1085.0
644	SEGC ₁₀₂	-5009.5	1085.0	695	SEGC ₁₁₉	-7202.5	1085.0	746	COM ₈₇	-9395.5	1085.0
645	SEGA ₁₀₃	-5052.5	1085.0	696	SEGA ₁₂₀	-7245.5	1085.0	747	COM ₈₈	-9438.5	1085.0
646	SEGB ₁₀₃	-5095.5	1085.0	697	SEGB ₁₂₀	-7288.5	1085.0	748	COM ₈₉	-9481.5	1085.0
647	SEGC ₁₀₃	-5138.5	1085.0	698	SEGC ₁₂₀	-7331.5	1085.0	749	COM ₉₀	-9524.5	1085.0
648	SEGA ₁₀₄	-5181.5	1085.0	699	SEGA ₁₂₁	-7374.5	1085.0	750	COM ₉₁	-9567.5	1085.0
649	SEGB ₁₀₄	-5224.5	1085.0	700	SEGB ₁₂₁	-7417.5	1085.0	751	COM ₉₂	-9610.5	1085.0
650	SEGC ₁₀₄	-5267.5	1085.0	701	SEGC ₁₂₁	-7460.5	1085.0	752	COM ₉₃	-9653.5	1085.0
651	SEGA ₁₀₅	-5310.5	1085.0	702	SEGA ₁₂₂	-7503.5	1085.0	753	COM ₉₄	-9696.5	1085.0
652	SEGB ₁₀₅	-5353.5	1085.0	703	SEGB ₁₂₂	-7546.5	1085.0	754	COM ₉₅	-9739.5	1085.0
653	SEGC ₁₀₅	-5396.5	1085.0	704	SEGC ₁₂₂	-7589.5	1085.0	755	COM ₉₆	-9782.5	1085.0
654	SEGA ₁₀₆	-5439.5	1085.0	705	SEGA ₁₂₃	-7632.5	1085.0	756	COM ₉₇	-9825.5	1085.0
655	SEGB ₁₀₆	-5482.5	1085.0	706	SEGB ₁₂₃	-7675.5	1085.0	757	COM ₉₈	-9868.5	1085.0
656	SEGC ₁₀₆	-5525.5	1085.0	707	SEGC ₁₂₃	-7718.5	1085.0	758	COM ₉₉	-9911.5	1085.0
657	SEGA ₁₀₇	-5568.5	1085.0	708	SEGA ₁₂₄	-7761.5	1085.0	759	COM ₁₀₀	-9954.5	1085.0
658	SEGB ₁₀₇	-5611.5	1085.0	709	SEGB ₁₂₄	-7804.5	1085.0	760	COM ₁₀₁	-9997.5	1085.0
659	SEGC ₁₀₇	-5654.5	1085.0	710	SEGC ₁₂₄	-7847.5	1085.0	761	COM ₁₀₂	-10040.5	1085.0
660	SEGA ₁₀₈	-5697.5	1085.0	711	SEGA ₁₂₅	-7890.5	1085.0	762	COM ₁₀₃	-10083.5	1085.0
661	SEGB ₁₀₈	-5740.5	1085.0	712	SEGB ₁₂₅	-7933.5	1085.0	763	COM ₁₀₄	-10126.5	1085.0
662	SEGC ₁₀₈	-5783.5	1085.0	713	SEGC ₁₂₅	-7976.5	1085.0	764	COM ₁₀₅	-10169.5	1085.0
663	SEGA ₁₀₉	-5826.5	1085.0	714	SEGA ₁₂₆	-8019.5	1085.0	765	COM ₁₀₆	-10212.5	1085.0

■ PAD COORDINATES 6

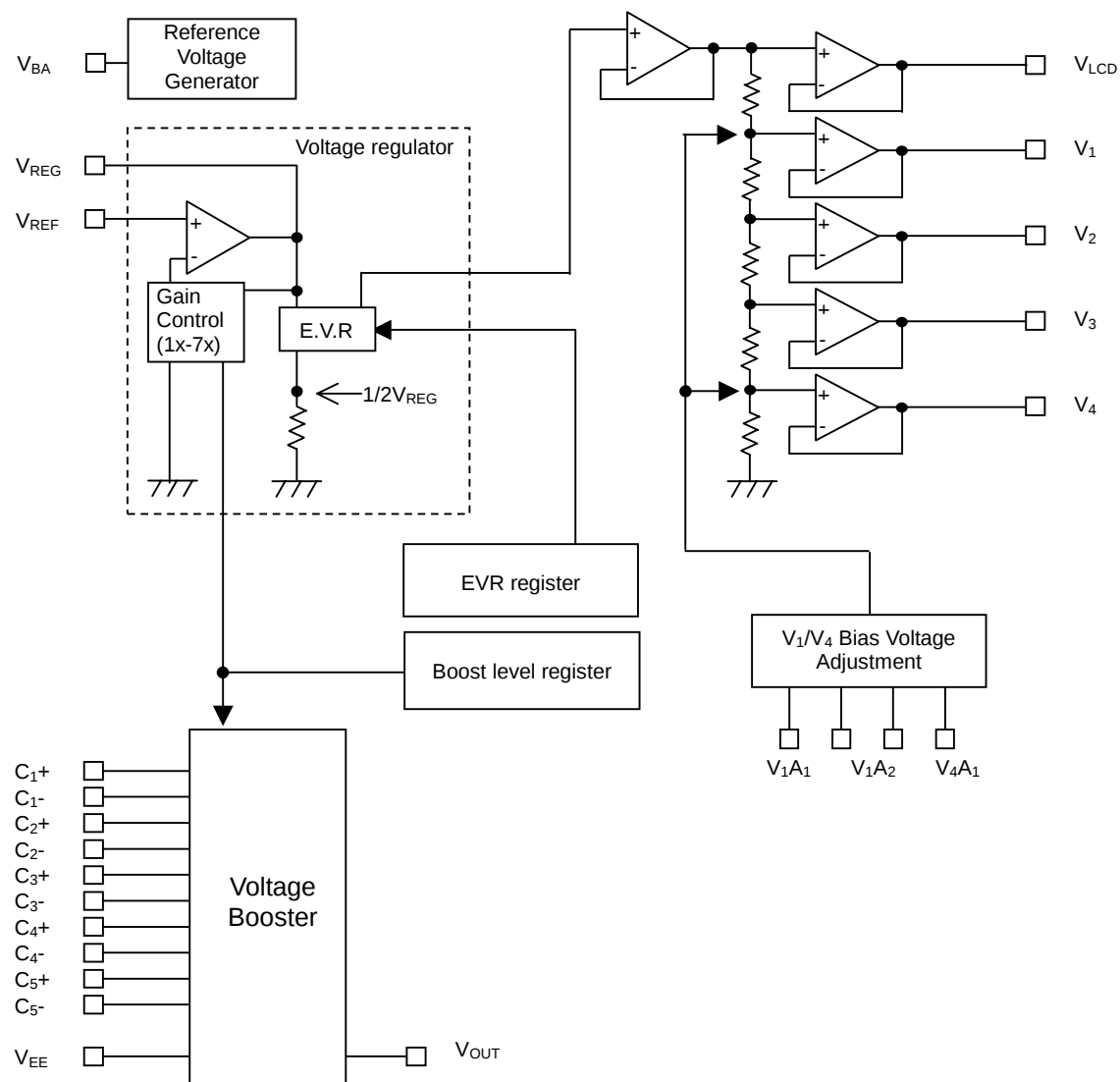
Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
766	COM ₁₀₇	-10255.5	1085.0	817	DMY ₇₁	-10845.0	-881.5				
767	COM ₁₀₈	-10298.5	1085.0								
768	COM ₁₀₉	-10341.5	1085.0								
769	COM ₁₁₀	-10384.5	1085.0								
770	COM ₁₁₁	-10427.5	1085.0								
771	COM ₁₁₂	-10470.5	1085.0								
772	COM ₁₁₃	-10513.5	1085.0								
773	DMY ₄₁	-10556.5	1085.0								
774	DMY ₄₂	-10599.5	1085.0								
775	DMY ₄₃	-10642.5	1085.0								
776	DMY ₄₄	-10845.0	881.5								
777	DMY ₄₅	-10845.0	838.5								
778	DMY ₄₆	-10845.0	795.5								
779	COM ₁₁₄	-10845.0	752.5								
780	COM ₁₁₅	-10845.0	709.5								
781	COM ₁₁₆	-10845.0	666.5								
782	COM ₁₁₇	-10845.0	623.5								
783	COM ₁₁₈	-10845.0	580.5								
784	COM ₁₁₉	-10845.0	537.5								
785	COM ₁₂₀	-10845.0	494.5								
786	COM ₁₂₁	-10845.0	451.5								
787	COM ₁₂₂	-10845.0	408.5								
788	COM ₁₂₃	-10845.0	365.5								
789	COM ₁₂₄	-10845.0	322.5								
790	COM ₁₂₅	-10845.0	279.5								
791	COM ₁₂₆	-10845.0	236.5								
792	COM ₁₂₇	-10845.0	193.5								
793	DMY ₄₇	-10845.0	150.5								
794	DMY ₄₈	-10845.0	107.5								
795	DMY ₄₉	-10845.0	64.5								
796	DMY ₅₀	-10845.0	21.5								
797	DMY ₅₁	-10845.0	-21.5								
798	DMY ₅₂	-10845.0	-64.5								
799	DMY ₅₃	-10845.0	-107.5								
800	DMY ₅₄	-10845.0	-150.5								
801	DMY ₅₅	-10845.0	-193.5								
802	DMY ₅₆	-10845.0	-236.5								
803	DMY ₅₇	-10845.0	-279.5								
804	DMY ₅₈	-10845.0	-322.5								
805	DMY ₅₉	-10845.0	-365.5								
806	DMY ₆₀	-10845.0	-408.5								
807	DMY ₆₁	-10845.0	-451.5								
808	DMY ₆₂	-10845.0	-494.5								
809	DMY ₆₃	-10845.0	-537.5								
810	DMY ₆₄	-10845.0	-580.5								
811	DMY ₆₅	-10845.0	-623.5								
812	DMY ₆₆	-10845.0	-666.5								
813	DMY ₆₇	-10845.0	-709.5								
814	DMY ₆₈	-10845.0	-752.5								
815	DMY ₆₉	-10845.0	-795.5								
816	DMY ₇₀	-10845.0	-838.5								

■ BLOCK DIAGRAM



■ POWER SUPPLY CIRCUITS BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Symbol	I/O	Function						
64~70	V _{DD}	Power	Power supply for logic circuits						
83~89	V _{SS}	Power	GND for logic circuits						
154~160	V _{SSH}	Power	GND for high voltage circuits						
8,9, 28,29, 92,93, 100,101	V _{DDA}	Power	This terminal is internally connected to the V _{DD} level. •This terminal is used to fix the select-terminals of the SEL68 and P/S to the V _{DD} level. Note) Do not use this terminal for a main power supply.						
4,5, 12,13, 46,47, 96,97, 104,105	V _{SSA}	Power	This terminal is internally connected to the V _{SS} level. •This terminal is used to fix the select-terminals of the SEL68 and P/S to the V _{SS} level. Note) Do not use this terminal for a main GND.						
106~111 112~117 118~123 124~129 130~135	V _{LCD} V ₁ V ₂ V ₃ V ₄	Power/O	LCD driving voltages •When the internal voltage booster is not used, external LCD driving voltages (V ₁ to V ₄ and V _{LCD}) should be supplied onto these terminals. The external voltages should be maintained with the following relationship. V _{SS} <V ₄ <V ₃ <V ₂ <V ₁ <V _{LCD} • When the internal voltage booster is used, the LCD driving voltages (V ₁ to V ₄ and V _{LCD}) are enabled by the “Power control” instruction. The capacitors between these terminals and Vss terminal must be connected.						
175~180 181~186	C ₁ + C ₁ -	O	Capacitor connection terminal for the voltage booster						
187~192 193~198	C ₂ + C ₂ -	O	Capacitor connection terminal for the voltage booster						
199~204 205~210	C ₃ + C ₃ -	O	Capacitor connection terminal for the voltage booster						
211~216 217~222	C ₄ + C ₄ -	O	Capacitor connection terminal for the voltage booster						
223~228 229~234	C ₅ + C ₅ -	O	Capacitor connection terminal for the voltage booster						
148~153	V _{BA}	O	Reference-voltage generator output						
142~147	V _{REF}	I	Voltage regulator input						
168~174	V _{EE}	Power	Voltage booster input •This terminal is normally connected to the V _{DD} level.						
161~167	V _{OUT}	Power/O	Voltage booster output for high voltage circuits (in external power supply)						
136~141	V _{REG}	O	Voltage regulator output						
90,91 94,95	V ₁ A ₁ V ₁ A ₂	I	V ₁ bias voltage adjustment terminal						
98,99 102,103	V ₄ A ₁ V ₄ A ₂	I	V ₄ bias voltage adjustment terminal						
14,15	RES	I	Reset Active “0”						
6,7	SEL68	I	MPU interface type select <table><tr><td>SEL86</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>68 series</td><td>80 series</td></tr></table>	SEL86	H	L	Status	68 series	80 series
SEL86	H	L							
Status	68 series	80 series							

■ TERMINAL DESCRIPTION 2

No.	Symbol	I/O	Function						
30,31	D ₀ /SCL	I/O	<u>Parallel interface:</u> D ₇ to D ₀ : 8-bit bi-directional bus •In the parallel interface mode (P/S="1"), these terminals should be connected to 8-bit bi-directional bus of MPU. <u>Serial interface:</u> SDA : serial data SCL : serial clock SMODE : 3-/4-line serial interface mode select SPOL : RS polarity select (in the 3-line serial interface mode) •In the 3-/4-line serial interface mode (P/S="0"), the D ₀ terminal is assigned to the SCL and the D ₁ terminal to the SDA. •In the 3-line serial interface mode, the D ₄ terminal is assigned to the SPOL. •The serial data on the SDA is fetched at the rising edge of the SCL signal in the order of the D ₇ , D ₆ ...D ₀ , and the fetched data is converted into 8-bit parallel data at the falling edge of the 8th SCL signal. •The SCL signal should be set to "0" after data transmissions or during non-access.						
32,33	D ₁ /SDA	I/O							
36,37	D ₃ /SMODE	I/O							
38,39	D ₄ /SPOL	I/O							
34,35 40,41 42,43 44,45	D ₂ D ₅ D ₆ D ₇	I/O							
48,49 50,51 52,53 54,55 56,57 58,59 60,61 62,63	D ₈ D ₉ D ₁₀ D ₁₁ D ₁₂ D ₁₃ D ₁₄ D ₁₅	I/O	8-bit bi-directional bus •In the 16-bit data bus mode, these terminals are assigned to the upper 8-bit data bus. •In the serial interface mode or 8-bit data bus mode in the parallel interface, these terminals should be fixed to "1" or "0".						
17,18	$\overline{\text{CS}}$	I	Chip select Active "0"						
20,21	RS	I	Resister select •This signal distinguishes an instruction data and display data for transferred data. <table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Distinct.</td><td>Instruction</td><td>Display data</td></tr></table>	RS	H	L	Distinct.	Instruction	Display data
RS	H	L							
Distinct.	Instruction	Display data							
26,27	$\overline{\text{RD}}$ (E)	I	<u>80 series MPU interface (P/S="1", SEL68="0")</u> RD signal. Active "0". <u>68 series MPU interface (P/S="1", SEL68="1")</u> Enable signal. Active "1".						
23,24	$\overline{\text{WR}}$ (R/W)	I	<u>80 series MPU interface (P/S="1", SEL68="0")</u> $\overline{\text{WR}}$ signal. Active "0". <u>68 series MPU interface (P/S="1", SEL68="1")</u> R/W signal. <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							

■ TERMINAL DESCRIPTION 3

No.	Symbol	I/O	Function																		
10,11	P/S	I	Parallel / serial interface mode select																		
			<table><tr><td>P/S</td><td>Chip Select</td><td>Data/ Instruction</td><td>Data</td><td>Read/Write</td><td>Serial clock</td></tr><tr><td>H</td><td>$\overline{\text{CS}}$</td><td>RS</td><td>D₀ ~ D₇</td><td>$\overline{\text{RD}}$, $\overline{\text{WR}}$</td><td>-</td></tr><tr><td>L</td><td>$\overline{\text{CS}}$</td><td>RS</td><td>SDA (D₁)</td><td>Write only</td><td>SCL (D₀)</td></tr></table>	P/S	Chip Select	Data/ Instruction	Data	Read/Write	Serial clock	H	$\overline{\text{CS}}$	RS	D ₀ ~ D ₇	$\overline{\text{RD}}$, $\overline{\text{WR}}$	-	L	$\overline{\text{CS}}$	RS	SDA (D ₁)	Write only	SCL (D ₀)
			P/S	Chip Select	Data/ Instruction	Data	Read/Write	Serial clock													
			H	$\overline{\text{CS}}$	RS	D ₀ ~ D ₇	$\overline{\text{RD}}$, $\overline{\text{WR}}$	-													
L	$\overline{\text{CS}}$	RS	SDA (D ₁)	Write only	SCL (D ₀)																
•In the serial interface mode (P/S="0"), the D ₁₅ to D ₅ and D ₂ terminals are in the high impedance status therefore those terminals should be fixed to "1" or "0". The RD and WR terminals also should be "1" or "0".																					
71,72	CL	O	This terminal should be opened.																		
73,74	FLM	O	This terminal should be opened.																		
75,76	FR	O	This terminal should be opened.																		
77,78	CLK	O	This terminal should be opened.																		
79,80 81,82	OSC ₁ OSC ₂	I O	OSC •When the internal oscillator clock is used, OSC ₁ terminal must be fixed to "1" or "0". OSC ₂ terminal should be opened. When the oscillation frequency from the internal oscillator is adjusted by an external resistor between OSC ₁ terminal and OSC ₂ •When an external oscillator is used, external clocks should be input onto the OSC ₁ terminal or an external resistor should be connected between the OSC ₁ and OSC ₂ terminals.																		

■ TERMINAL DESCRIPTION 4

No.	Symbol	I/O	Function															
336~719	SEGA ₀ ~ SEGA ₁₂₇ , SEGB ₀ ~ SEGB ₁₂₇ , SEGC ₀ ~ SEGC ₁₂₇	O	Segment output <table><tr><th>REF Mode</th><th>Turn-off</th><th>Turn-on</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table> •These terminals output LCD driving waveforms in accordance with the combination of FR signal and display data. In the B/W mode FR signal Display data Normal display mode Reverse display mode	REF Mode	Turn-off	Turn-on	Normal	0	1	Reverse	1	0						
REF Mode	Turn-off	Turn-on																
Normal	0	1																
Reverse	1	0																
333,720 334,721 335,722	SEGSA ₀ , SEGSA ₁ SEGSB ₀ , SEGSB ₁ SEGSC ₀ , SEGSC ₁	O	Icon segment output terminal •These terminals are assigned at both edge of normal segment output terminals line for out line frame display.															
332~283, 276~263, 723~772, 779~792	COM ₀ ~ COM ₁₂₇	O	Common output •These terminals output LCD driving waveforms in accordance with the combination of the FR signal and scanning data. <table><tr><th>Data</th><th>FR</th><th>Output level</th></tr><tr><td>H</td><td>H</td><td>V_{SS}</td></tr><tr><td>L</td><td>H</td><td>V₁</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V₄</td></tr></table>	Data	FR	Output level	H	H	V _{SS}	L	H	V ₁	H	L	V _{LCD}	L	L	V ₄
Data	FR	Output level																
H	H	V _{SS}																
L	H	V ₁																
H	L	V _{LCD}																
L	L	V ₄																

(Terminal No. 1~3,16,19,22,25,235~262,277~282,773~778,793~817 are dummy.)

■ Functional Description

(1) MPU Interface

(1-1) Parallel / serial interface mode select

The P/S terminal is used to select parallel or serial interface mode as shown in the following table. In the serial interface mode, it is impossible to read out display data from the DDRAM and status from the internal resistor.

Table1

P/S	P/S mode	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	SEL68	SDA	SCL	Data
H	Parallel I/F	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	SEL68			$D_7-D_0 (D_{15}-D_0)$
L	Serial I/F	$\overline{CS}$	RS	-	-	-	SDA	SCL	-

Note 1) “-” : Fix to “1” or “0”.

(1-2) MPU interface type select

In the parallel interface mode, the SEL68 terminal is used to select 68- or 80-series MPU interface type as shown in the following table.

Table2

SEL68	MPU type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	Data
H	68 series MPU	$\overline{CS}$	RS	E	R/W	$D_7-D_0 (D_{15}-D_0)$
L	80 series MPU	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	$D_7-D_0 (D_{15}-D_0)$

(1-3) Data distinction

In the parallel interface mode, the combination of RS, $\overline{RD}$, and $\overline{WR}$ (R/W) signals distinguishes an instruction data or display data for the transferred data from or to MPU as shown in the following table.

Table3

RS	68 series	80 series		Function
	R/W	$\overline{RD}$	$\overline{WR}$	
H	H	L	H	Read out instruction data
H	L	H	L	Write instruction data
L	H	L	H	Read out display data
L	L	H	L	Write display data

(1-4) 3- / 4-line serial interface mode select

In the serial interface mode, the SMODE is used to select 3- or 4-line serial interface mode as shown in the following table.

Table4

SMODE	Serial interface mode
H	3-line
L	4-line



(1-5) 4-line serial interface mode

In the 4-line serial interface mode, during the chip select is active ($\overline{CS}=“0”$), the SDA and SCL are enabled. During the chip select is not active ($\overline{CS}=“1”$), the SDA and SCL are disabled and the internal shift register and counter are being initialized. The 8-bit serial data on the SDA is fetched at the rising edge of the SCL signal (serial clock) in order of the $D_7, D_6 \dots D_0$, and the fetched data is converted into the 8-bit parallel data at the rising edge of the 8th SCL signal.

In the 4-line serial interface mode, the transferred data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS signal.

Table5

RS	Data distinction
H	Instruction data
L	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to “0” after data transmissions or during non-access. To prevent for the continuous mal-function caused by the external noises, the chip-selected status should be released ($\overline{CS}=“1”$) after each of the 8-bit data transmissions. The following figure illustrates the interface timing for the 4-line serial interface operation.

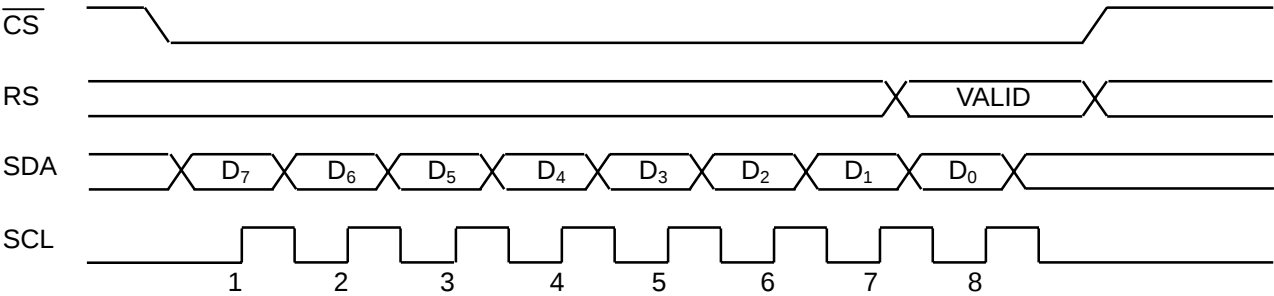


Fig1 4-line serial interface timing

(1-6) 3-line serial interface mode

In the 3-line serial interface mode, during the chip select is active ($\overline{CS}=“0”$), the SDA and SCL are enabled. During the chip select is not active ($\overline{CS}=“1”$), the SDA and SCL are disabled and the internal shift register and counter are being initialized. The 9-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the RS, $D_7, D_6 \dots D_0$, and the fetched data is converted into the 9-bit parallel data at the rising edge of the 9th SCL signal.

In the 3-line serial interface mode, the data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS bit of SDA data and the status of the SPOL, as follows.

Table6

SPOL=L		SPOL=H	
RS	Data distinction	RS	Data distinction
L	Display data	L	Instruction data
H	Instruction data	H	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to "0" after data transmissions or during non-access. To prevent for the continuous mal-function caused by the external noises, the chip-selected status should be released (CS="1") after each of the 9-bit data transmissions. The following figure illustrates the interface timing for the 3-line serial interface operation.

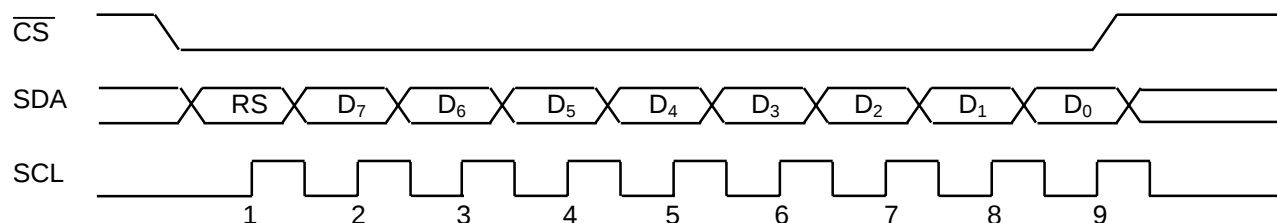


Fig2 3-line serial interface timing

(2) Access to the DDRAM

During the $\overline{CS}$ signal is "0", the transferred data is written into the DDRAM or instruction register in accordance with the condition of the RS signal.

In condition that the RS signal is "1", the transferred data is distinguished as display data. After the "column address" and "row address" instructions are executed, the display data is written into the DDRAM by the "display data write" instruction. The data is written at the rising edge of the $\overline{WR}$ signal in the 80 series MPU mode or falling edge of the E signal in the 68 series MPU mode.

Table6

RS	Data
L	Display RAM Data
H	Internal Command Register

In the sequence of the "display data read" operation, the transferred data from MPU is temporarily held in the internal bus-holder and then transferred to the internal data-bus. When the "display data read" operation is executed just after the "column address" and "row address" instructions or "display data write" instruction, unexpected data on the bus-holder is read out at the 1st execution and then the correct designated DDRAM address data is read out from the 2nd execution. For this reason, a dummy read cycle must be executed to avoid the unexpected 1st data read.

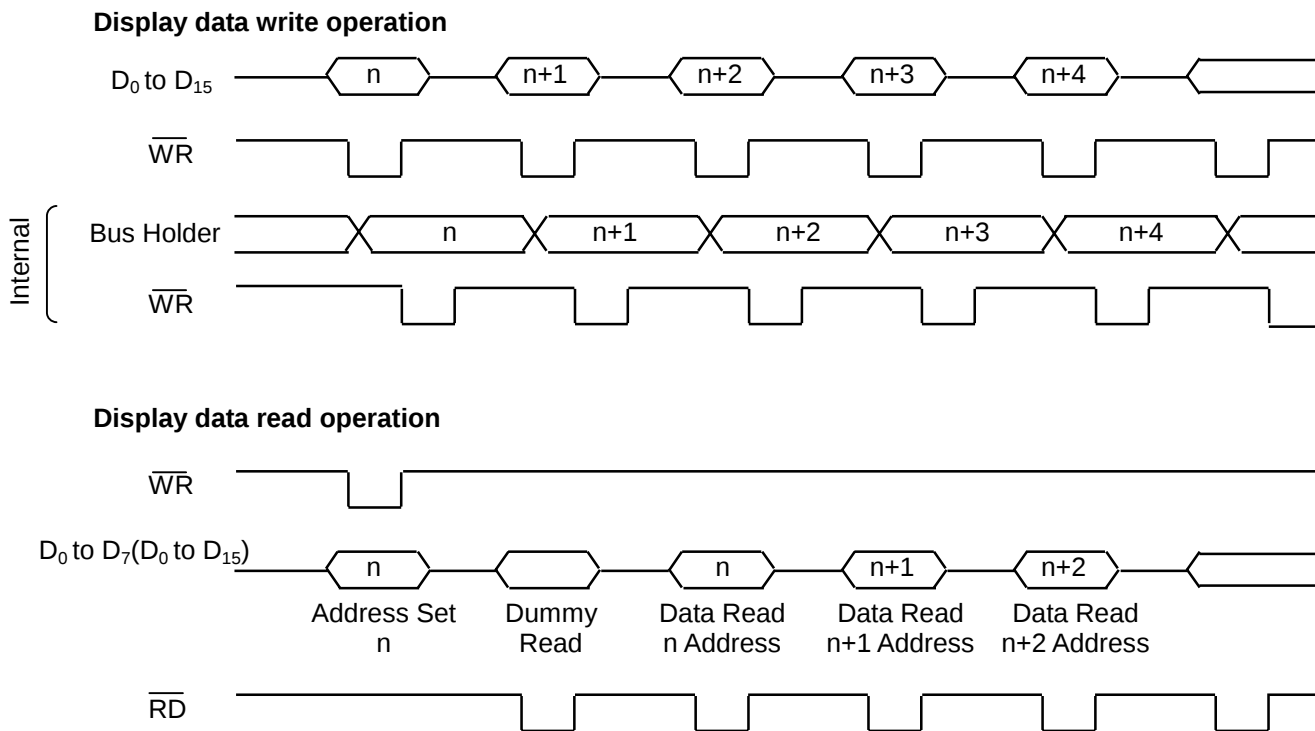


Fig3

Note) In 16-bit operation mode, command operation must set "Write" or "Read" with 16-bit data length as same as the access to RAM.

(3) Access to the instruction register

Each of the instruction registers is assigned to the address in between 0_H and F_H in order that it is possible to read out the content of the instruction registers by the combination instructions of the "Instruction register address" and "Instruction register read".

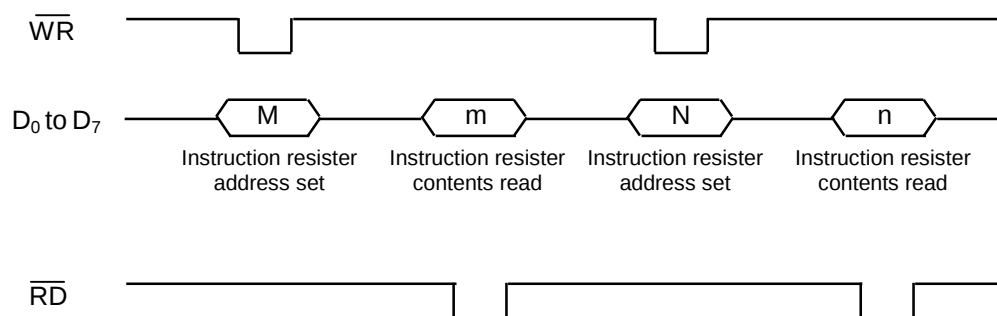


Fig4

(4) 8-/16-bit data bus length for display data (in the parallel interface mode)

The 8- or 16-bit data bus length for display data is determined by the "WLS" in the "Data bus length" instruction.

In the 16-bit data bus mode, not only the display data but also the instruction data is required to be transferred by 16-bit data (D_{15} to D_0). However, in case of the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. In case of the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

Table8

WLS	Data bus length mode
L	8-bit
H	16-bit

(5) Initial display line register

The initial display line register specifies the line address, corresponding to the initial COM line, by the "Initial display line" instruction. The initial COM line signifies the common driver, starting scanning the display data in the DDRAM, and specified by the "Initial COM line" instruction.

The line address, established in the initial display line register, is preset into the line counter whenever the FLM signal becomes "1". At the rising edge of the CL signal, the line counter is counted-up and addressed 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latched data output to the segment drivers.

(6) DDRAM mapping

The DDRAM is capable of 1,536-bit (12-bit x 128-segment) for the column address and 128-bit for the row address.

In the gradation mode, each pixel for RGB corresponds to the successive 3-segment drivers with 16-gradation per segment, so that the LSI can drive a 4096-color display (16-gradation x 16-gradation x 16-gradation) with up to 128x128 pixels.

In 8-bit access mode(C256 mode) for DDRAM, sequential twice accesses to DDRAM complete one pixel data access. Therefore, it must be accessed with a couple of operation.

- In the 8-bit data bus length mode

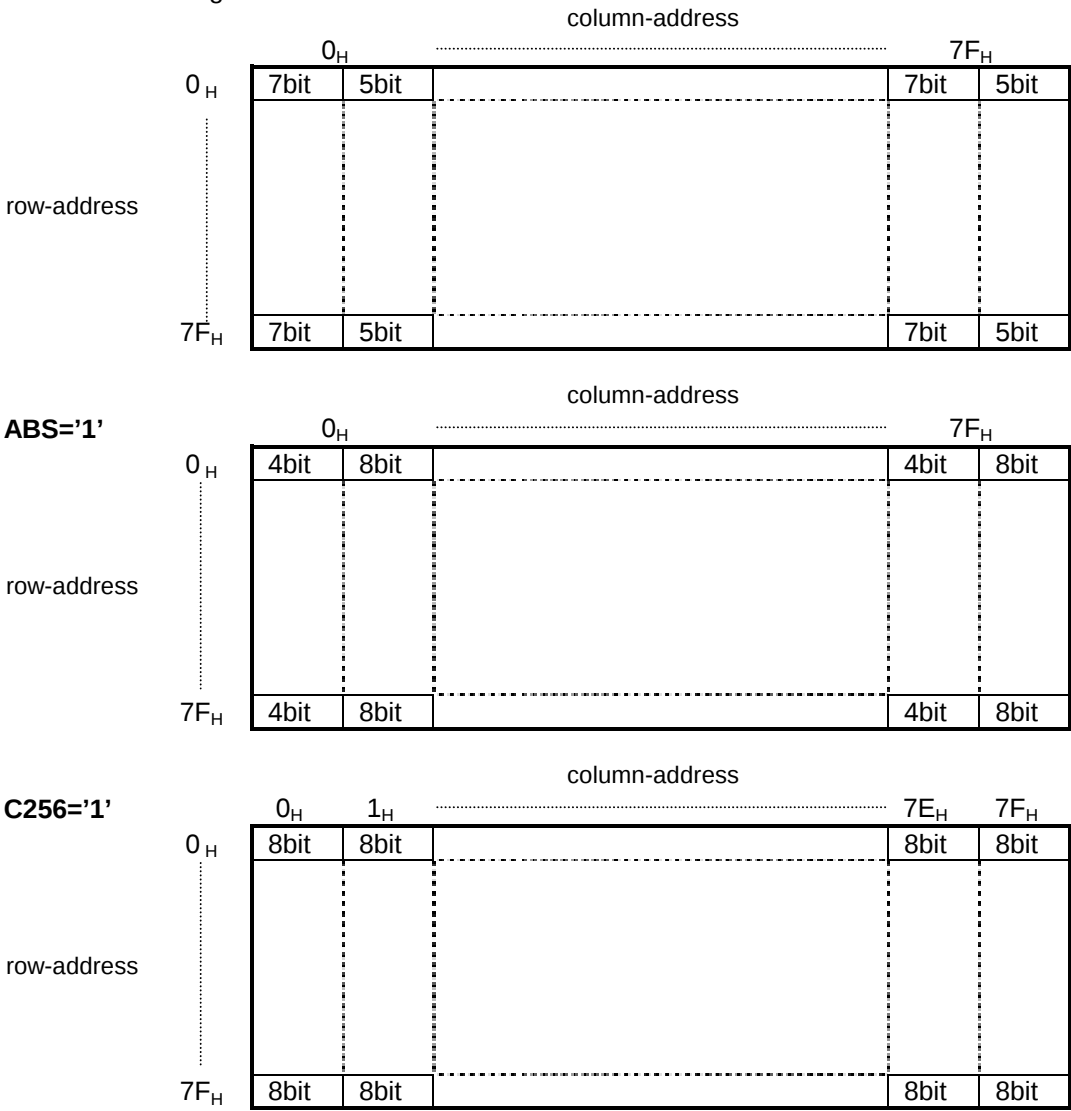


Fig5

- In the 16-bit data bus length mode

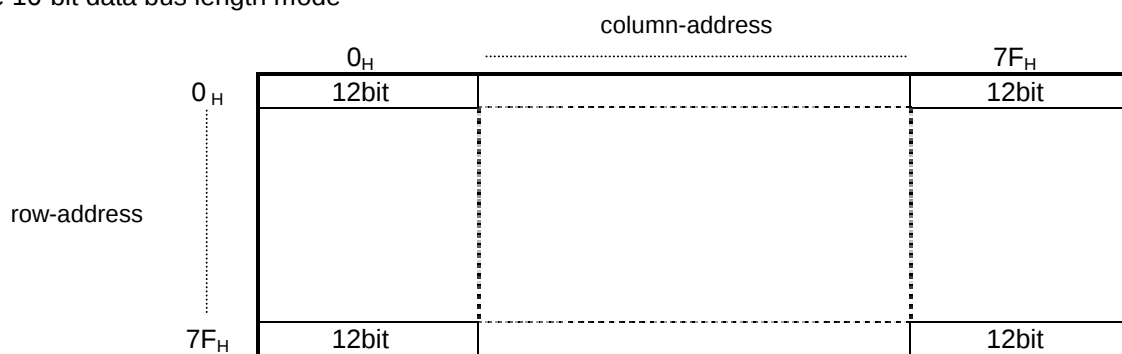


Fig6

In the B&W mode, only MSB data from each 4-bit display data group in the DDRAM is used. Therefore, 384 x 128 pixels B&W display or 128 x 128 pixels 8 kinds display is also available.

The column address range varies depending on the data bus length. The range between 00_H and 7F_H is used in the 8-bit or 16-bit data bus length.

The DDRAM is accessing 8-bit or 16-bit unit addressed by column and row address. In the 8-bit or 16-bit data bus length mode, over 80_H address setting is prohibited.

The increment for the column address and row address can be set in the auto-increment mode by programming "AXI" and "AYI" registers in the "Increment control" instruction. In this mode, the contents of the column address and row address counters automatically increment whenever the DDRAM is accessed.

The column address and row address counters are independent of the line counter. They are used to designate the column address and row address for the display data transferred from MPU. On the other hand, the line counter is used to generate the line address and output the display data to the segment drivers, being synchronized with the display control timing of the FLM and CL signals.

RAM Map 1

Mode	WLS	ABS	256	SEG0												SEG1												SEG126												SEG127																																																											
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C																																																															
				A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0																																																												
16bit	1	0	0	X=00H												X=01H												X=7EH												X=7FH																																																											
				D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0																																																
				X=00H												X=01H												X=7EH												X=7FH																																																											
8bit	0	0	0	X=00H (Upper)												X=00H (Lower)												X=01H (Upper)												X=01H (Lower)												X=7EH (Upper)												X=7EH (Lower)												X=7FH (Upper)												X=7FH (Lower)											
				D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0																																																
				X=00H (Upper)												X=00H (Lower)												X=01H (Upper)												X=01H (Lower)												X=7EH (Upper)												X=7EH (Lower)												X=7FH (Upper)												X=7FH (Lower)											
0	1	0	0	D3												D2												D1												D0												D3												D2												D1												D0											

RAM Map 2 (256 Color Mode)

Mode	WLS	ABS	256	SEG0									SEG1									SEG126									SEG127								
				Palette A			Palette B			Palette C			Palette A			Palette B			Palette C			Palette A			Palette B			Palette C			Palette A			Palette B			Palette C		
8bit	0	X	1	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
				X=00H									X=01H									X=7EH									X=7FH								
				D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-
				X=00H									X=01H									X=7EH									X=7FH								

SWAP

SWAP	Palette A				Palette B				Palette C			
	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
0	SEGAX				SEGBX				SEGCX			
1	SEGCX				SEGBX				SEGAX			

- Note1) In case of 256-color mode, the vacant LSB bit is filled by "1".
- Note2) 256-color mode is difference function with fixed 8-gradation mode (fixed 256-color mode).
- Note3) The written data into DD RAM in "C256"=0 in not used in "C256"=1.
- Note4) In case of 256-color mode, only 8-bit length mode is available and 16-bit is not used.
- Note5) In 8-bit access mode(C256 mode) for DDRAM, sequential twice accesses to DDRAM complete one pixel data access. Therefore, it must be accessed with a couple of operation.

Icon Segment Map 1

Mode	WLS	ABS	256	SEGS0												SEGS1																							
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C															
				A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0												
16bit	1	0	0	X=00H												X=01H																							
				D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0				
	1	1	0	X=00H												X=01H																							
8bit				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	X=00H (Upper)						X=00H (Lower)						X=01H (Upper)						X=01H (Lower)																	
	0	1	0	X=00H (Upper)						X=00H (Lower)						X=01H (Upper)						X=01H (Lower)																	
				D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

Icon Segment Map 2 (256 Color Mode)

Mode	WLS	ABS	256	SEGS0												SEGS1											
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
				X=00H												X=01H											
				D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
				X=00H												X=01H											
8bit	0	X	1	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0

SWAP

SWAP	Palette A				Palette B				Palette C			
	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
0	SEGSAX				SEGSBX				SEGSX			
1	SEGSX				SEGSBX				SEGSAX			

Note1) In case of 256-color mode, the vacant LSB bit is filled by "1".
Note2) 256-color mode is difference function with fixed 8-gradation mode (fixed 256-color mode).
Note3) The written data into DD RAM in "C256"=0 in not used in "C256"=1.
Note4) In case of 256-color mode, only 8-bit length mode is available and 16-bit is not used.
Note5) In 8-bit access mode(C256 mode) for DDRAM, sequential twice accesses to DDRAM complete one pixel data access. Therefore, it must be accessed with a couple of operation.

(7) Window addressing mode

Window area must be designated before RAM access.

In the window addressing mode, the address space of the DDRAM designated by the start and end point is defined. The start point is determined by the "column address" and "row address" instructions, and the end point is determined by the "Window end column address" and "Window end row address" instructions. The setting for the window addressing is listed in the following.

1. "Increment control" instruction set (HV, XD, YD)
2. Set "column address" and "row address" instructions for the start point
3. Set "Window end column address" and "Window end row address" instructions for the end point
4. Enable to access to the DDRAM by the window addressing mode

In addition, the read-modify-write operation is available by setting "AIM" register to "L" in the "Increment control" instruction.

For the window area designation, the address directions of RAM (HV, XD, YD) must be set first, and Column address and Row of Start point must be set second, Column address and Row of Stop point must be set third, then RAM should be accessed. Low address must be set first and High address must be set second in all of addresses. The directions of HV, XD, YD should be check to keep the area in RAM.

Also in the window addressing mode, correct start and end point setting is required to abide to access invalid addressing space.

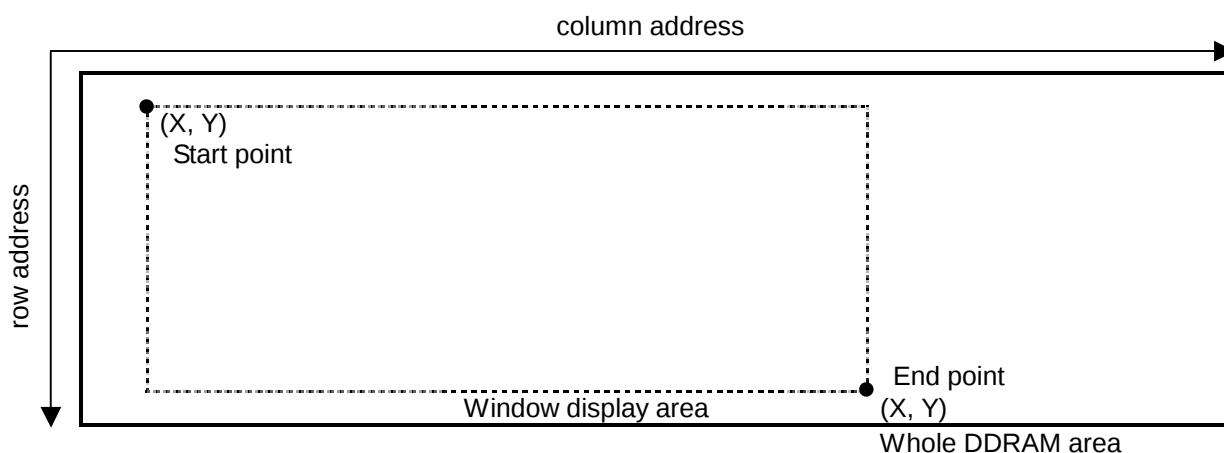


Fig7

(8) Reverse display ON/OFF

The "Reverse display ON/OFF" function is used to reverse the display data without changing the display data in the DDRAM.

Table9

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(9) Address directions of RAM access (Display rotation)

The bellow picture shows display image after set of HV, XD and YD for address directions. The display data from CPU can be written into RAM with rotation to 90 degrees or 180 degrees or 270 degrees, and also mirrored.

The address directions of RAM access is set by HV, XD and YD.

* : The segments of Icon are not rotated.

No.	HV	XD	YD	Data writing direction	Display image	Valid address
1	0	0	0			$Xs < Xe$ $Ys < Ye$
2	0	0	1			$Xs < Xe$ $Ys > Ye$
3	0	1	0			$Xs > Xe$ $Ys < Ye$
4	0	1	1			$Xs > Xe$ $Ys > Ye$
5	1	0	0			$Xs < Xe$ $Ys < Ye$
6	1	0	1			$Xs < Xe$ $Ys > Ye$
7	1	1	0			$Xs > Xe$ $Ys < Ye$
8	1	1	1			$Xs > Xe$ $Ys > Ye$

*:The display image shows the display direction when the same data as No.1 are written into RAM for condition change.

*: The outside address of RAM must not be set for correct operation.

Xs : start address of X , Ys : Start address of Y, Xe : End address of X, Ye : End address of Y

(10) The relationship among the DDRAM column address, display data and segment drivers

Color mode, 16-bit data bus mode

ABS	SWAP	X address / bit / segment assign																								
0	0	X=00 _H												↔	X=7F _H											
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				↕↕	palette A				palette B				palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↕↕	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	X address / bit / segment assign																								
0	1	X=00 _H												↔	X=7F _H											
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				↕	palette A				palette B				palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↕	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

ABS	SWAP	X address / bit / segment assign																								
1	0	X=00 _H												↔	X=7F _H											
		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↑ ↓	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A				palette B				palette C				↑ ↓	palette A				palette B				palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↑ ↓	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	X address / bit / segment assign																								
1	1	X=00 _H												↔	X=7F _H											
		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↑ ↓	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A				palette B				palette C				↑ ↓	palette A				palette B				palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↑ ↓	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

Color mode, 8-bit data bus mode

ABS	SWAP	X address / bit / segment assign																								
0	0	X=00 _H (Upper)					X=00 _H (Lower)					↔	X=7F _H (Upper)					X=7F _H (Lower)								
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				↕	palette A				palette B				palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↕	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	X address / bit / segment assign																								
0	1	X=00 _H (Upper)							X=00 _H (Lower)					↔	X=7F _H (Upper)							X=7F _H (Lower)				
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				↕	palette A				palette B				palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↕	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

ABS	SWAP	X address / bit / segment assign																											
1	0	X=00 _H (Upper)				X=00 _H (Lower)								↔		X=7F _H (Upper)				X=7F _H (Lower)									
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
		palette A				palette B				palette C				↕		↕		palette A				palette B				palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↕		↕		SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	X address / bit / segment assign																											
1	1	X=00 _H (Upper)				X=00 _H (Lower)								↔		X=7F _H (Upper)				X=7F _H (Lower)									
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
		palette A				palette B				palette C				↕		↕		palette A				palette B				palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↕		↕		SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

Color mode, 8-bit data bus mode, C256 mode (C256=1)

ABS	SWAP	X address / bit / segment assign																
*	0	X=00 _H								↔	X=7F _H							
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A			palette B			palette C		↕	palette A			palette B			palette C	
		SEGA ₀			SEGB ₀			SEGC ₀		↕	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇	

ABS	SWAP	X address / bit / segment assign																
*	1	X=00 _H								↔	X=7F _H							
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A			palette B			palette C		↕	palette A			palette B			palette C	
		SEGC ₀			SEGB ₀			SEGA ₀		↕	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇	

B&W mode, 16-bit data bus mode

[illegible]

ABS	SWAP	X address / bit / segment assign																																			
0	1	X=00 _H																↔	X=7F _H																		
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀			
		SEGC ₀					SEGB ₀					SEGA ₀							↕	SEGC ₁₂₇					SEGB ₁₂₇					SEGA ₁₂₇							

[illegible]

ABS	SWAP	X address / bit / segment assign																																	
1	1	X=00 _H																↔	X=7F _H																
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↑ ↓	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
						SEGC ₀				SEGB ₀				SEGA ₀				↑ ↓					SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇				

B&W mode, 8-bit data bus mode

ABS	SWAP	X address / bit / segment assign																									
0	0	X=00 _H (Upper)							X=00 _H (Lower)					↔	X=7F _H (Upper)							X=7F _H (Lower)					
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	
		SEGA ₀								SEGB ₀						SEGA ₁₂₇							SEGB ₁₂₇				
														↕													

ABS	SWAP	X address / bit / segment assign																									
0	1	X=00 _H (Upper)							X=00 _H (Lower)					↔	X=7F _H (Upper)							X=7F _H (Lower)					
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	
		SEGC ₀								SEGA ₀					↕	SEGC ₁₂₇							SEGB ₁₂₇				
																											

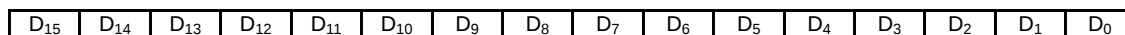
ABS	SWAP	X address / bit / segment assign																									
1	0	X=00 _H (Upper)				X=00 _H (Lower)								↔	X=7F _H (Upper)				X=7F _H (Lower)								
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
		SEGA ₀				SEGB ₀				SEGC ₀				↕	SEGA ₁₂₇				SEGB ₁₂₇					SEGC ₁₂₇			

ABS	SWAP	X address / bit / segment assign																									
1	1	X=00 _H (Upper)				X=00 _H (Lower)								↔	X=7F _H (Upper)				X=7F _H (Lower)								
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
		SEGC ₀				SEGB ₀				SEGA ₀				↕	SEGC ₁₂₇				SEGB ₁₂₇					SEGA ₁₂₇			

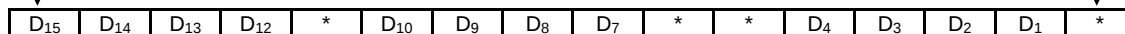
Write and read data bit assignment (in the 16-bit data bus mode)

ABS=0

Write data

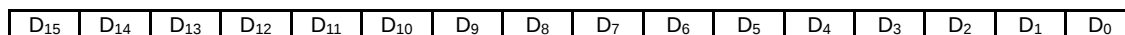


Read data

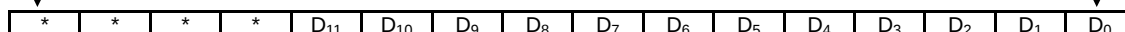


ABS=1

Write data



Read data



Examples for write and read display data (In 8 bit bus mode)

ABS=0, C256=0

(Address; Upper bit)

Write data



Read data



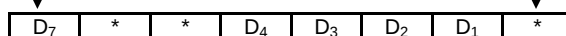
ABS=0, C256=0

(Address; Lower bit)

Write data



Read data



ABS=1, C256=0

(Address; Upper bit)

Write data



Read data



ABS=1, C256=0

(Address; Lower bit)

Write data



Read data



ABS=0, C256=1

Write data



Read data



*: Invalid Data

Icon segment register address bit assignment

Color mode, 16-bit data bus mode

ABS	SWAP	X address / bit / segment assign																							
0	0	X=00 _H												X=01 _H											
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSA ₀				SEGSA ₀				SEGSA ₀				SEGSA ₁				SEGSA ₁				SEGSA ₁			

ABS	SWAP	X address / bit / segment assign																							
0	1	X=00 _H												X=01 _H											
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSC ₀				SEGSC ₀				SEGSC ₀				SEGSC ₁				SEGSC ₁				SEGSC ₁			

ABS	SWAP	X address / bit / segment assign																							
1	0	X=00 _H												X=01 _H											
		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSA ₀				SEGSA ₀				SEGSA ₀				SEGSA ₁				SEGSA ₁				SEGSA ₁			

ABS	SWAP	X address / bit / segment assign																							
1	1	X=00 _H												X=01 _H											
		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSC ₀				SEGSC ₀				SEGSC ₀				SEGSC ₁				SEGSC ₁				SEGSC ₁			

Color mode, 8-bit data bus mode

ABS	SWAP	X address / bit / segment assign																							
0	0	X=00 _H (Upper)							X=00 _H (Lower)					X=01 _H (Upper)						X=01 _H (Lower)					
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀				SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	X address / bit / segment assign																							
0	1	X=00 _H (Upper)							X=00 _H (Lower)					X=01 _H (Upper)						X=01 _H (Lower)					
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSC ₀				SEGSB ₀				SEGSA ₀				SEGSC ₁				SEGSB ₁				SEGSA ₁			

ABS	SWAP	X address / bit / segment assign																							
1	0	X=00 _H (Upper)				X=00 _H (Lower)								X=01 _H (Upper)				X=01 _H (Lower)							
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀				SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	X address / bit / segment assign																							
1	1	X=00 _H (Upper)				X=00 _H (Lower)								X=01 _H (Upper)				X=01 _H (Lower)							
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		palette A				palette B				palette C				palette A				palette B				palette C			
		SEGSC ₀				SEGSB ₀				SEGSA ₀				SEGSC ₁				SEGSB ₁				SEGSA ₁			

B/W mode, 16-bit data bus mode

ABS	SWAP	X address / bit / segment assign																																
0	0	X=00 _H																X=01 _H																
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
		SEGS _{A0}						SEGS _{B0}						SEGS _{C0}				SEGS _{A1}						SEGS _{B1}						SEGS _{C1}				

ABS	SWAP	X address / bit / segment assign																																
0	1	X=00 _H																X=01 _H																
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
		SEGS _{C0}					SEGS _{B0}							SEGS _{A0}				SEGS _{C1}						SEGS _{B1}						SEGS _{A1}				

ABS	SWAP	X address / bit / segment assign																																
1	0	X=00 _H																X=01 _H																
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
						SEGS _{A0}				SEGS _{B0}				SEGS _{C0}								SEGS _{A1}				SEGS _{B1}				SEGS _{C1}				

ABS	SWAP	X address / bit / segment assign																																
1	1	X=00 _H																X=01 _H																
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
						SEGS _{C0}				SEGS _{B0}				SEGS _{A0}								SEGS _{C1}				SEGS _{B1}				SEGS _{A1}				

B/W mode, 8-bit data bus mode

ABS	SWAP	X address / bit / segment assign																							
0	0	X=00 _H (Upper)							X=00 _H (Lower)				X=01 _H (Upper)				X=01 _H (Lower)								
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}				SEGS _{B1}				SEGS _{C1}			

ABS	SWAP	X address / bit / segment assign																							
0	1	X=00 _H (Upper)							X=00 _H (Lower)					X=01 _H (Upper)						X=01 _H (Lower)					
		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		SEGS _{C0}				SEGS _{B0}				SEGS _{A0}				SEGS _{C1}				SEGS _{B1}				SEGS _{A1}			

ABS	SWAP	X address / bit / segment assign																							
1	0	X=00 _H (Upper)				X=00 _H (Lower)								X=01 _H (Upper)				X=01 _H (Lower)							
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}				SEGS _{B1}				SEGS _{C1}			

ABS	SWAP	X address / bit / segment assign																							
1	1	X=00 _H (Upper)				X=00 _H (Lower)								X=01 _H (Upper)				X=01 _H (Lower)							
		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		SEGS _{C0}				SEGS _{B0}				SEGS _{A0}				SEGS _{C1}				SEGS _{B1}				SEGS _{A1}			

(11) Gradation palette

In the gradation mode, variable or fixed gradation mode is selected by programming the “PWM” register in the “Gradation control” instruction.

PWM=0: Variable gradation mode
 (Select 16 gradation levels out of a palette consisting of 32-gradation levels)

PWM=1: Fixed gradation mode
 (Fixed 8-gradation levels)

In the gradation mode, each of the gradation palettes Aj, Bj and Cj can select 16-gradation levels out of a palette consisting of 32-gradation levels by setting 5-bit palette value into the “PA” registers in the “Gradation palette j” instructions (j=0 to Fh).

The gradation palettes Aj correspond to the SEGAI, the Bj to SEGBj and the Cj to SEGCI (j=0 to 15, i=0 to 127).

The correspondence between display data and gradation palettes

Table 10 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

(MSB) Display data (LSB)				Gradation palette	Default palette value
0	0	0	0	Palette 0	0 0 0 0
0	0	0	1	Palette 1	0 0 0 1
0	0	1	0	Palette 2	0 0 1 0
0	0	1	1	Palette 3	0 0 1 1
0	1	0	0	Palette 4	0 1 0 0
0	1	0	1	Palette 5	0 1 0 1
0	1	1	0	Palette 6	0 1 1 0
0	1	1	1	Palette 7	0 1 1 1
1	0	0	0	Palette 8	1 0 0 0
1	0	0	1	Palette 9	1 0 0 1
1	0	1	0	Palette10	1 0 1 0
1	0	1	1	Palette11	1 0 1 1
1	1	0	0	Palette12	1 1 0 0
1	1	0	1	Palette13	1 1 0 1
1	1	1	0	Palette14	1 1 1 0
1	1	1	1	Palette15	1 1 1 1

Gradation palette table (PWM="0", MON="0", Variable gradation mode)

Table 11 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0 0	0	Palette 0(default)	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 0(default)8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette 1(default)	1 0 0 1 1	19/31	Palette 9(default)
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 2(default)	1 0 1 0 1	21/31	Palette 10(default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette 3(default)	1 0 1 1 1	23/31	Palette 11(default)
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette 4(default)	1 1 0 0 1	25/31	Palette 12(default)
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette 5(default)	1 1 0 1 1	27/31	Palette 13(default)
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette 6(default)	1 1 1 0 1	29/31	Palette 14(default)
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette 7(default)	1 1 1 1 1	31/31	Palette 15(default)

Gradation palette table (PWM="1", MON="0", Fixed gradation mode)

Table 12 8-gradation segment drivers

(MSB) Display data (LSB)				Gradation level
0	0	0	*	0/7
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

(MSB) Display data (LSB)				Gradation level
0	0	*	*	0/7
0	0	*	*	
0	1	*	*	3/7
0	1	*	*	
1	0	*	*	5/7
1	0	*	*	
1	1	*	*	7/7
1	1	*	*	

The correspondence between display data and gradation level (MON="1", B&W mode)

Table 13

(MSB) Display data (LSB)				Gradation level
0	*	*	*	0
1	*	*	*	1

*:Don't care

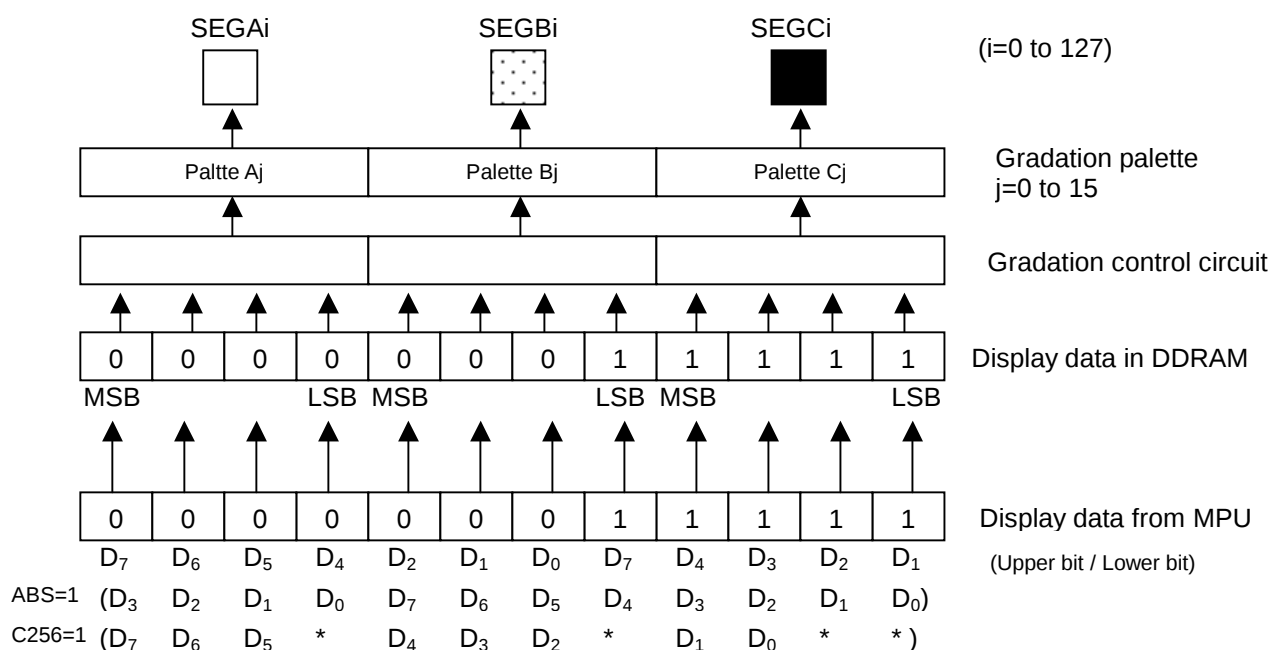
(12) Gradation control and display data

(12-1) Gradation mode

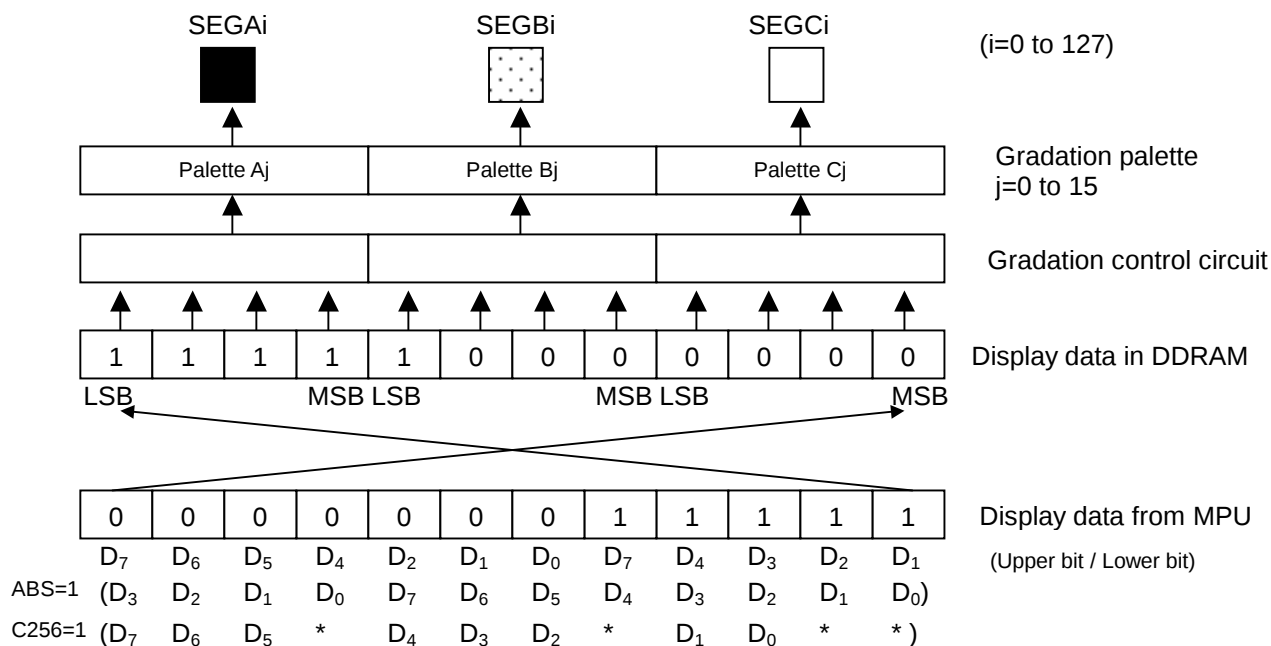
In the gradation mode, each pixel for RGB corresponds to the successive 3 segment drivers that each segment driver provides 16-gradation PWM output, so that **NJU6824** can drive a 4096-color display (16-gradation x 16-gradation x 16-gradation = 4-bit x 4-bit x 4-bit) with up to 128x128 pixels. The 16-gradation segment drivers can generate 16-gradation levels controlled by using 4-bit of display data in the DDRAM.

In addition, the LSI can transfer 16-bit display data for 1-pixel RGB by one-time access or 8-bit by two-time access. The display data assignments for the gradation palettes and segment drivers vary in accordance with the setting for the "SWAP" bit in the "Display control (2)" instruction.

- SWAP = 0

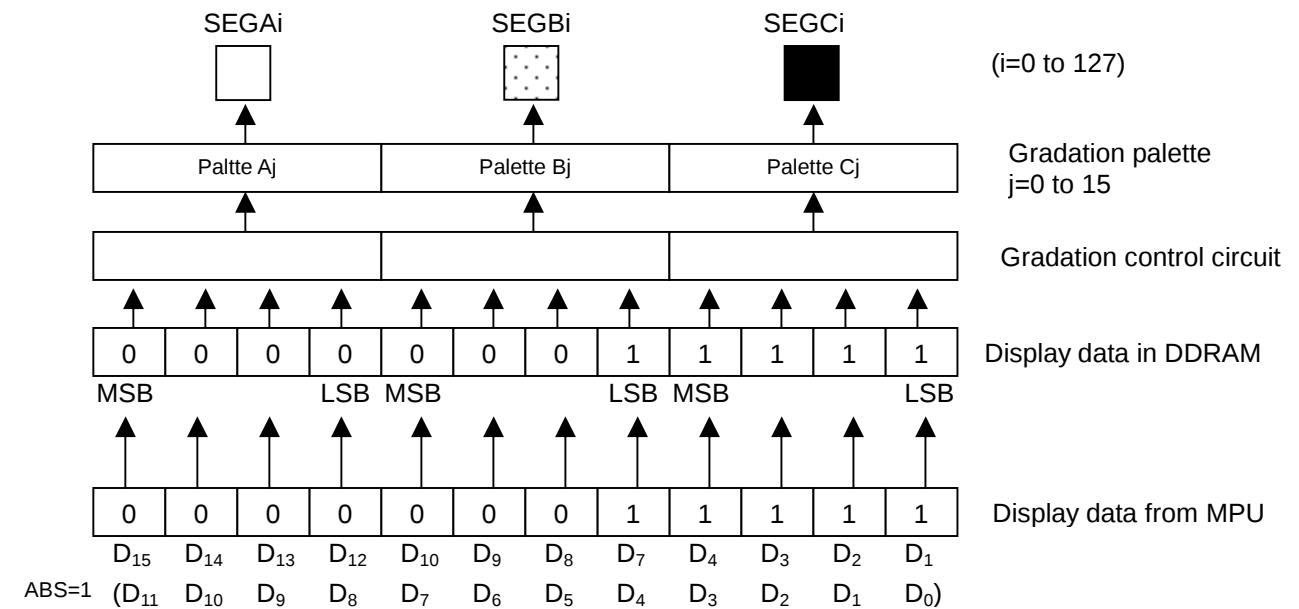


- SWAP = 1

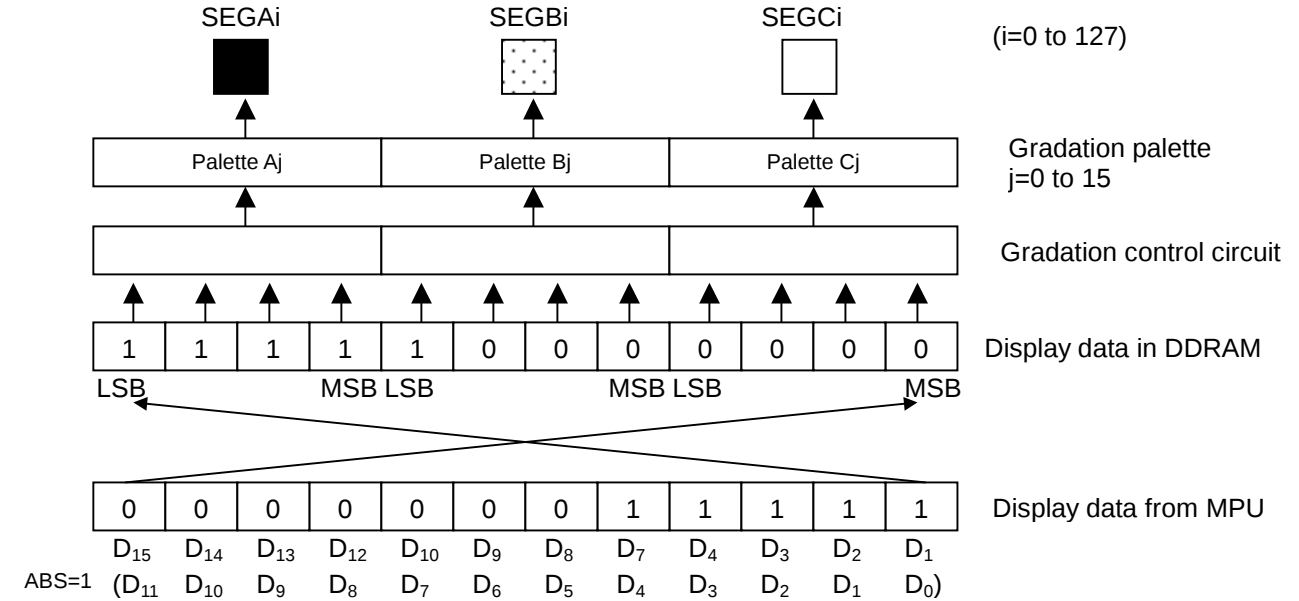


In the 16-bit data bus mode, the display data assignments for the gradation palettes and segment drivers vary in accordance with the setting for the "SWAP" bit in the "Display control (2)" instruction as well as the assignment in the 8-bit data bus mode.

- SWAP = 0



- SWAP = 1

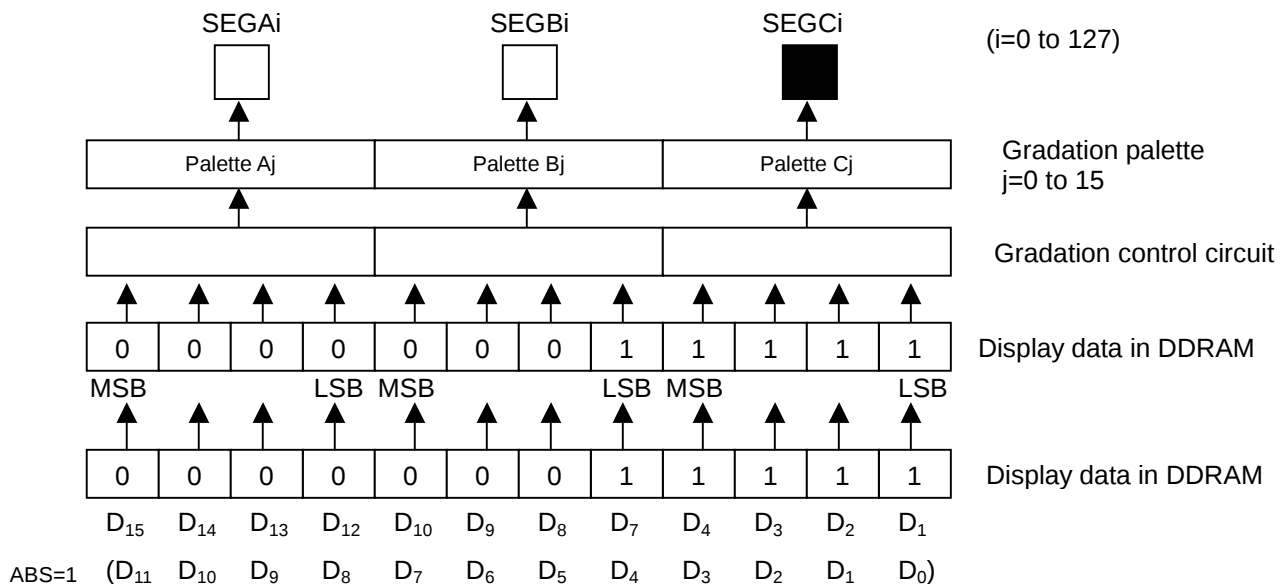


(12-2) B&W mode (MON="1")

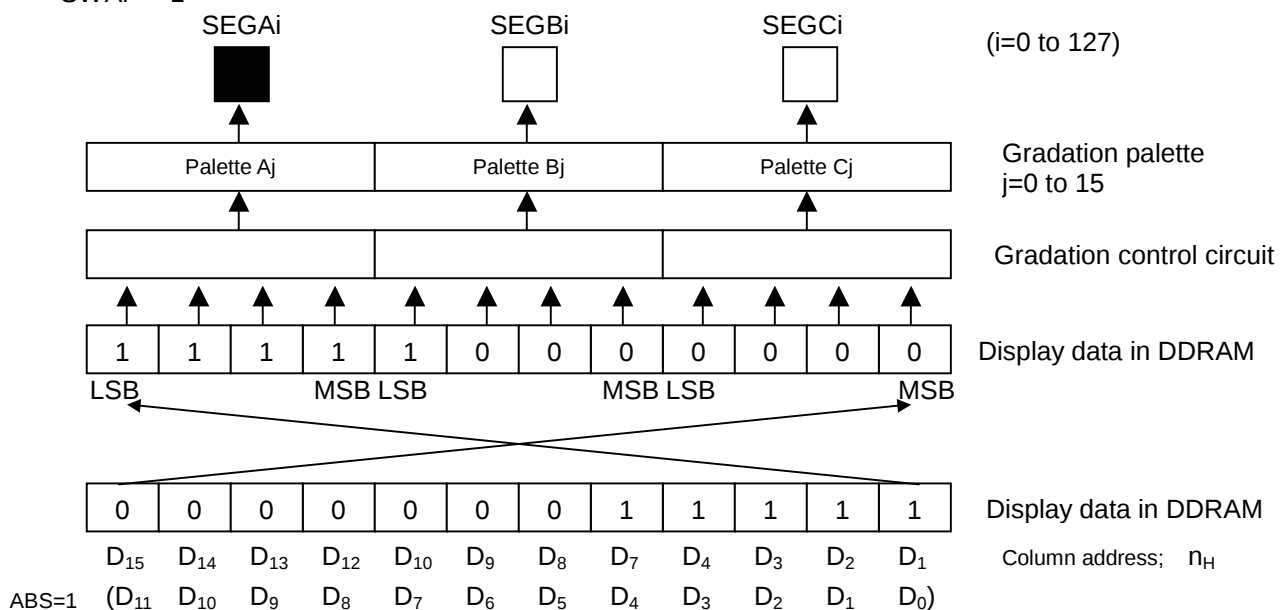
In the B&W mode, only 3 of MSB of each display data are used for the display by the 16-bit data bus mode and 8-bit.

16-bit data bus access example (Similarly 8-bit data bus access)

- SWAP = 0



- SWAP = 1



The correlation of display data with gradation control is also applied to Icon segment.

(13) Display timing generator

The display-timing generator creates the timing pulses such as the CL, FLM, FR and CLK by dividing the oscillation frequency oscillate an external or internal resistor mode. The each of timing pulses is outputted through the each output terminals by "SON" = 1.

(14) LCD line clock (CL)

The LCD line clock (CL) is used as the count-up signal for the line counter and the latch signal for the data latch circuit. At the rising edge of the CL signal, the line counter is counted-up and the 384-bit display data, corresponding to the counted-up line address, is latched into the data latch circuit. And at the falling edge of the CL signal, the latched data output onto the segment drivers. The read out operation from DDRAM to the latch is completely independent from the MPU accessing. Therefore, MPU can access to the LSI regardless the internal operation.

(15) LCD alternate signal (FR) and LCD synchronous signal (FLM)

Both of the FR and FLM signals are created from the CL signal. The FR signal is used to alternate inverse driving for the LCD panel. It can be programmed so that the FR signal is toggle on every frame in the default setting or once every N frames in the N-line inversion mode. The FLM signal is used to indicate the start line of a new display frame. It presets an initial display line address into the line counter when the FLM signal becomes "1".

(16) Data latch circuit

The data latch circuit is used temporarily store the display data that will output to the segment drivers. The display data in this circuit is updated in synchronization of the CL signal.

The "All pixels ON/OFF", "Display ON/OFF" and "Reverse display ON/OFF" instructions change the display data in this circuit but do not change the display data in the DDRAM.

(17) Common and segment drivers

The LSI includes 384+6-segment drivers and 128-common drivers for a graphic display. The common drivers generate the LCD driving waveforms composed of the V_{LCD} , V_1 , V_4 and V_{SS} in accordance with the FR signal and scanning data. The segment drivers generate the waveforms composed of the V_{LCD} , V_2 , V_3 and V_{SS} in accordance with the FR signal and display data.

LCD Driving waveforms (Reverse display OFF, 1/129 duty, B&W mode)

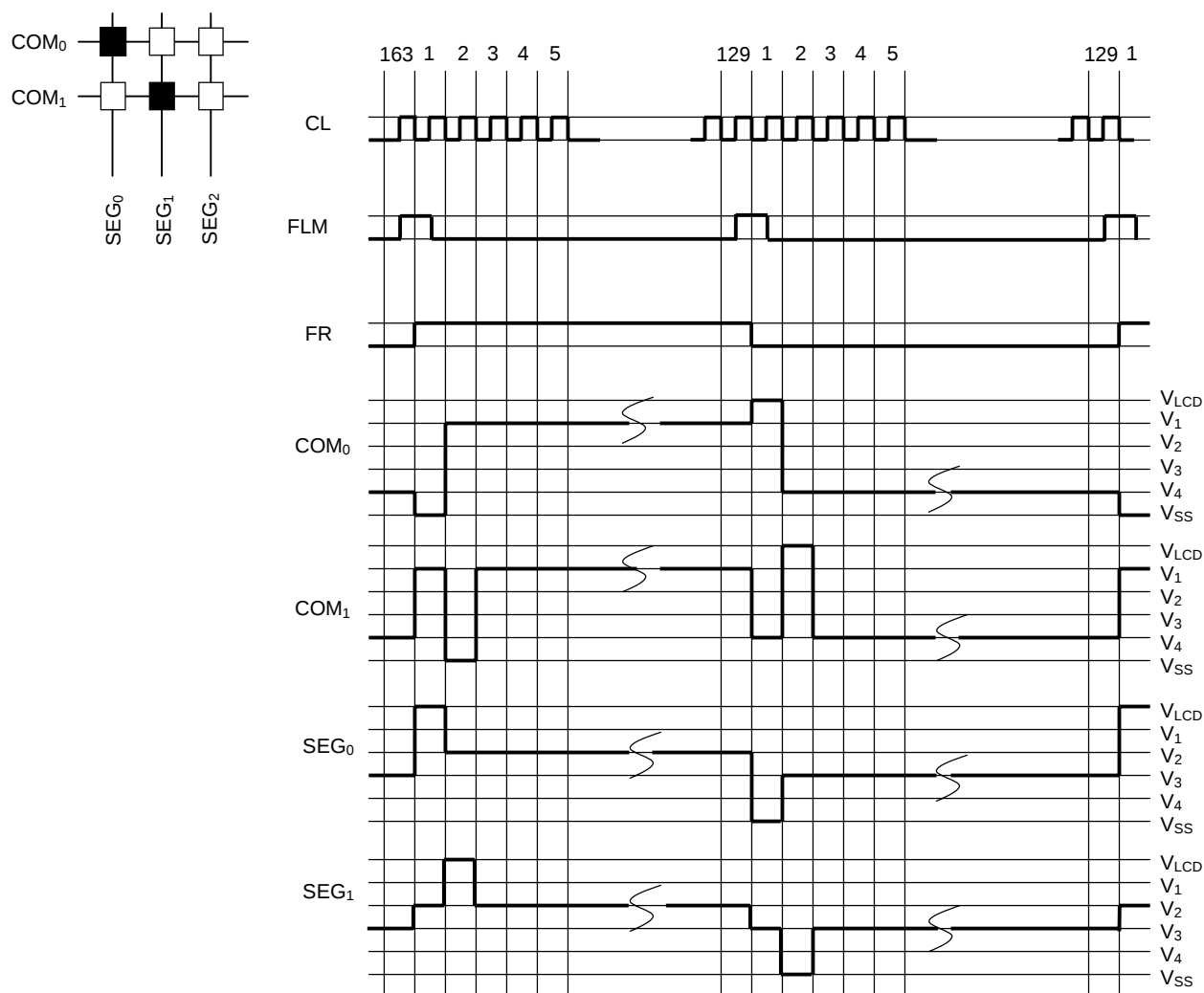


Fig 8

(18) Icon Segment Driver Circuit

Each 3 outputs (SEGSA0 to SEGSA1, SEGSB0 to SEGSB1, SEGSC0 to SEGSC1) placed at both edges of normal segment output terminals line are Segment outputs for Icon. Although normal Segment output generates the LCD driving voltage corresponding with the data in Display Data RAM, Icon segment driver provides the register instead of the display data RAM. The data corresponding to SEGSA0, SEGSB0 and SEGSC0 are in 12-bit register and output the same driving voltage on the row direction. (The data corresponding to SEGSA1, SEGSB1 and SEGSC1 are same as SEGSA0, SEGSB0 and SEGSC0.)

The outputs of SEGSA0 to SEGSA1 assign the same gradation pallet as SEGSA0 to SEGSA127, SEGSB0 to SEGSB1 are SEGSB0 to SEGSB127 and SEGSC0 to SEGSC1 are SEGSC0 to SEGSC127.

Icon Segment Driver Circuit operates for the outline frame display or background. These displays are changed in accordance with attribute of ALLON or REV command, but no change by LREV command.

The capacity of register corresponding with Icon segment driver (SEGSA0 to SEGSA1, SEGSB0 to SEGSB1, SEGSC0 to SEGSC1) is 24 bits. The access to from this register performed at DMY="1"..

Table14

RS	DMY	68type	80 type		Function
		R/W	$\overline{\text{RD}}$	$\overline{\text{WR}}$	
L	0	H	L	H	Display data read
L	0	L	H	L	Display data write
L	1	H	L	H	Icon segment register read
L	1	L	H	L	Icon segment register read

Read out function from the Icon segment register is restricted as same as the display data read out function from Display Data RAM. After address set, the addressed data does not come out by the first read instruction immediately but comes out by the second read instruction. Therefore, one dummy read out function is required for data read from Icon segment register after the address set or the data write operation.

When the Icon segment registers are accessed in DMY="1", the valid addressing is just a column address. Because of 24 bits Icon register, the valid addresses are "00h" and "01h" in 8-bit or 16-bit mode.

When the Icon segment registers are accessed in DMY="1", the data write operation into Icon register is enabled with the increment / decrement operation.

The column address increment operates as shown below. But the auto carry up operation like as the maximum address to "00h" does not operate of the display data RAM access.

00h -> Max.

- 8-bit or 16-bit data bus mode (DMY="1")

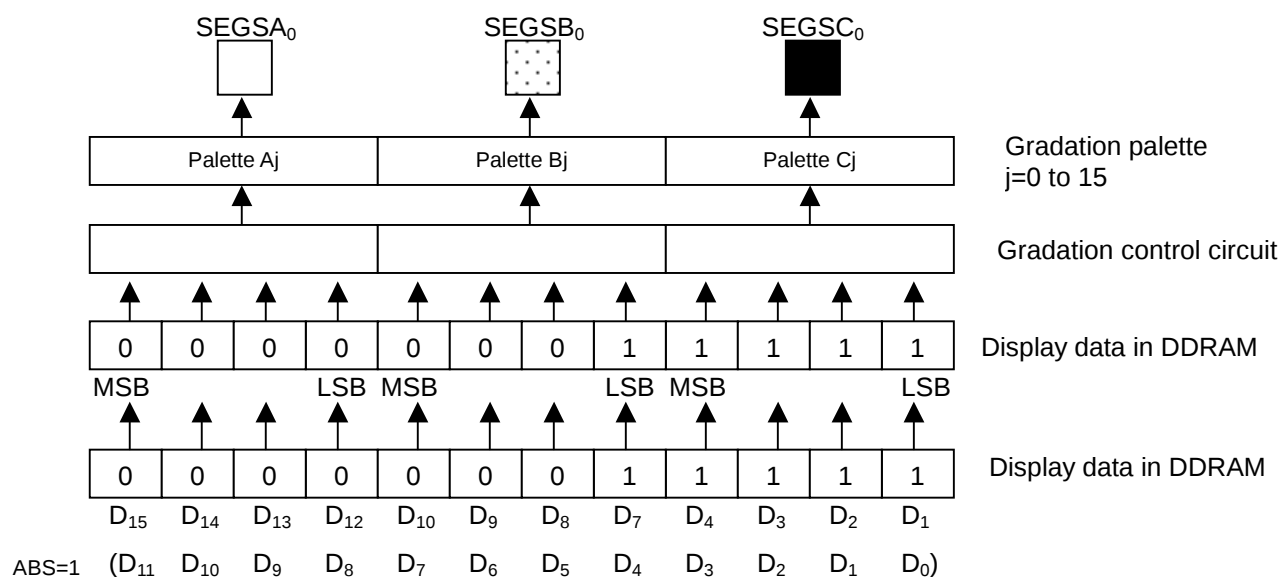
Column address	00 _H :	SEGSA ₀ , SEGSB ₀ , SEGSC ₀
	01 _H :	SEGSA ₁ , SEGSB ₁ , SEGSC ₁

Note) Refer the "Icon segment register address bit assignment" in (10) The relationship among the DDRAM column address, display data and segment drivers. Both of Icon segment register and Display data RAM operate a same address counter so that the address is set again in the status transition of DMY = "0" to "1" or "1" to "0".

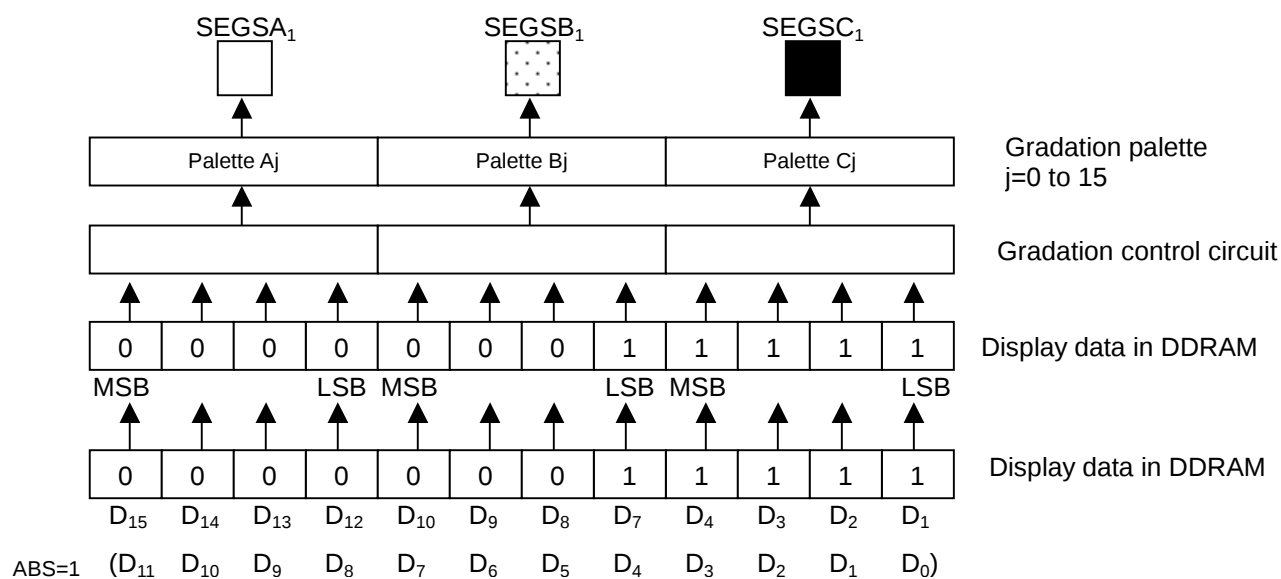
The access to Icon register must be operated in the condition of HV=0.

Examples for the dummy segment registers (DMY="1")
(In the 16-bit data bus mode, gradation mode, (REF,SWAP)=(0,0))

Column address: 00_H



Column address: 01_H



(19) Oscillator

The oscillator generates the internal clock for the display timing and voltage booster. The C and R for the oscillator are on-chipped, therefore, there is no C, R required as an external components. Use an external R instead of internal R is also available (CSK=1), in this time connect the resistor between OSC₁ and OSC₂ terminals. However, when the internal oscillator is not used, an external clock, which duty should be 50%, inputs onto the OSC₁ terminal.

In addition, the value of the feed back resistor for the oscillator can be varied by programming the "Rf" register in the "Frequency control" instruction so that it is possible to optimize the frame frequency for a LCD panel.

[Setting of MON(B&W /Gradation) and PWM(Variable gradation/Fixed gradation)]

In case of the internal oscillation mode (CSK=0)

Symbol	MON	PWM	Display mode
FR1	0	0	Variable gradation mode
FR2	0	1	Fixed gradation mode
FR3	1	*	B&W mode

*: Don't care

In case of the external resistor oscillation mode(CSK=1)

In case of the external resistor oscillation, clock frequency should be adjusted with resistor as same as the frequency of internal oscillation. And also MON and PWM should be set.

In case of the external clock input mode(CSK=1)

In case of the external clock input operation, clock frequency should be input as same as the frequency of internal oscillation on a display mode. And also MON and PWM should be set. Because the frame frequency and the internal voltage booster circuit operation frequency are determined by the external clock frequency and conditions of MON and PWM.

(20) Power supply circuits

The internal power supply circuits are composed of the voltage booster, electrical variable resistor (EVR), voltage regulator, reference voltage generator and voltage followers.

The status of the power supply circuits is arranged by programming the "DCON" and "AMPON" registers in the "Power control" instruction. For this arrangement, the part of the internal power supply circuits can be used in combination with an external power supply as described in the following table.

Table 15

DCON	AMPON	Voltage booster	Voltage followers Voltage regulator EVR	External voltage	Note
0	0	Disable	Disable	V _{OUT} , V _{LCD} , V ₁ , V ₂ , V ₃ , V ₄	1, 3
0	1	Disable	Enable	V _{OUT}	2, 3
1	1	Enable	Enable	—	—

Note1) The internal power circuits are not used. The C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋, V_{OUT}, V_{REF}, V_{REG} and V_{EE} terminals should be open.

Note2) The internal power circuits are used, excluding the voltage booster. The external V_{OUT} voltage is required and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋ and V_{EE} terminals should be open. The reference voltage is required into V_{REF} terminal.

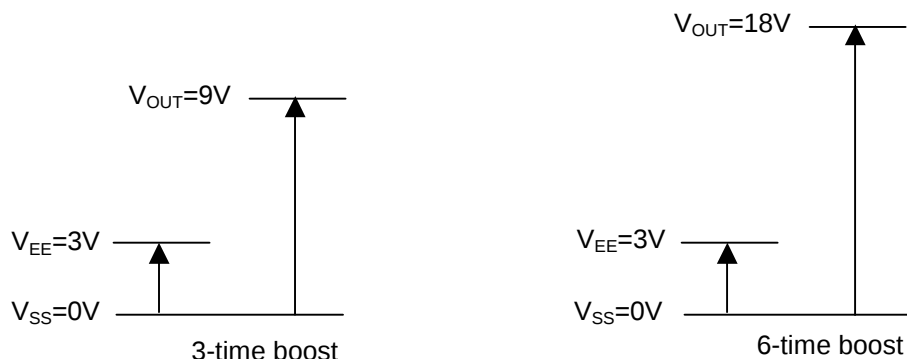
Note3) The relation among the voltages should be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$$

(21) Voltage booster

The voltage booster generates maximum 6x voltage of the V_{EE} level. It is programmed so that the boost level can be selected out of 1x, 2x, 3x, 4x, 5x and 6x by the “Boost level select” instruction. The boosted voltage V_{OUT} must not exceed beyond 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

Boosted voltages



Capacitor connections for the voltage Booster

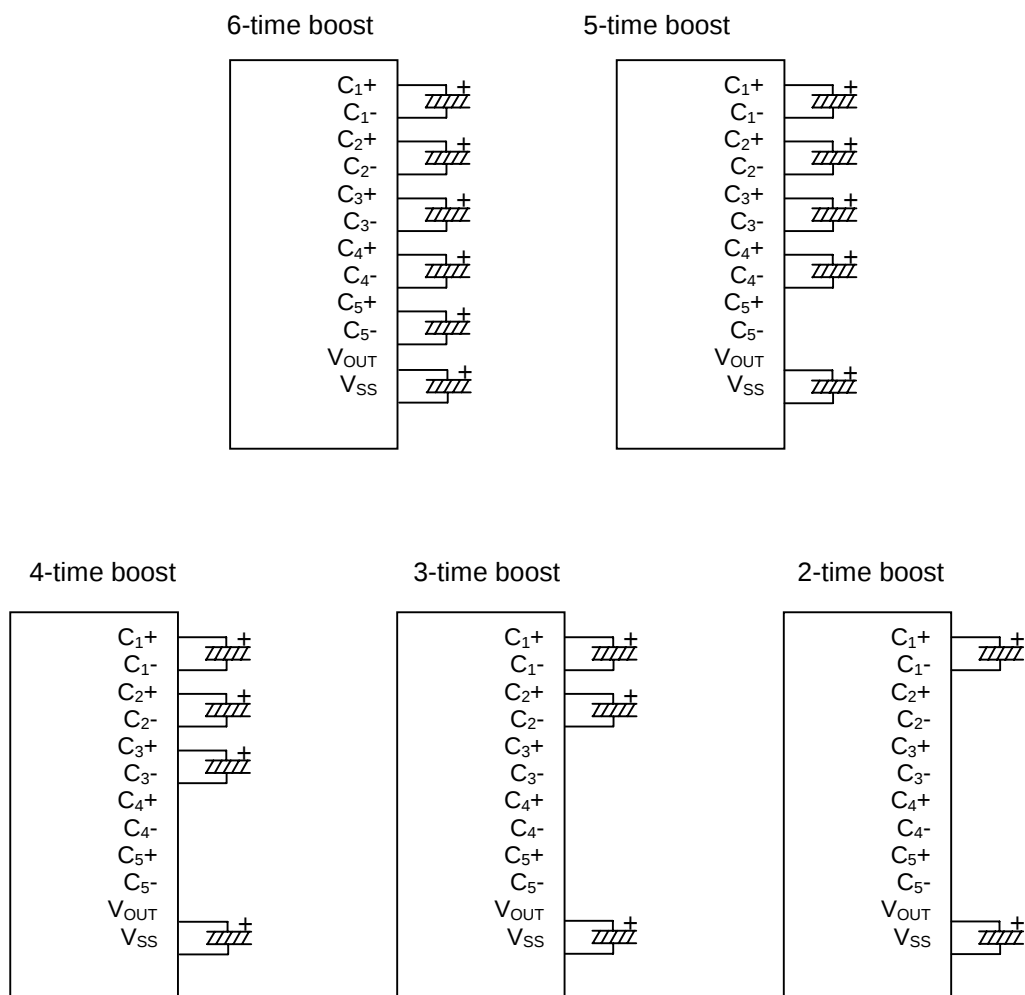


Fig 9

(22) Reference voltage generator

The reference voltage generator is used to produce the reference voltage (V_{BA}) that is output from the V_{BA} terminal and input to the V_{REF} terminal.

$$V_{BA} = V_{EE} \times 0.9$$

(23) Voltage regulator

The voltage regulator, composed of the gain control circuit and operational amplifier, is used to gain the reference voltage (V_{REF}) and create the regulated voltage (V_{REG}). The V_{REG} is used for the input voltage for the EVR by programming the "VU" register in the "Boost level" instruction.

$$V_{REG} = V_{REF} \times N \quad (N: \text{register value for the boost level})$$

(24) Electrical variable resister (EVR)

The EVR, variable with 128-step, is used to fine-tune the LCD driving voltage (V_{LCD}) by programming the "DV" register in the "EVR control" instruction, so that it is possible to optimize the contrast level for a LCD panel.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (M: \text{register value for the EVR})$$

(25) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates the VLCD voltage levels as V_{LCD} , V_1 , V_2 , V_3 and V_4 with internal E.V.R and Bleeder resistors. And a BIAS ratio of LCD driving voltage can be selected out of follows; 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11 or 1/12.

In case of internal power supply operation, a voltage stabilization capacitor CA_2 must be connected to V_{LCD} , V_1 , V_2 , V_3 and V_4 terminals, and the value of CA_2 is fixed with the result of actual LCD display evaluation.

In case of external power supply operation, the LCD driving voltages as V_{LCD} , V_1 , V_2 , V_3 and V_4 should be supplied from the external power supply in OFF state of internal power supply (DCON = AMPON = "0"). In this mode, voltage booster terminals as $C1+$, $C1-$, $C2+$, $C2-$, $C3+$, $C3-$, $C4+$, $C4-$, $C5+$, $C5-$, V_{EE} , V_{REF} and V_{REG} should be opened.

In case of external power supply operation and a part of internal (Voltage converter), $C1+$, $C1-$, $C2+$, $C2-$, $C3+$, $C3-$, $C4+$, $C4-$, $C5+$ and $C5-$ terminals should be opened because the voltage booster circuit does not operate, a power for the voltage converter circuit should supply into V_{OUT} terminal, and a reference voltage is supplied into V_{REF} terminal.

In addition, a capacitor CA_3 should connect into V_{REG} terminal for stabilization.

< Bias adjustment function >

NJU6823 prepares bias adjustment terminals V_1A_1 , V_1A_2 , V_4A_1 and V_4A_2 for fine adjustment of V_1 and V_4 out of voltages.

The status combination of V_1A_1 terminal and V_1A_2 can adjust V_1 voltage in below table and V_4A_1 and V_4A_2 can adjust V_4 voltage. These adjustment performs by the connection change between the Bleeder resistors and the output buffer operational amplifier as voltage follower circuit.

V_1A_1 terminal	V_1A_2 terminal	Fluctuation voltage [mV] *1
0	0	0
0	1	+5
1	0	-5
1	1	+10

V_4A_1 terminal	V_4A_2 terminal	Fluctuation voltage [mV] *1
0	0	0
0	1	+5
1	0	-5
1	1	-10

Note 1) The fluctuation voltage is a adjusted voltage against the default voltage at (V_1A_1 , V_1A_2 = "0, 0" and V_4A_1 , V_4A_2 = "0, 0"). The "+" mark means a direction of voltage fluctuation to V_{LCD} and the "-" is to V_{SS} .

Note 2) The fluctuation voltage is an ideal value.

Note 3) The fluctuation voltage is at $V_{LCD}=13.5V$.

Note 4) "0" of V_1A_1 , V_1A_2 , V_4A_1 and V_4A_2 means V_{SS} and "1" means V_{DD} .

Capacitor connections for the voltage booster

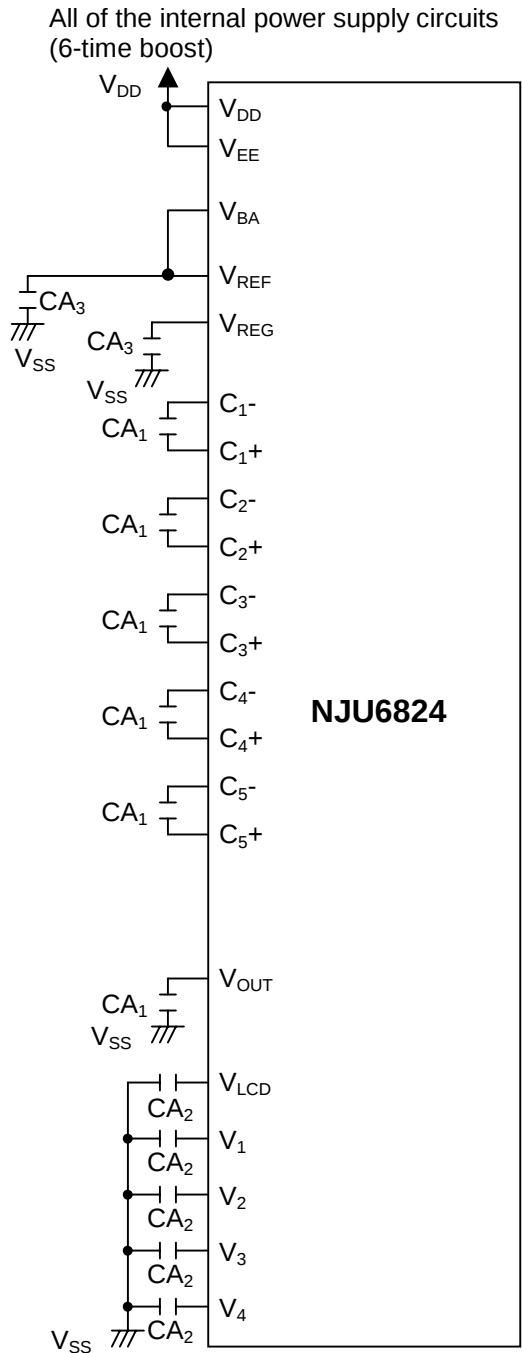


Fig 10

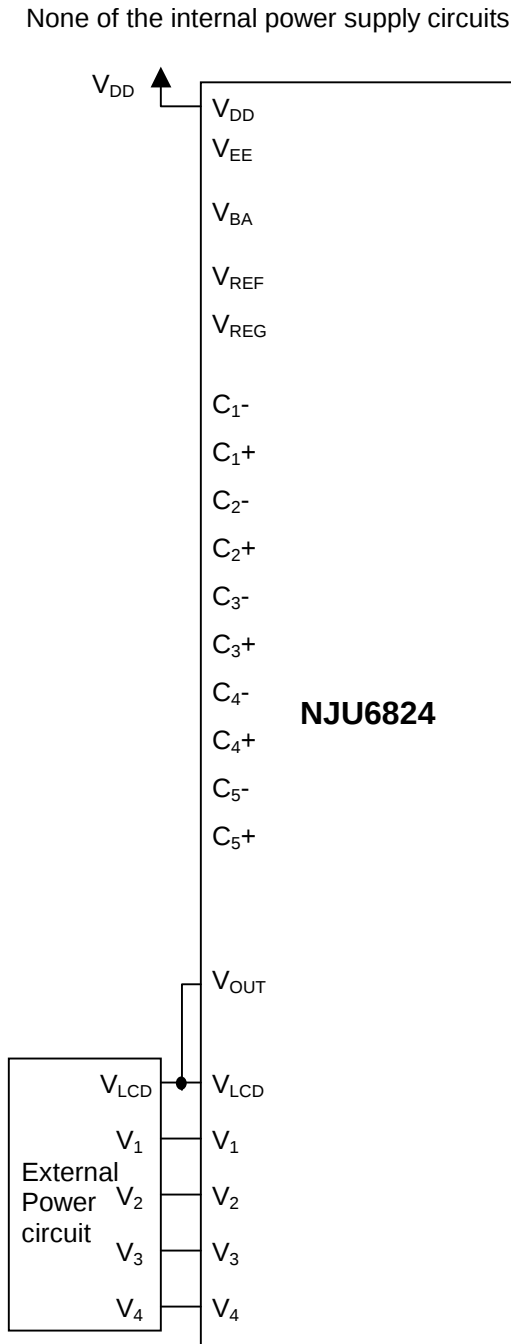


Fig11

Reference values

CA ₁	1.0 to 4.7uF
CA ₂	1.0 to 2.2uF
CA ₃	0.1uF

Note) B grade capacitors are required.

The internal power supply circuits
Excluding the reference voltage generator(1)
(6-time boost)

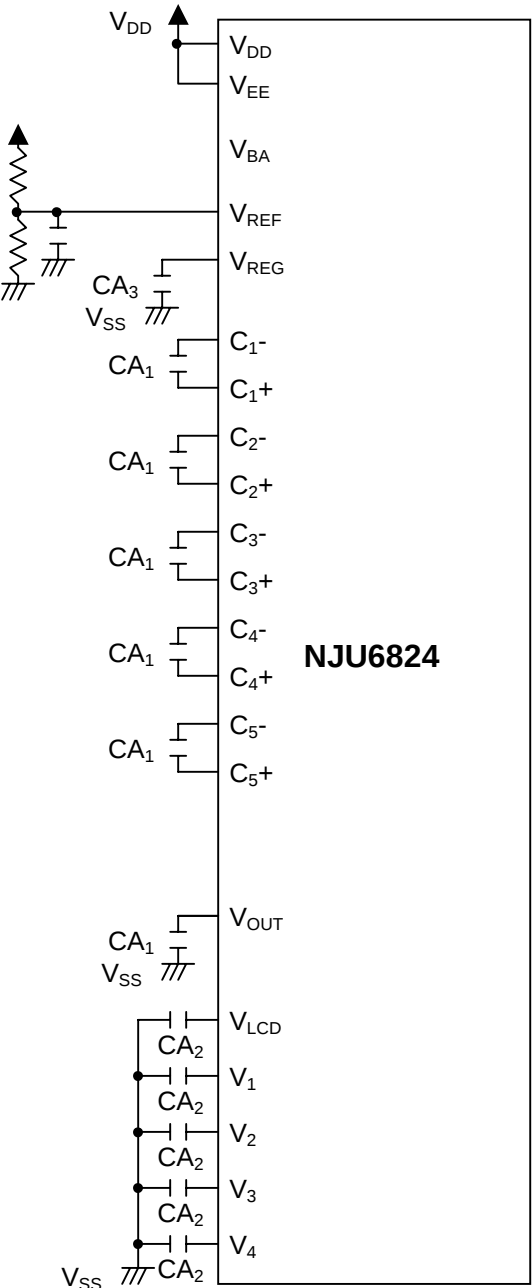


Fig 12

The internal power supply circuit
Excluding the reference voltage generator(2)
(6-time boost, temperature compensation)

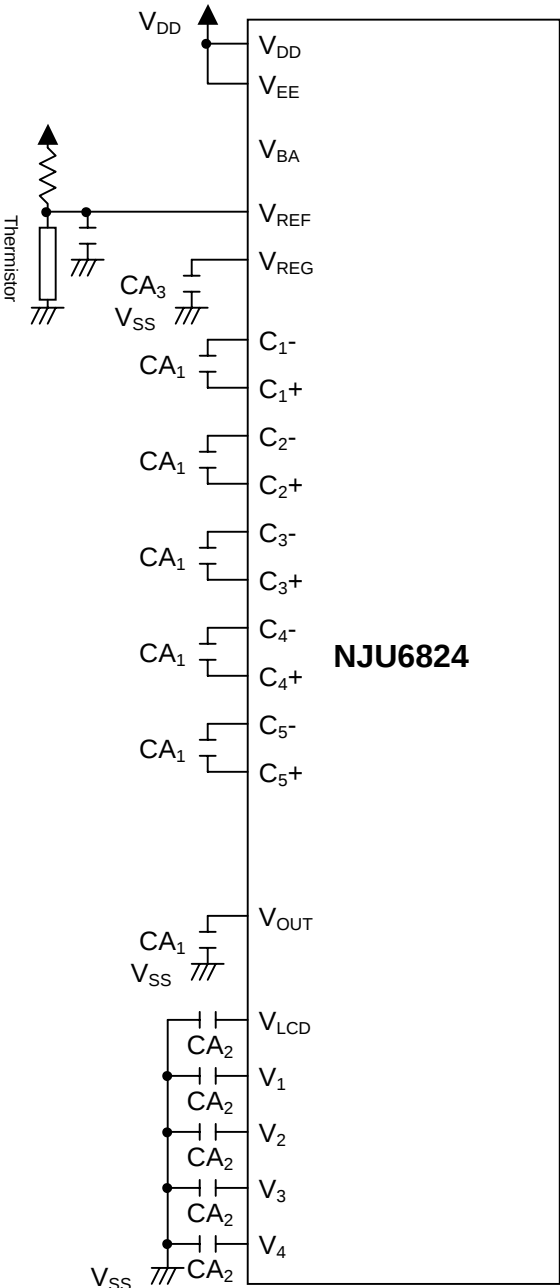


Fig 13

Reference value

CA ₁	1.0 to 4.7μF
CA ₂	1.0 to 2.2μF
CA ₃	0.1μF

Note) B grade capacitors are required.

The internal power supply circuits
Excluding the voltage booster

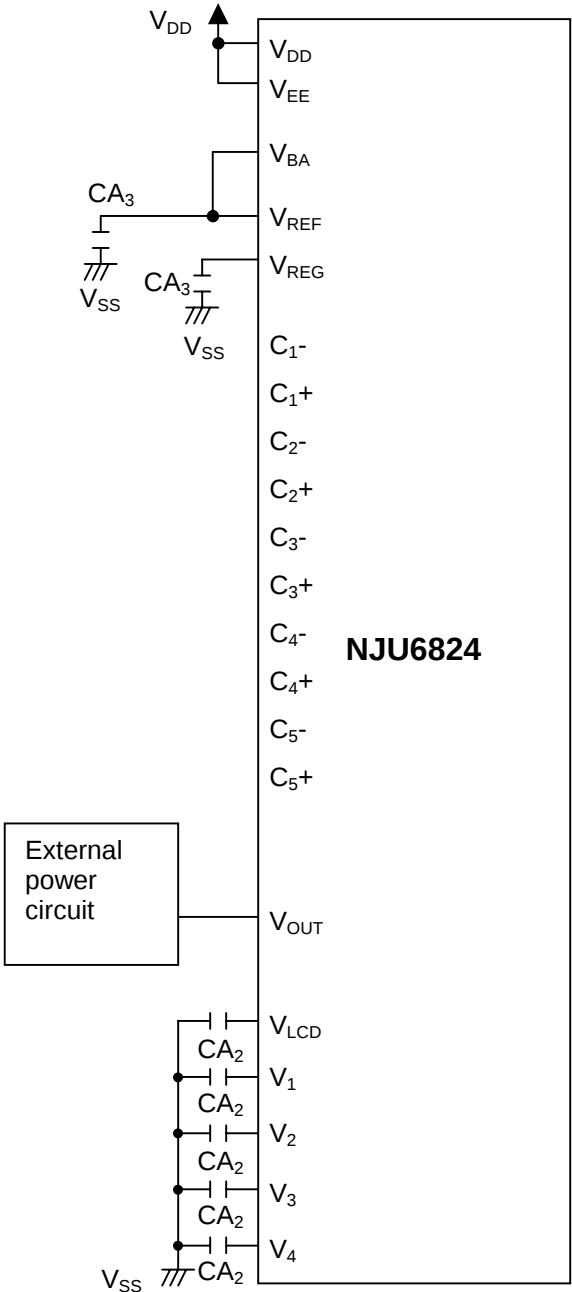


Fig 14

Reference value

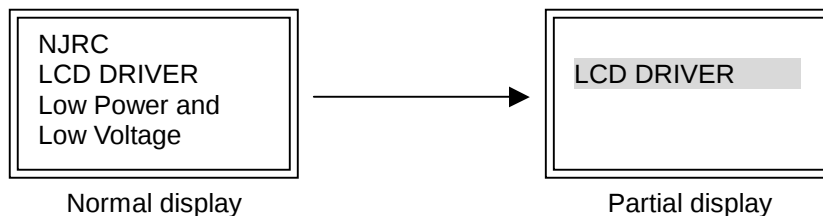
CA ₁	1.0 to 4.7μF
CA ₂	1.0 to 2.2μF
CA ₃	0.1μF

Note) B grade capacitors are required.

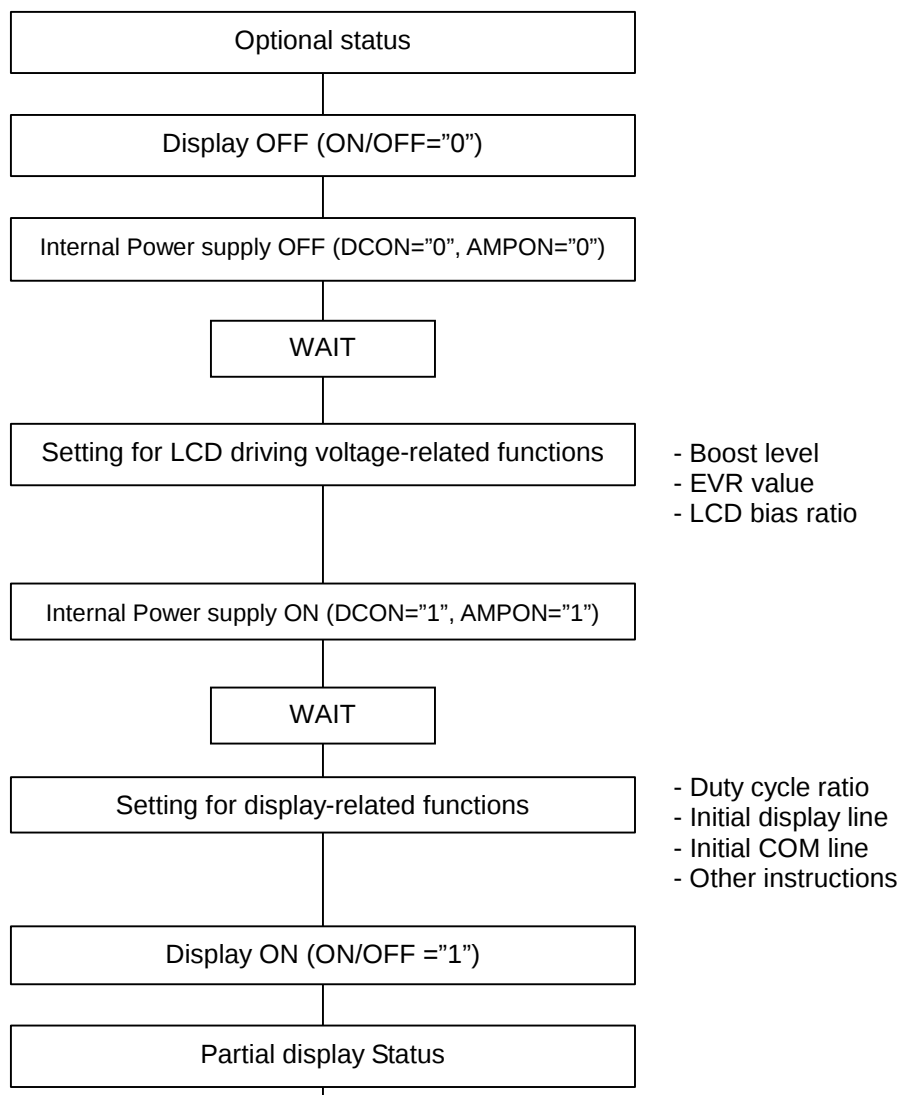
(26) Partial display function

The partial display function is used to specify the partial display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage, so that it is possible to display a time and calendar in the extremely low power consumption. It can be programmed to select a duty cycle ratio (1/17, 1/25, 1/33, 1/41, 1/49, 1/57, 1/65, 1/73, 1/81, 1/89, 1/97, 1/105, 1/113, 1/121, 1/129, in case of DSE=0), LCD bias ratio, boost level and EVR value by the instructions so that it is possible to optimize the LSI condition in accordance with the display status.

Partial display image



Partial display sequence



(27) Discharge circuit

The discharge circuit is used to discharge the electric charge in the capacitors connected to the V_1 to V_4 and V_{LCD} terminals. It is activated by setting "0" into the "DIS" register in the "Discharge" instruction or by setting "RES" terminal to "0" level. The "Discharge ON/OFF" instruction is usually required just after the internal power supply is turned off by setting "0" into the "DCON" and "AMPON" registers, or just after the external power supply is turned off. During the discharge operation, it is required that no supply the power neither from an internal or external power supply to the LSI.

(28) Reset circuit

The reset circuit initializes the LSI into the following default status. It is activated by setting the RES terminal to "0" level. The RES terminal is usually required to connect to the MPU's reset terminal in order that the LSI can be initialized at the same timing of the MPU reset.

● Default status

1. DDRAM display data	:Undefined
2. column address	:(00) _H
3. row address	:(00) _H
4. Initial display line	:(0) _H (1st line)
5. Display ON/OFF	:OFF
6. Reverse display ON/OFF	:OFF (normal)
7. Duty cycle ratio	:1/129 duty(DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM scan direction	:COM ₀ → COM ₁₂₇
10. Address direction of RAM	:(HV, XD, YD) = (0, 0, 0)
11. Read modify write	:OFF (AIM=0)
12. SWAP mode	:OFF (normal)
13. EVR value	:(0, 0, 0, 0, 0, 0, 0)
14. Internal power supply	:OFF
15. Display mode	:Gradation display mode
16. LCD bias ratio	:1/9 bias
17. Gradation Palette 0	:(0, 0, 0, 0, 0)
18. Gradation Palette 1	:(0, 0, 0, 1, 1)
19. Gradation Palette 2	:(0, 0, 1, 0, 1)
20. Gradation Palette 3	:(0, 0, 1, 1, 1)
21. Gradation Palette 4	:(0, 1, 0, 0, 1)
22. Gradation Palette 5	:(0, 1, 0, 1, 1)
23. Gradation Palette 6	:(0, 1, 1, 0, 1)
24. Gradation Palette 7	:(0, 1, 1, 1, 1)
25. Gradation Palette 8	:(1, 0, 0, 0, 1)
26. Gradation Palette 9	:(1, 0, 0, 1, 1)
27. Gradation Palette 10	:(1, 0, 1, 0, 1)
28. Gradation Palette 11	:(1, 0, 1, 1, 1)
29. Gradation Palette 12	:(1, 1, 0, 0, 1)
30. Gradation Palette 13	:(1, 1, 0, 1, 1)
31. Gradation Palette 14	:(1, 1, 1, 0, 1)
32. Gradation Palette 15	:(1, 1, 1, 1, 1)
33. Gradation mode control	:Variable gradation mode
34. Data bus length	:8-bit data bus length
35. Discharge circuit	:OFF

(29) Power supply ON/OFF sequences

The following paragraphs describes the power supply ON/OFF sequences to prevent high current flowing into the LSI, otherwise the current may cause a permanent damage to the LSI.

(29-1) Using an external power supply

- Power supply ON sequence

The logic voltage (V_{DD}) is turned on first, and then the LCD driving voltages (V_1 to V_4 and V_{LCD}) can be turned on. When supply the V_{OUT} from outside, turn on the logic voltage (V_{DD}), then reset, after then supply the V_{OUT} is required.

- Power supply OFF sequence

The reset operation, cut off the V_1 to V_4 and V_{LCD} from the LSI by the RES terminal or the "Power control" instruction first, and then the V_{DD} can be turned off. It is recommended that a series-resistor between 50 ohms and 100 ohms is inserted in the V_{LCD} line (or V_{OUT} line in case of using only an external V_{OUT} voltage) in order to protect the LSI from an over current.

(29-2) Using the internal power supply circuits

- Power supply ON sequence

The V_{DD} is turned on and the reset operation is required first, and then the V_1 to V_4 and V_{LCD} can be turned on by setting "1" into the "DCON" and "AMPON" registers in the "Power control" instruction.

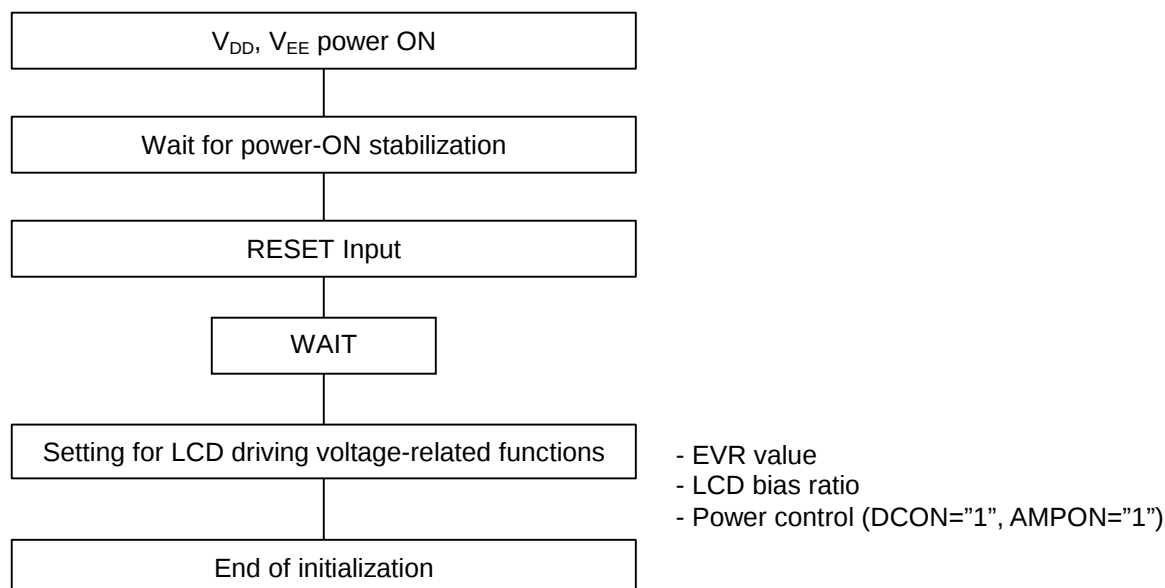
- Power supply OFF sequence

The reset operation is required first in order to cut off the V_1 to V_4 and V_{LCD} from the LSI, and then the input voltage for the voltage booster (V_{EE}) and the V_{DD} can be turned off.

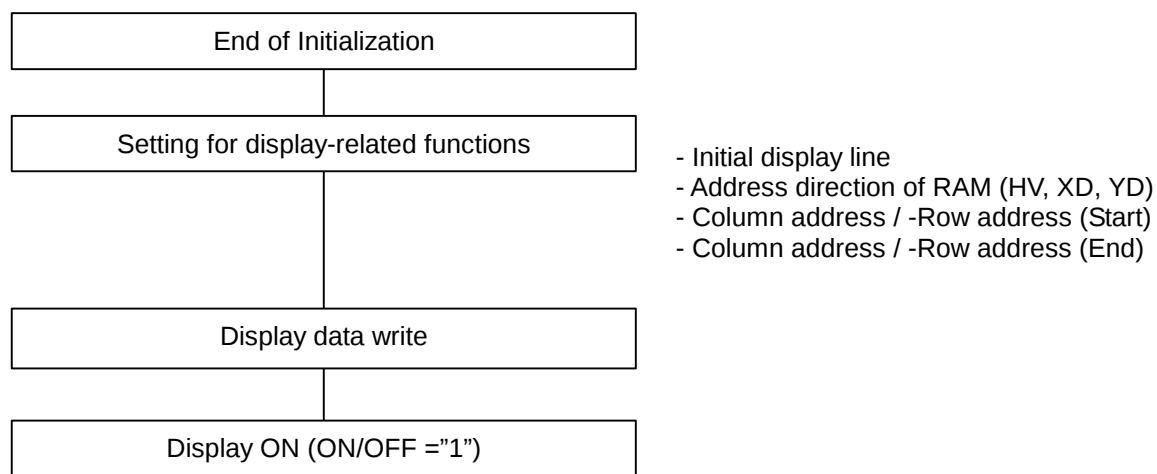
In case that the V_{EE} and V_{DD} are supplied from deferent voltage sources, the V_{EE} is required to be turned off first, and then the V_{DD} can be turned off.

(30) Referential instruction sequences

(30-1) Initialization in using the internal power supply circuits



(30-2) Display data writing

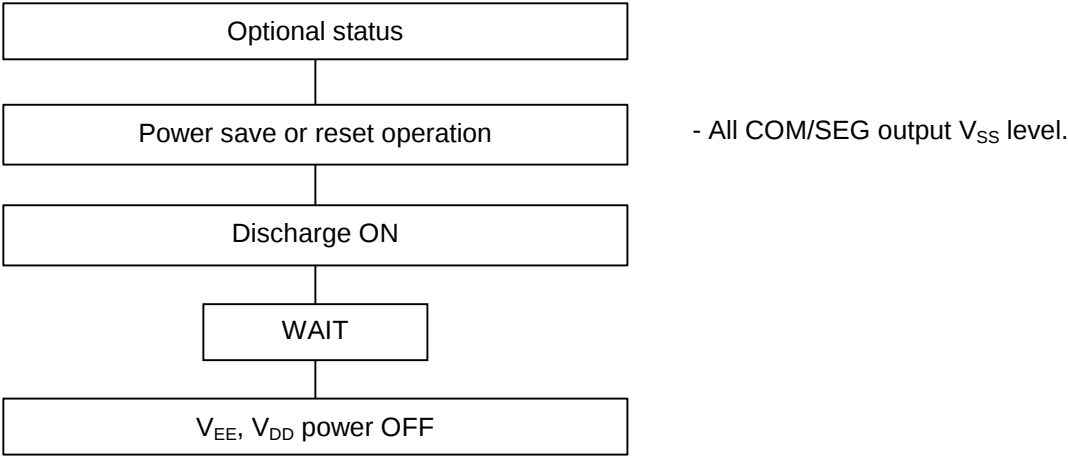


*: Before display data write / read operation, the address directions should be set first , then Column address set / Row address set of start point and end are set in order. (Display data write / read for whole display area or a portion requires the same procedure as above.)

To avoid incorrect data writing into registers by noise and so forth, the written data from registers should be checked after write operation.



(30-3) Power OFF



(31) Instruction table

Instruction Table (1)

Instructions	Code (80 series MPU I/F)							Code								Functions
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Display data write	0	0	1	0	0/1	0/1	0/1	Write Data								Write display data to DDRAM
Display data read	0	0	0	1	0/1	0/1	0/1	Read Data								Read display data from DDRAM
column address (Lower) [0 _H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	DDRAM column address
column address (Upper) [1 _H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	DDRAM column address
row address (Lower) [2 _H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	DDRAM row address
row address (Upper) [3 _H]	0	1	1	0	0	0	0	0	0	1	1	*	AY6	AY5	AY4	DDRAM row address
Initial display line (Lower) [4 _H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Sets row address corresponding to initial COM line (scan-starting line)
Initial display line (Upper) [5 _H]	0	1	1	0	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Sets row address corresponding to initial COM line (scan-starting line)
N-line inversion (Lower) [6 _H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Sets the number of N-line inversion
N-line inversion (Upper) [7 _H]	0	1	1	0	0	0	0	0	1	1	1	*	N6	N5	N4	Sets the number of N-line inversion
Display control (1) [8 _H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/OFF	SHIFT: Common direction MON: Gradation or B/W display mode ALLON: All pixels ON/OFF ON/OFF: Display ON/OFF
Display control (2) [9 _H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	*	REV: Reverse display ON/OFF NLIN: N-line inversion ON/OFF, SWAP: SWAP mode ON/OFF
Increment control [A _H]	0	1	1	0	0	0	0	1	0	1	0	AIM	HV	XD	YD	AIM: Read-modify-write ON/OFF HV: Increment / Decrement direction XD: Column Increment / Decrement set YD: Row Increment / Decrement set
Power control [B _H]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON: Voltage followers ON/OFF HALT: Power save ON/OFF DCON: Voltage booster ON/OFF ACL: Reset
Duty cycle ratio [C _H]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Sets LCD duty cycle ratio
Boost level [D _H]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Sets boost level
LCD bias ratio [E _H]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Sets LCD bias ratio
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [] : Instruction register address

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (2)

Instructions	Code (80 series MPU I/F)							Code								Functions
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette A0/A8 (Lower) [0 _H]	0	1	1	0	0	0	1	0	0	0	0	PA03/PA83	PA02/PA82	PA01/PA81	PA00/PA80	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A0/A8 (Upper) [1 _H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/PA84	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A1/A9 (Lower) [2 _H]	0	1	1	0	0	0	1	0	0	1	0	PA13/PA93	PA12/PA92	PA11/PA91	PA10/PA90	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A1/A9 (Upper) [3 _H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/PA94	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A2/A10 (Lower) [4 _H]	0	1	1	0	0	0	1	0	1	0	0	PA23/PA103	PA22/PA102	PA21/PA101	PA20/PA100	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A2/A10 (Upper) [5 _H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/PA104	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A3/A11 (Lower) [6 _H]	0	1	1	0	0	0	1	0	1	1	0	PA33/PA113	PA32/PA112	PA31/PA111	PA30/PA110	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A3/A11 (Upper) [7 _H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/PA114	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A4/A12 (Lower) [8 _H]	0	1	1	0	0	0	1	1	0	0	0	PA43/PA123	PA42/PA122	PA41/PA121	PA40/PA120	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A4/A12 (Upper) [9 _H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/PA124	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A5/A13 (Lower) [A _H]	0	1	1	0	0	0	1	1	0	1	0	PA53/PA133	PA52/PA132	PA51/PA131	PA50/PA130	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A5/A13 (Upper) [B _H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/PA134	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A6/A14 (Lower) [C _H]	0	1	1	0	0	0	1	1	1	0	0	PA63/PA143	PA62/PA142	PA61/PA141	PA60/PA140	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
Gradation palette A6/A14 (Upper) [D _H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/PA144	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [] : Instruction register address

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (3)

Instructions	Code (80 series MPU I/F)							Code								Functions
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette A7/A15 (Lower) [0 _H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette A7/A15 (Upper) [1 _H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette B0/B8 (Lower) [2 _H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B0/B8 (Upper) [3 _H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B1/B9 (Lower) [4 _H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B1/B9 (Upper) [5 _H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B2/B10 (Lower) [6 _H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B2/B10 (Upper) [7 _H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B3/B11 (Lower) [8 _H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B3/B11 (Upper) [9 _H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B4/B12 (Lower) [A _H]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B4/B12 (Upper) [B _H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B5/B13 (Lower) [C _H]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
Gradation palette B5/B13 (Upper) [D _H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [] : Instruction register address

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (4)

Instructions	Code (80 series MPU I/F)							Code								Functions
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette B6/B14 (Lower) [0 _H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B6/B14 (Upper) [1 _H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B7/B15 (Lower) [2 _H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette B7/B15 (Upper) [3 _H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette C0/C8 (Lower) [4 _H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C0/C8 (Upper) [5 _H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C1/C9 (Lower) [6 _H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C1/C9 (Upper) [7 _H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C2/C10 (Lower) [8 _H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C2/C10 (Upper) [9 _H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C3/C11 (Lower) [A _H]	0	1	1	0	0	1	1	1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C3/C11 (Upper) [B _H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C4/C12 (Lower) [C _H]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
Gradation palette C4/C12 (Upper) [D _H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [] : Instruction register address

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (5)

Instructions	Code (80 series MPU I/F)							Code								Functions
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette C5/C13 (Lower) [0 _H]	0	1	1	0	1	0	0	0	0	0	0	PC53/PC133	PC52/PC132	PC51/PC131	PC50/PC130	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C5/C13 (Upper) [1 _H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/PC134	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C6/C14 (Lower) [2 _H]	0	1	1	0	1	0	0	0	0	1	0	PC63/PC143	PC62/PC142	PC61/PC141	PC60/PC140	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C6/C14 (Upper) [3 _H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/PC154	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C7/C15 (Lower) [4 _H]	0	1	1	0	1	0	0	0	1	0	0	PC73/PC153	PC72/PC152	PC71/PC151	PC70/PC150	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Gradation palette C7/C15 (Upper) [5 _H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/PC154	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Initial COM line [6 _H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Sets scan-starting common driver
Display control Signal/Duty Select [7 _H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : CL, FLM, FR, CLK signal DSE : Duty select
Gradation mode control [8 _H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM : Variable 16 Gradation Mode Stability 8 Gradation Mode C256 : 256 Color Mode FDC : Boost Clock
Data bus length [9 _H]	0	1	1	0	1	0	0	1	0	0	1	*	ABS	CKS	WLS	ABS : 12bits RAM Data Select CKS : OSC Select WLS : Data Length at Data Access
EVR control (Lower) [A _H]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Sets EVR level (Lower bit)
EVR control (Upper) [B _H]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Sets EVR level (Upper bit)
Frequency control [D _H]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Controls oscillation frequency
Discharge ON/OFF [E _H]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge the electric charge in capacitors on V ₁ to V ₄ and V _{LCD}
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag
Instruction register address [C _H]	0	1	1	0	1	0	0	1	1	0	0	Reading register address				Sets instruction register address
Instruction register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Read out instruction register data

Note 1) * : Don't care.

Note 2) [] : Instruction register address

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Note 4) CKS=0: Internal oscillation mode (default)
CKS=1: External oscillation mode

Instruction Table (6)

Instructions	Code (80 series MPU I/F)							Code								Functions
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Window end column address (Lower) [0 _H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Sets column address for end point
Window end column address (Upper) [1 _H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Sets column address for end point
Window end row address (Lower) [2 _H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Sets row address for end point
Window end row address (Upper) [3 _H]	0	1	1	0	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Sets row address for end point
Initial reverse line (Lower) [4 _H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Sets address for reverse line
Initial reverse line (Upper) [5 _H]	0	1	1	0	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Sets address for reverse line
Last reverse line (Lower) [6 _H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Sets address for reverse line
Last reverse line (Upper) [7 _H]	0	1	1	0	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Sets address for reverse line
Reverse line display ON/OFF [8 _H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink type setting LREV : Reverse line display ON/OFF
Gradation palette setting control / Icon SEG address [9 _H]	0	1	1	0	1	0	1	1	0	0	1	*	*	DMY	PS	PS : gradation setting DMY : Icon SEG address set
PWM control [A _H]	0	1	1	0	1	0	1	1	0	1	0	PWM _S	PWM _A	PWM _B	PWM _C	Sets PWM mode
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag

Note 1) * : Don't care.

Note 2) [] : Instruction register address

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

(32) Instruction descriptions

This chapter provides detail description of the instructions, registers, their settings and programming examples. The non-existent instruction codes in the instruction tables (1), (2)...(6) are required not to be programmed.

(32-1) Display data write

The "Display data write" instruction is used to write 8-bit display data into the DDRAM.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	0	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display data							

(32-2) Display data read

The "Display data read" instruction is used to read out 8-bit display data from the DDRAM, where the column address and row address are required to be specified beforehand by the "column address" and "row address" instructions. The dummy read is required just after the "column address" and "row address" instructions.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	0	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display data							

(32-3) Column address

The "column address" instruction is used to specify the column address for the display data read and write operations. It includes dual instructions for lower 4-bit and upper 4-bit data. The instruction for the lower 4-bit data is required to be executed first.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	AX ₃	AX ₂	AX ₁	AX ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	AX ₇	AX ₆	AX ₅	AX ₄

(32-4) Row address

The "row address" instruction is used to specify the row address for the display data read and write operations. It includes dual instructions for lower 4-bit and upper 3-bit data. The instruction for the lower 4-bit data is required to be executed first.

The row address can be specified in between 00_H and 7F_H. The setting for the non-existence row address between 80_H and FF_H is prohibited.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	AY ₃	AY ₂	AY ₁	AY ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	AY ₆	AY ₅	AY ₄

(32-5) Initial display line

The "Initial display line" instruction is used to specify the line address corresponding to the initial COM line. The initial COM line indicates the common driver that starts scanning the display data, which is specified by the "Initial COM line" instruction.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LA ₃	LA ₂	LA ₁	LA ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LA ₆	LA ₅	LA ₄

LA ₆	LA ₅	LA ₄	LA ₃	LA ₂	LA ₁	LA ₀	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
⋮							⋮
1	1	1	1	1	1	1	127

(32-6) N-line inversion

The "N-line inversion" instruction is used to control the alternate rates of the liquid crystal direction. It is programmed to select the N value between 2 and 128, so that the FR signal toggles once every N frames by setting "1" into the "NLIN" register in the "Display control (2)" instruction. In case that the N-line inversion is disabled by setting "0" into "NLIN" register, the FR signal toggles by the frame.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	N3	N2	N1	N0

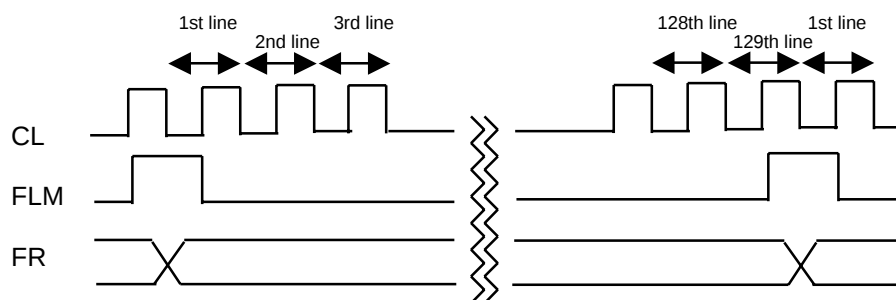
$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	N6	N5	N4

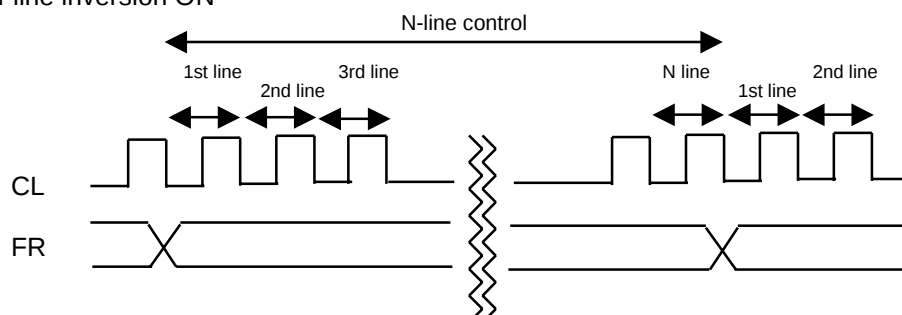
N6	N5	N4	N3	N2	N1	N0	N value
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
⋮							⋮
0	1	0	0	0	0	0	128

● N-line Inversion Timing (1/129 duty cycle ratio)

N-line inversion OFF



N-line inversion ON



(32-7) Display control (1)

The "Display control (1)" instruction is used to control the display conditions for the "Display ON/OFF", "All pixels ON/OFF", Display mode" and "Common direction" registers.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

● ON/OFF register

ON/OFF=0 : Display OFF (All COM/SEG output V_{ss} level.)
ON/OFF=1 : Display ON

● All ON register

The "All pixels ON/OFF" register is used to turn on all pixels without changing the display data in the DDRAM. The setting for the "All pixels ON/OFF" register has a priority over the "Reverse display ON/OFF" register.

ALLON=0 : Normal
ALLON=1 : All pixels turn on.

● MON register

MON=0 : Gradation mode
MON=1 : B&W mode

● SHIFT register

SHIFT=0 : COM₀ → COM₁₂₇
SHIFT=1 : COM₁₂₇ → COM₀

(32-8) Display control (2)

The "Display control (2)" instruction is used to control the display conditions for the "SWAP mode ON/OFF", "N-line inversion ON/OFF" and "Reverse display ON/OFF".

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	REV	NLIN	SWAP	*

● SWAP register

The "SWAP" register is used to reverse the arrangement for the display data in the DDRAM.

SWAP=0 : SWAP mode OFF (Normal)
 SWAP=1 : SWAP mode ON

	SWAP="0"	SWAP="1"
Write data	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀
RAM data	D ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	d ₀ d ₁ d ₂ d ₃ d ₄ d ₅ d ₆ d ₇
Read data	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀

● NLIN register

The "NLIN" is used to enable or disable the N-line inversion.

NLIN=0 : N-line inversion OFF (The FR signal toggles by the frame.)
 NLIN=1 : N-line inversion ON (The FR signal toggles once every N frames.)

● REV register

The "REV" register is used to enable or disable the reverse display mode that reverses the polarity of the display data without changing the display data in the DDRAM.

REV=0 : Reverse display mode OFF
 REV=1 : Reverse display mode ON

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(32-9) Increment control

The "Increment control" instruction is used to control the conditions for the increment mode. In the auto-increment mode, the DDRAM address is automatically incremented (+1) whenever the DDRAM is accessed by the "Display data write" and "Display data read" instructions, so that it is possible to continuously access to the DDRAM without executing the "column address" and "row address" instructions after each "Display data write" or "Display data read" instruction. The settings for the "AIM", "HV", "XD" and "YD" registers are listed in the following tables.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	AIM	HV	XD	YD

● AIM, HV, XD and YD registers

AIM	Increment mode	Note
0	Auto-increment for both of the display data read and write operations	1
1	Auto-increment for the display write operation (Read modify write)	2

Note 1) It is valid during continuing to write or read serial address area.

Note 2) It is valid at writing modified data that read, write, and read every address.

HV	XD	YD	Increment / Decrement mode / Scanning Direction
0	0	0	Column increment / Row increment / Horizontal direction
0	0	1	Column increment / Row decrement / Horizontal direction
0	1	0	Column decrement / Row increment / Horizontal direction
0	1	1	Column decrement / Row decrement / Horizontal direction
1	0	0	Column increment / Row increment / Vertical direction
1	0	1	Column increment / Row decrement / Vertical direction
1	1	0	Column decrement / Row increment / Vertical direction
1	1	1	Column decrement / Row decrement / Vertical direction

For the window area designation, the address directions of RAM (HV, XD, YD) must be set first, and Column address and Row of Start point must be set second, Column address and Row of Stop point must be set third, then RAM should be accessed. Low address must be set first and High address must be set second in all of addresses. The directions of HV, XD, YD should be check to keep the area in RAM.

(32-10) Power control

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	AMPON	HALT	DCON	ACL

● ACL register

The "ACL" register is used to initialize the internal power supply circuits. It is available only in the master mode.

ACL=0 : Initialization OFF (Normal)
 ACL=1 : Initialization ON

When the data in the "ACL register" is read out by the "Instruction register read" instruction, the read-out data is "1" during the initialization and "0" after the initialization. This initialization is performed using the internal reset signal produced by 2 clocks on the OSC₁. For this reason, the wait time for 2 clocks on the OSC₁ is required until the next instruction after the initialization by programming "ACL" register.

● DCON register

The "DCON" register is used to enable or disable the voltage booster.

DCON=0 : Voltage booster OFF
 DCON=1 : Voltage booster ON

● HALT register

The "HALT" register is used to enable or disable the power save mode. It is possible to reduce the operating current down to the stand-by level in the power save mode. The internal status in the power save mode is listed below.

HALT=0 : Power save OFF (Normal)
 HALT=1 : Power save ON

Internal status in the power save mode

- The oscillation circuits and internal power supply circuits are halted.
- All segment and common drivers output V_{SS} level.
- The display data in the DDRAM is maintained.
- The operational modes before the power save mode are maintained.
- The V₁ to V₄ and V_{LCD} are in the high impedance.
- The clock input into the OSC₁ is inhibited.

In the power save ON sequence, it is required that the "Display OFF" instruction is executed before the "Power save ON" instruction, so that all common and segment drivers output V_{SS} level. And in the power save OFF sequence, it is required that the "Power save OFF" instruction is executed first and then the "Display ON" instruction is executed. If the "Power save OFF" instruction is executed in the display ON status, unexpected pixels may be instantly turned on.

● AMPON register

The "AMPON" register is used to enable or disable the voltage followers, voltage regulator and EVR.

AMPON=0 : The voltage followers, voltage regulator and EVR OFF
 AMPON=1 : The voltage followers, voltage regulator and EVR ON

(32-11) Duty cycle ratio

The "Duty cycle ratio" instruction is used to select the LCD duty cycle ratio for the partial display function. The partial display function specifies the partial display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage, so that it is possible to display a time and calendar in the extremely low power consumption.

It can be also programmed to select not only the duty cycle ratio but also the LCD bias ratio, boost level and EVR value by the instructions so that it is possible to optimize the LSI conditions in accordance with the display.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	DS ₃	DS ₂	DS ₁	DS ₀

DS ₃	DS ₂	DS ₁	DS ₀	Duty cycle ratio
0	0	0	0	Row way 128 dots display, 1/129 Duty
0	0	0	1	Row way 120 dots display, 1/121 Duty
0	0	1	0	Row way 112 dots display, 1/113 Duty
0	0	1	1	Row way 104 dots display, 1/105 Duty
0	1	0	0	Row way 96 dots display, 1/97 Duty
0	1	0	1	Row way 88 dots display, 1/89 Duty
0	1	1	0	Row way 80 dots display, 1/81 Duty
0	1	1	1	Row way 72 dots display, 1/73 Duty
1	0	0	0	Row way 64 dots display, 1/75 Duty
1	0	0	1	Row way 56 dots display, 1/57 Duty
1	0	1	0	Row way 48 dots display, 1/49 Duty
1	0	1	1	Row way 40 dots display, 1/41 Duty
1	1	0	0	Row way 32 dots display, 1/33 Duty
1	1	0	1	Row way 24 dots display, 1/25 Duty
1	1	1	0	Row way 16 dots display, 1/17 Duty
1	1	1	1	Inhibited

All of duty value are decreased "1" by Duty selection set (DSE=1).

Ex.) In case of (DS₃,DS₂,DS₁,DS₀)=(0,0,0,0)

DSE="0" :1/129Duty

DSE="1" :1/128Duty

In period of last Common driving, all of Commons are not selected and Segment outputs are not change from previous condition.

Ex.) Conditions of Commons and segments at 129th line in case of 1/129 duty

COM output : All of Commons are not selected

SEG output : Not change from previous condition (same 128 line).

(32-12) Boost level

The "Boost level" is used to select the multiple for the voltage booster for the partial display function.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	VU ₂	VU ₁	VU ₀

VU ₂	VU ₁	VU ₀	Boost level
0	0	0	1-time (No boost)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	6-time
1	1	0	Inhibited
1	1	1	Inhibited

(32-13) LCD bias ratio

The "LCD bias ratio" is used to select the LCD bias ratio for the partial display function.

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	B ₂	B ₁	B ₀

B ₂	B ₁	B ₀	LCD bias ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

(32-14) RE flag

The "RE flag" registers are used to determine the contents for the RE registers (RE₂, RE₁ and RE₀) in order that it is possible to access to the instruction registers.

The data in the "TST₀" register must be "0", which is used only for maker tests.

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀

(32-15) Gradation palette A, B and C

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA ₀₃ / PA ₈₃	PA ₀₂ / PA ₈₂	PA ₀₁ / PA ₈₁	PA ₀₀ / PA ₈₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA ₀₄ / PA ₈₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PA ₁₃ / PA ₉₃	PA ₁₂ / PA ₉₂	PA ₁₁ / PA ₉₁	PA ₁₀ / PA ₉₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PA ₁₄ / PA ₉₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PA ₂₃ / PA ₁₀₃	PA ₂₂ / PA ₁₀₂	PA ₂₁ / PA ₁₀₁	PA ₂₀ / PA ₁₀₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PA ₂₄ / PA ₁₀₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PA ₃₃ / PA ₁₁₃	PA ₃₂ / PA ₁₁₂	PA ₃₁ / PA ₁₁₁	PA ₃₀ / PA ₁₁₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PA ₃₄ / PA ₁₁₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PA ₄₃ / PA ₁₂₃	PA ₄₂ / PA ₁₂₂	PA ₄₁ / PA ₁₂₁	PA ₄₀ / PA ₁₂₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PA ₄₄ / PA ₁₂₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PA ₅₃ / PA ₁₃₃	PA ₅₂ / PA ₁₃₂	PA ₅₁ / PA ₁₃₁	PA ₅₀ / PA ₁₃₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PA ₅₄ / PA ₁₃₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PA ₆₃ / PA ₁₄₃	PA ₆₂ / PA ₁₄₂	PA ₆₁ / PA ₁₄₁	PA ₆₀ / PA ₁₄₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PA ₆₄ / PA ₁₄₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA ₇₃ / PA ₁₅₃	PA ₇₂ / PA ₁₅₂	PA ₇₁ / PA ₁₅₁	PA ₇₀ / PA ₁₅₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA ₇₄ / PA ₁₅₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB ₀₃ / PB ₈₃	PB ₀₂ / PB ₈₂	PB ₀₁ / PB ₈₁	PB ₀₀ / PB ₈₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB ₀₄ / PB ₈₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PB ₁₃ / PB ₉₃	PB ₁₂ / PB ₉₂	PB ₁₁ / PB ₉₁	PB ₁₀ / PB ₉₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PB ₁₄ / PB ₉₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PB ₂₃ / PB ₁₀₃	PB ₂₂ / PB ₁₀₂	PB ₂₁ / PB ₁₀₁	PB ₂₀ / PB ₁₀₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PB ₂₄ / PB ₁₀₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PB ₃₃ / PB ₁₁₃	PB ₃₂ / PB ₁₁₂	PB ₃₁ / PB ₁₁₁	PB ₃₀ / PB ₁₁₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PB ₃₄ / PB ₁₁₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PB ₄₃ / PB ₁₂₃	PB ₄₂ / PB ₁₂₂	PB ₄₁ / PB ₁₂₁	PB ₄₀ / PB ₁₂₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PB ₄₄ / PB ₁₂₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PB ₅₃ / PB ₁₃₃	PB ₅₂ / PB ₁₃₂	PB ₅₁ / PB ₁₃₁	PB ₅₀ / PB ₁₃₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PB ₅₄ / PB ₁₃₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PB ₆₃ / PB ₁₄₃	PB ₆₂ / PB ₁₄₂	PB ₆₁ / PB ₁₄₁	PB ₆₀ / PB ₁₄₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PB ₆₄ / PB ₁₄₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB ₇₃ / PB ₁₅₃	PB ₇₂ / PB ₁₅₂	PB ₇₁ / PB ₁₅₁	PB ₇₀ / PB ₁₅₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB ₇₄ / PB ₁₅₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC ₀₃ / PC ₈₃	PC ₀₂ / PC ₈₂	PC ₀₁ / PC ₈₁	PC ₀₀ / PC ₈₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC ₀₄ / PC ₈₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PC ₁₃ / PC ₉₃	PC ₁₂ / PC ₉₂	PC ₁₁ / PC ₉₁	PC ₁₀ / PC ₉₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PC ₁₄ / PC ₉₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PC ₂₃ / PC ₁₀₃	PC ₂₂ / PC ₁₀₂	PC ₂₁ / PC ₁₀₁	PC ₂₀ / PC ₁₀₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PC ₂₄ / PC ₁₀₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PC ₃₃ / PC ₁₁₃	PC ₃₂ / PC ₁₁₂	PC ₃₁ / PC ₁₁₁	PC ₃₀ / PC ₁₁₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PC ₃₄ / PC ₁₁₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PC ₄₃ / PC ₁₂₃	PC ₄₂ / PC ₁₂₂	PC ₄₁ / PC ₁₂₁	PC ₄₀ / PC ₁₂₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PC ₄₄ / PC ₁₂₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PC ₅₃ / PC ₁₃₃	PC ₅₂ / PC ₁₃₂	PC ₅₁ / PC ₁₃₁	PC ₅₀ / PC ₁₃₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PC ₅₄ / PC ₁₃₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PC ₆₃ / PC ₁₄₃	PC ₆₂ / PC ₁₄₂	PC ₆₁ / PC ₁₄₁	PC ₆₀ / PC ₁₄₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PC ₆₄ / PC ₁₄₄

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC ₇₃ / PC ₁₅₃	PC ₇₂ / PC ₁₅₂	PC ₇₁ / PC ₁₅₁	PC ₇₀ / PC ₁₅₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC ₇₄ / PC ₁₅₄

Gradation Level Table

(PA_j, PB_j, PC_j, j=0–15)

Palette Value	Gradation Level	Note	Palette Value	Gradation Level	Note
0 0 0 0 0	0/31	Gradation Palette 0 Initial Value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Gradation Palette 8 Initial Value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Gradation Palette 1 Initial Value	1 0 0 1 1	19/31	Gradation Palette 9 Initial Value
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Gradation Palette 2 Initial Value	1 0 1 0 1	21/31	Gradation Palette 10 Initial Value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Gradation Palette 3 Initial Value	1 0 1 1 1	23/31	Gradation Palette 11 Initial Value
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Gradation Palette 4 Initial Value	1 1 0 0 1	25/31	Gradation Palette 12 Initial Value
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Gradation Palette 5 Initial Value	1 1 0 1 1	27/31	Gradation Palette 13 Initial Value
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Gradation Palette 6 Initial Value	1 1 1 0 1	29/31	Gradation Palette 14 Initial Value
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Gradation Palette 7 Initial Value	1 1 1 1 1	31/31	Gradation Palette 15 Initial Value

(32-16) Initial COM line

The "Initial COM line" instruction is used to specify the common driver that starts scanning the display data. The line address, corresponding to the initial COM line, is specified by the "Initial display line" instruction.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	SC ₃	SC ₂	SC ₁	SC ₀

SC3	SC2	SC1	SC0	Initial COM line (SHIFT=0)	Initial COM line (SHIFT=1)
0	0	0	0	COM ₀	COM ₁₂₇
0	0	0	1	COM ₄	COM ₁₂₃
0	0	1	0	COM ₈	COM ₁₁₉
0	0	1	1	COM ₁₆	COM ₁₁₁
0	1	0	0	COM ₂₄	COM ₁₀₃
0	1	0	1	COM ₃₂	COM ₉₅
0	1	1	0	COM ₄₀	COM ₈₇
0	1	1	1	COM ₄₈	COM ₇₉
1	0	0	0	COM ₅₆	COM ₇₁
1	0	0	1	COM ₆₄	COM ₆₃
1	0	1	0	COM ₇₂	COM ₅₅
1	0	1	1	COM ₈₀	COM ₄₇
1	1	0	0	COM ₈₈	COM ₃₉
1	1	0	1	COM ₉₆	COM ₃₁
1	1	1	0	COM ₁₀₄	COM ₂₃
1	1	1	1	COM ₁₁₂	COM ₁₅

SHIFT=0: Positive scan direction
SHIFT=1: Negative scan direction

(for instance, COM₀ → COM₁₂₇)
(for instance, COM₁₂₇ → COM₀)

(32-17) Display control signal / Duty select

CL, FLM, FR, and CLK signal outputs control ON/OFF and Duty select.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	DSE	SON

SON=0: CL, FLM, FR, and CLK outputs level "0".
SON=1: CL, FLM, FR, and CLK outputs are active.

DSE=0: Refer the table of (32-11) Duty cycle ratio. (Default)
DSE=1: The duty ratio is set by the value subtracted "1" from the content of the table.

(32-18) Gradation mode control

The "Gradation mode control" is selecting the gradation mode, selecting the 256-color mode, and setting boost clock.

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PWM	C256	FDC1	FDC2

● PWM register

- PWM=0: Variable gradation mode
(16-gradation levels out of a palette consisting of 32-gradation levels)
- PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

● C256 register

- C256=0 Variable gradation mode
(16-gradation levels out of a palette consisting of 32-gradation levels.)
- C256=1 256-color mode
(8-gradation levels out of a palette consisting of 32-gradation levels.)
(4-gradation levels out of a palette consisting of 32-gradation levels at the palette B.)

● FDC1 and FDC2 register

FDC1	FDC2	Boost Clock
0	0	×1
0	1	×2
1	0	×4
1	1	×1/2

(32-19) Data bus length

The "Data bus length" instruction is used to select the 8- or 16- bit data bus length and determine the internal or external oscillation. In the 16-bit data bus mode, not only the display data but also the instruction data is required to be transferred by 16-bit data (D_{15} to D_0). However, in case of the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. In case of the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	ABS	CKS	WLS

● ABS register

ABS=0: Normal Mode

ABS=1: ABS Mode

● WLS register

WLS=0: 8-bit data bus length

WLS =1: 16-bit data bus length

● CKS register

CKS =0: Internal oscillation

(The OSC_1 terminal must be fixed "1" or "0".)

CKS =1: External oscillation

(By the external clock into the OSC_1 or external resister between the OSC_1 and OSC_2 . OSC_2 should be open when clock is inputted from OSC_1 .)

(32-20)EVR control

The “EVR control” instruction is used to fine-tune the LCD driving voltage (V_{LCD}) so that it is possible to optimize the contrast level for the display.

The “EVR control” instruction requires to be programmed by the upper 3-bit data first and then lower 4-bit data, where programming the only upper 3-bit data has not enabled it, so that it is possible to prevent unexpected high voltage for the V_{LCD} .

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	DV ₆	DV ₅	DV ₄

DV ₆	DV ₅	DV ₄	DV ₃	DV ₂	DV ₁	DV ₀	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

The V_{LCD} is calculated by the following equation.

$$V_{LCD} [V] = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127$$

$$V_{BA} = V_{EE} \times 0.9$$

$$V_{REG} = V_{REF} \times N$$

V_{BA} : Output voltage of the reference voltage generator

V_{REF} : Input voltage of the voltage regulator

V_{REG} : Output voltage of the voltage regulator

N : Register value for the voltage booster

M : Register value for the EVR

(32-21) Frequency control

The "Frequency control" instruction is used to control the frame frequency for a LCD panel.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	Rf ₂	Rf ₁	Rf ₀

- Rfx register (x=0, 1, 2)

The "Rfx" register is used to determine the feed back resistor value for the internal oscillator in order that it is possible to adjust the frame frequency.

Rf 2	Rf 1	Rf 0	Feedback resistor value
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	0.7 x reference value
1	1	0	1.3 x reference value
1	1	1	Inhibited

(32-22) Discharge ON/OFF

The "Discharge ON/OFF" instruction is used to enable or disable the discharge circuits, so that it is possible to prevent unexpected pixels turned on just after the internal or external power supply is turned off. During the discharge operation, do not supply the power neither from an internal or external power supplies to the LSI.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	*	DIS2	DIS

DIS=0: Discharge OFF: Capacitors for V_{LCD}, V₁, V₂, V₃ and V₄

DIS=1: Discharge ON : Capacitors for V_{LCD}, V₁, V₂, V₃ and V₄

DIS2=0: Discharge OFF: Resistance between V_{OUT} and V_{EE}

DIS2=1: Discharge ON : Resistance between V_{OUT} and V_{EE}

*In the power on, 100kΩ (Typ.) resistance is connected between V_{OUT} and V_{EE}.

(32-23) Instruction register address

The "Instruction register address" is used to specify the instruction register address, so that it is possible to read out the contents of the instruction registers in combination with the "Instruction register read" instruction.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	RA ₃	RA ₂	RA ₁	RA ₀

(32-24) Instruction register read

The "Instruction register read" instruction is used to read out the contents of the instruction register in combination with the "Instruction register address" instruction.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
*	*	*	*	Internal register data read			

(32-25) Window end column address

The "Window end column address" is used to specify the column address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 4-bit data can be programmed.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	EX ₃	EX ₂	EX ₁	EX ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	EX ₇	EX ₆	EX ₅	EX ₄

(32-26) Window end row address set

The "Window end row address" is used to specify the row address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 3-bit data can be programmed.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	EY ₃	EY ₂	EY ₁	EY ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	EY ₆	EY ₅	EY ₄

(32-27) Initial reverse line

The "Initial reverse line" instruction is used to specify the initial reverse line address for the reverse line display. The lower 4-bit data is required to be programmed first and then the upper 3-bit data can be programmed. It can be programmed in between 00_H and 7F_H and the line address beyond 7F_H is inhibited. The address relationship: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LS ₃	LS ₂	LS ₁	LS ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LS ₆	LS ₅	LS ₄

(32-28) Last reverse line

The "Last reverse line" instruction is used to specify the last reverse line address for the reverse line display. The lower 4-bit data is required to be programmed first and then the upper 3-bit data can be programmed. It can be programmed in between 00_H and 7F_H and the line address beyond 7F_H is inhibited. The address relationship: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	LE ₃	LE ₂	LE ₁	LE ₀

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	LE ₆	LE ₅	LE ₄

(32-29) Reverse line display ON/OFF

The "Reverse line display ON/OFF" is used to enable or disable the reverse line display for the blink operation and determine the reverse line display mode.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	*	*	BT	LREV

● LREV register

The "LREV" register is used to enable or disable the reverse line display.

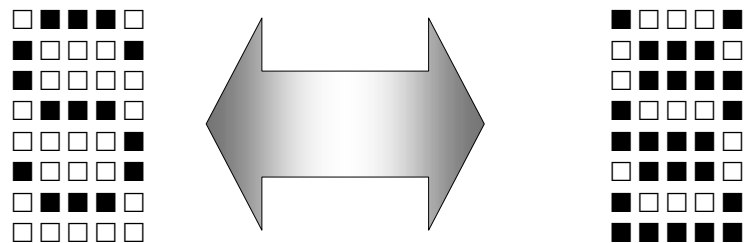
LREV =0: Reverse line display OFF (Normal)

LREV =1: Reverse line display ON

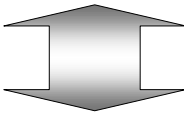
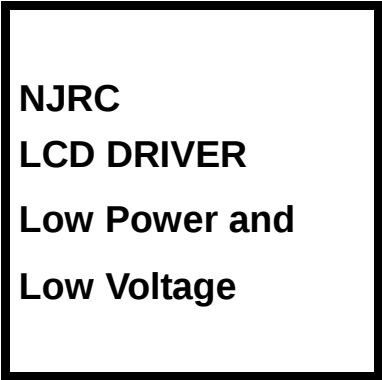
- BT register
The “BT” register is used to determine the reverse line display mode in the reverse line display ON (LREV=1) status.

BT =0: Normal reverse line display
BT =1: Blink once every 32 frames

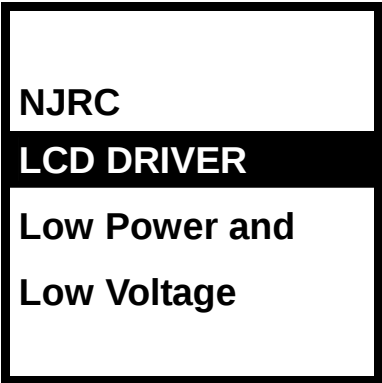
Display examples in the LREV=“1” and BT=“1”



Blink once every 32 frames



Blink once every 32 frames



←Initial reverse line address

←Last reverse line address

(32-30) Gradation palette setting control / Icon SEG address set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	DMY	PS

- PS register

PS=0: Lower 8 Gradation setting

PS=1: Upper 8 Gradation setting

- DMY register

Although segment drivers in normal condition output LCD driving voltage corresponding to data in Display data RAM, Icon segment driver output LCD driving voltage corresponding to registers. The 24 bits register corresponds to SEGSA0 ~ SEGSA1, SEGSB0 ~ SEGSB1, SEGSC0 ~ SEGSC1.

DMY=0: Normal RAM access

DMY=1: Icon segment driver RAM access

(32-31) PWM control

The "PWM control" is used to determine the PWM type for the segment waveforms, where the type can be specified for each of the SEGAI, SEGBi and SEGCi (i=0-127) drivers.

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PWMS	PWMA	PWMB	PWMC

- PWMS register

PWMS=0: Type 1

PWMS=1: Type 2

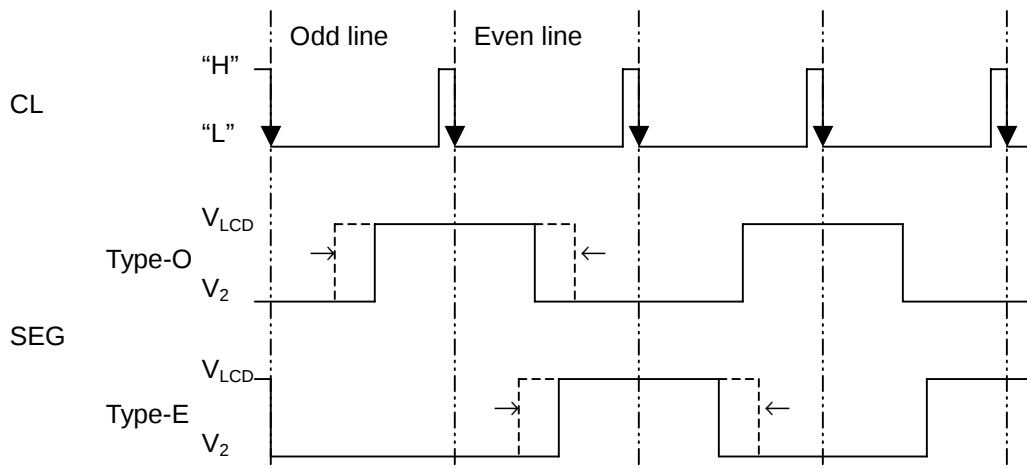
- PWMA, B and C registers

The "PWMA, PWMB and PWMC" registers are used to select the type 1-O or type 1-E.

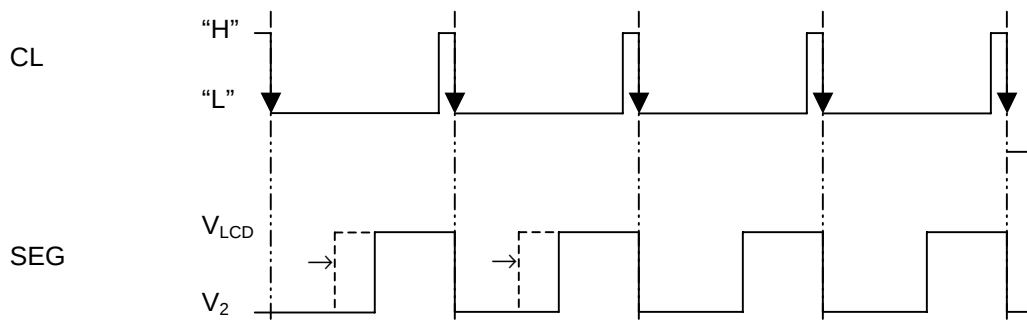
PWMZ=0 (Z=A, B and C): Type 1-O

PWMZ=1 (Z=A, B and C): Type 1-E

PWM type1 (PWMS="0")



PWM type2 (PWMS="1")



(33) The relationship between Common driver and row address

The row address assignment for the common driver can be programmed by the "SHIF" register in the "Display control (1)", and "Duty cycle ratio", "Initial display line" and "Initial COM line" instructions.

- When initial display line is "0"

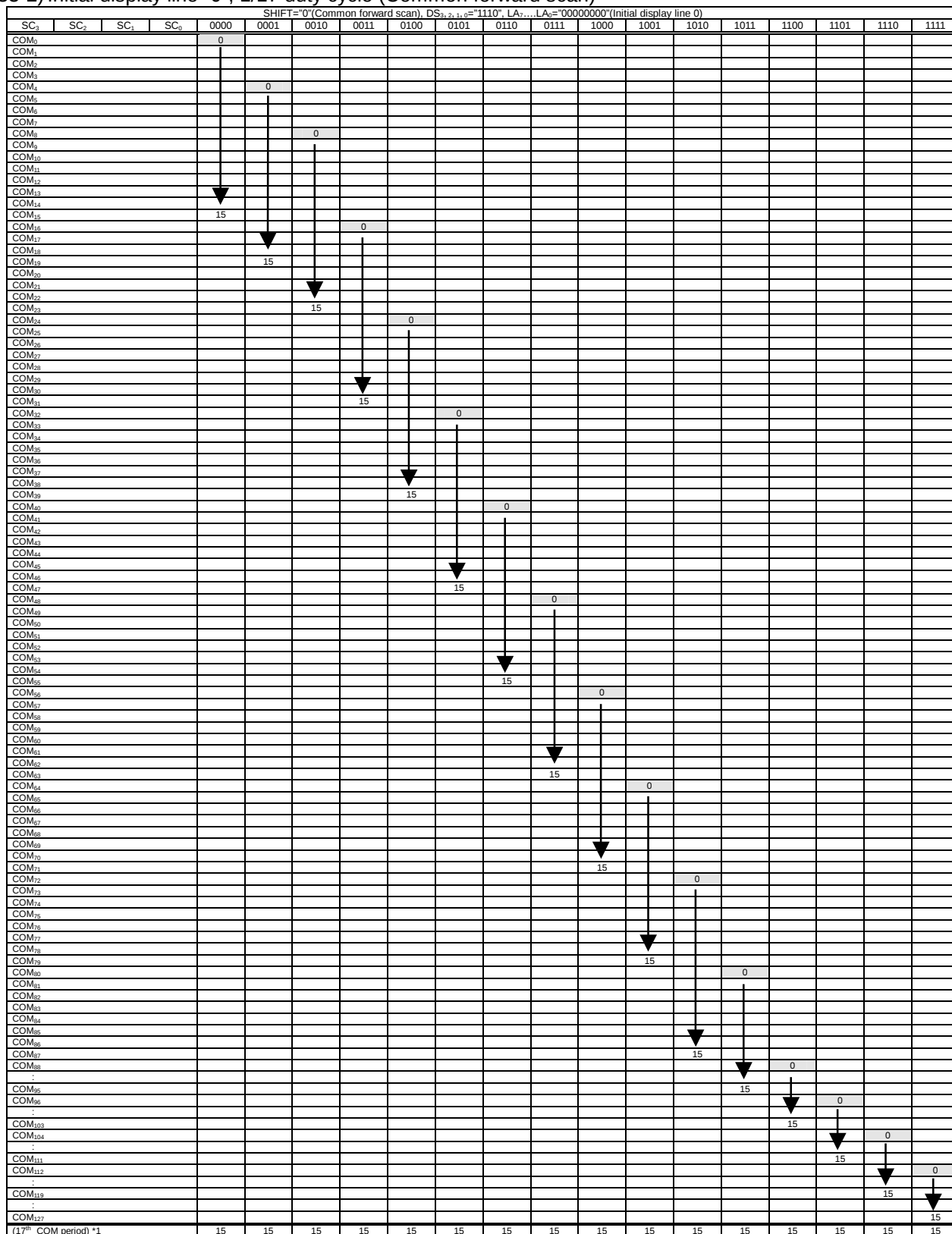
The relation between common drivers and row address of DDRAM (MY) is changing by the "Duty cycle ratio" and "Initial COM line" instructions. If the shift bit is "0", the order of common scanning is normal and if it is "1", the common scanning order is inversed. When LA₀ to LA₆ of initial display line setting is "0", the "MY" corresponding to the Initial COM line is also "0". And "MY" is increasing.
- When initial display line is not "0"

The relation between common drivers and row address of DDRAM (MY) is changing by the "Duty cycle ratio" and "Initial COM line" instructions. If the shift bit is "0", the order of common scanning is normal and if it is "1", the common scanning order is inversed. When LA₀ to LA₆ of initial display line setting is not "0", the "MY" corresponding to the Initial COM line is biased by the setting value. During the display, "MY" is increasing up to "127". When "MY" over than "127", its back to "0". And "MY" is increasing from 0 continuously.

The following are Examples of setting the start-line 0 or 5 at 1/129, 1/128, or 1/17 duty.

*1 : 129th COM period is not selected.

(33-2) Initial display line "0", 1/17 duty cycle (Common forward scan)



(33-3) Initial display line "0", 1/129 duty cycle (Common backward scan)

SHIFT="1"(Common backward scan), DS_{3,2,1,0}="0000", LA_{7,...}LA₀="00000000"(Initial display line 0)

Diagram illustrating the display layout and scan direction for a 128x128 pixel display. The layout is divided into four quadrants by a vertical line between columns 0000 and 0001, and a horizontal line between rows COM64 and COM65. The scan direction is indicated by arrows pointing right or down. The diagram shows the sequence of scan lines (COM0 to COM127) and the corresponding column addresses (0000 to 1111) for each scan line. The scan direction is indicated by arrows pointing right or down. The diagram shows the sequence of scan lines (COM0 to COM127) and the corresponding column addresses (0000 to 1111) for each scan line.

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 129th COM period is not selected.

(33-4) Initial display line "5", 1/129 duty cycle (Common forward scan)

[illegible]

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 129th COM period is not selected.

(33-5) Initial display line "0", 1/128 duty cycle (Common forward scan, DSE="1")

SHIFT="0"(Common forward scan), DS _{23,24,25} ="0000", LA ₁ ...LA ₅ ="00000000"(Initial display line 0) DSE="1"																						
SC ₆	SC ₅	SC ₄	SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
COM ₁							0	124	120	112	104	96	88	80	72	64	56	48	40	32	24	16
COM ₂								▼														
COM ₃								127														
COM ₄								0														
COM ₅									▼													
COM ₆									127													
COM ₇									0													
COM ₈										▼												
COM ₉										127												
COM ₁₀										0												
COM ₁₁											▼											
COM ₁₂											127											
COM ₁₃											0											
COM ₁₄												▼										
COM ₁₅												127										
COM ₁₆												0										
COM ₁₇													▼									
COM ₁₈													127									
COM ₁₉													0									
COM ₂₀														▼								
COM ₂₁														127								
COM ₂₂														0								
COM ₂₃															▼							
COM ₂₄															127							
COM ₂₅															0							
COM ₂₆																▼						
COM ₂₇																127						
COM ₂₈																0						
COM ₂₉																	▼					
COM ₃₀																	127					
COM ₃₁																	0					
COM ₃₂																		▼				
COM ₃₃																		127				
COM ₃₄																		0				
COM																						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	$V_{SS}=0V$ $T_a = +25^{\circ}C$	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +20.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +20.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +20.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

Note 1) $\overline{D_0}$ to $\overline{D_{15}}$, $\overline{CS}$, $\overline{RS}$, $\overline{RD}$, $\overline{WR}$, $\overline{OSC_1}$, $\overline{RES}$ terminals.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	$^{\circ}C$	

Note1) Applies to the condition when the reference voltage generator is not used.

Note2) Applies to the condition when the reference voltage generator is used.

Note3) Applies to the condition when the voltage booster is used.

Note4) The following relationship among the supply voltages must be maintained.

$$V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD} \leq V_{OUT}$$

Note5) The relationship: $V_{REF} < V_{EE}$ must be maintained.

■ DC CHARACTERISTICS 1

$V_{SS} = 0V$, $V_{DD} = +1.7$ to $+3.3V$, $T_a = -30$ to $+85^\circ C$

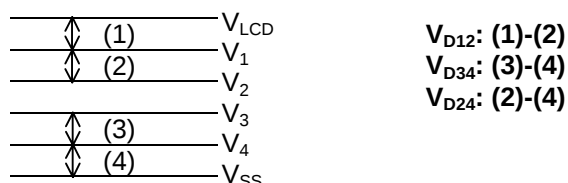
PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	*1
Low level input voltage	V_{IL}		0		$0.2V_{DD}$	V	*1
High level output voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	*2
Low level output voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	*2
High level output voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	*3
Low level output voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	*3
Input leakage current	I_{LI}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*4
Output leakage current	I_{LO}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*5
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$	$V_{LCD} = 10V$	1	2	k Ω	*6
			$V_{LCD} = 6V$	2	4		
Stand-by current	I_{STB}	$CS = V_{DD}$, $T_a = 25^\circ C$	$V_{DD} = 3V$		15	μA	*7
Internal oscillation Frequency	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^\circ C$	490	600	710	kHz	*8
	f_{OSC2}		110	135.5	160		*9
	f_{OSC3}		15.5	19.4	22.9		*10
External oscillation Frequency	f_{r1}	$R_f = 12k\Omega$		575		kHz	*11
	f_{r2}	$R_f = 62k\Omega$		135			
	f_{r3}	$R_f = 470k\Omega$		19.6			
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 6) $R_L = 500k\Omega$ ($V_{OUT} - V_{SS}$)	$(N \times V_{EE})$ $\times 0.95$			V	*12
Supply current (1)	I_{DD1}	$V_{DD} = 3V$, 6-time booster Whole ON pattern		760	1140	μA	*13
Supply current (2)	I_{DD2}	$V_{DD} = 3V$, 6-time booster Checker pattern		930	1400		
Supply current (3)	I_{DD3}	$V_{DD} = 3V$, 5-time booster Whole ON pattern		520	780		
Supply current (4)	I_{DD4}	$V_{DD} = 3V$, 5-time booster Checker pattern		650	980		
Supply current (5)	I_{DD5}	$V_{DD} = 3V$, 4-time booster Whole ON pattern		360	540		
Supply current (6)	I_{DD6}	$V_{DD} = 3V$, 4-time booster Checker pattern		450	680		
V_{BA} Operating voltage	V_{BA}	$V_{EE} = 2.4$ to $3.3V$	$(0.9 V_{EE})$ $\times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE})$ $\times 1.02$	V	*14
V_{REG} Operating voltage	V_{REG}	$V_{EE} = 2.4$ to $3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time booster (N=2 to 6)	$(V_{REF} \times N)$ $\times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N)$ $\times 1.03$	V	*15
Output Voltage	V_2		-100	0	+100	mV	*16
	V_3		-100	0	+100		
	V_{D12}		-30	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

■ CLOCK and FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/129 to 1/81	1/73 to 1/41	1/33 to 1/25	1/17	
Internal clock	f_{OSC}	16 Gradation mode	$f_{OSC} / (62xD)$	$f_{OSC} / (62xD \times 2)$	$f_{OSC} / (62xD \times 4)$	$f_{OSC} / (62xD \times 8)$	FLM
		Simplified 8 gradation mode	$f_{OSC} / (14xD)$	$f_{OSC} / (14xD \times 2)$	$f_{OSC} / (14xD \times 4)$	$f_{OSC} / (14xD \times 8)$	
		B&W mode	$f_{OSC} / (2xD)$	$f_{OSC} / (2xD \times 2)$	$f_{OSC} / (2xD \times 4)$	$f_{OSC} / (2xD \times 8)$	
External clock	f_{CK}	16 Gradation mode	$f_{CK} / (62xD)$	$f_{CK} / (62xD \times 2)$	$f_{CK} / (62xD \times 4)$	$f_{CK} / (62xD \times 8)$	
		Simplified 8 gradation mode	$f_{CK} / (14xD)$	$f_{CK} / (14xD \times 2)$	$f_{CK} / (14xD \times 4)$	$f_{CK} / (14xD \times 8)$	
		B&W mode	$f_{CK} / (2xD)$	$f_{CK} / (2xD \times 2)$	$f_{CK} / (2xD \times 4)$	$f_{CK} / (2xD \times 8)$	

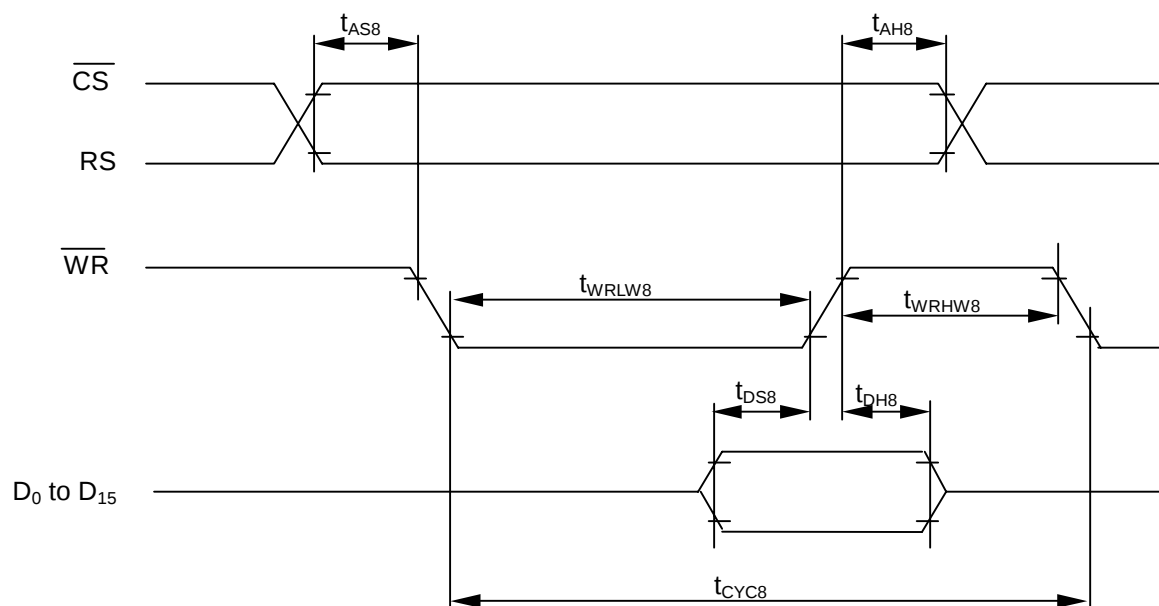
APPLIED TERMINALS and CONDITIONS

- Note 1) D_0 - D_{15} , $\overline{CS}$, RS, $\overline{RD}$, $\overline{WR}$, P/S, SEL68, $\overline{RES}$
- Note 2) D_0 - D_{15}
- Note 3) CL, FLM, FR, CLK
- Note 4) $\overline{CS}$, RS, SEL68, $\overline{RD}$, $\overline{WR}$, P/S, $\overline{RES}$, OSC₁
- Note 5) D_0 - D_{15} in the high impedance
- Note 6) - SEG_{A0}-SEG_{A127}, SEG_{B0}-SEG_{B127}, SEG_{C0}-SEG_{C127}, COM₀-COM₁₂₇ and SEG_{SA0}-SEG_{SA1}, SEG_{SB0}-SEG_{SB1}, SEG_{SC0}-SEG_{SC1}
Defines the resistance between each of the SEG and COM terminals and each of the power supply terminals (V_{LCD} , V_1 , V_2 , V_3 and V_4) in the 0.5V deference and 1/9 LCD bias ratio.
- Note 7) V_{DD}
The oscillator is halted, $\overline{CS}$ ="1" (disabled), No-load onto the segment and common drivers
- Note 8) OSC
Defines the internal oscillation frequency at (Rf_2 , Rf_1 , Rf_0)=(0,0,0) in the variable gradation mode.
- Note 9) OSC
Defines the internal oscillation frequency at (Rf_2 , Rf_1 , Rf_0)=(0,0,0) in the fixed gradation mode.
- Note 10) OSC
Defines the internal oscillation frequency at (Rf_2 , Rf_1 , Rf_0)=(0,0,0) in the Black & White mode.
- Note 11) V_{DD} =3V, T_a =25°C
- Note 12) V_{OUT}
Applies to the condition when the internal voltage booster (N=2-6), internal oscillator and internal power circuits are used. V_{EE} =2.4V to 3.3V, EVR= (1,1,1,1,1,1)
1/5 to 1/12 LCD bias, 1/129 duty cycle, No-load on segment and common drivers
RL=500Kohm between V_{OUT} and V_{SS} , CA_1 = CA_2 =1.0uF, CA_3 =0.1uF, DCON="1", AMPON="1"
- Note 13) V_{DD}
Applies to the condition when using the internal oscillator and internal power circuits without any access from MPU. EVR= (1,1,1,1,1,1), All pixels turned-on or checkerboard display in gradation mode.
No-load onto the segment and common drivers
 V_{DD} = V_{EE} , V_{REF} =0.9 V_{EE} , CA_1 = CA_2 =1.0uF, CA_3 =0.1uF, DCON="1", AMPON="1", NLIN="0"
1/129 Duty cycle, T_a =25°C
- Note 14) V_{BA}
Applies to the condition that V_{BA} = V_{REF} and voltage booster N= 1.
When DCON="0", V_{OUT} =13.5V input.
- Note 15) V_{REG}
 V_{EE} =2.4V to 3.3V, V_{REF} =0.9 V_{EE} , V_{OUT} =18V, 1/5 to 1/12 LCD bias ratio, 1/129 duty cycle, EVR=(1,1,1,1,1,1), Checkerboard display, No-load onto the segment and common drivers, voltage booster N=2 to 6, V_1A_1 , V_1A_2 , V_4A_1 , V_4A_2 ="0".
 CA_1 = CA_2 =1.0uF, CA_3 =0.1uF, DCON="0", AMPON="1", NLIN="0".
- Note 16) V_{LCD} , V_1 , V_2 , V_3 , V_4
 V_{EE} =3.0V, V_{REF} =0.9 V_{EE} , V_{OUT} =15V, 1/5 to 1/12 LCD Bias, EVR= (1,1,1,1,1,1), Display OFF, No-load onto the segment and common drivers, voltage booster N=5, V_1A_1 , V_1A_2 , V_4A_1 , V_4A_2 ="0".
 CA_1 = CA_2 =1.0uF, CA_3 =0.1uF, DCON="0", AMPON="1"



■ AC CHARACTERISTICS

● Write operation (80-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	$\overline{CS}$
Address setup time	t_{AS8}		0		ns	$\overline{RS}$
System cycle time	t_{CYC8}		90		ns	$\overline{WR}$
Enable "L" level pulse width	t_{WRLW8}		35		ns	
Enable "H" level pulse width	t_{WRHW8}		35		ns	
Data setup time	t_{DS8}		30		ns	D_0 to D_{15}
Data hold time	t_{DH8}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

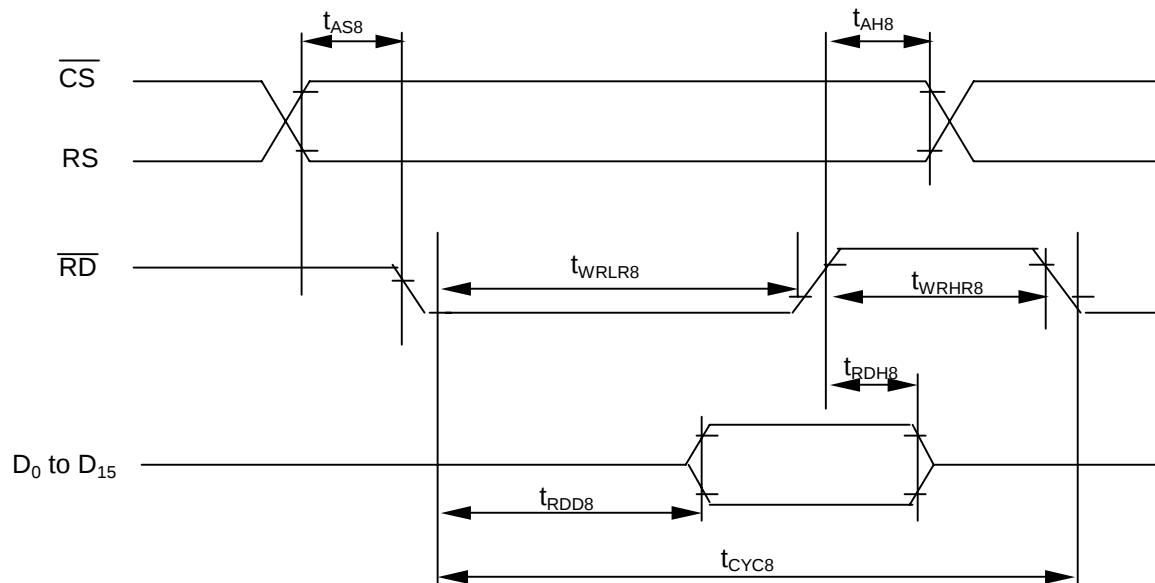
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	$\overline{CS}$
Address setup time	t_{AS8}		0		ns	$\overline{RS}$
System cycle time	t_{CYC8}		160		ns	$\overline{WR}$
Enable "L" level pulse width	t_{WRLW8}		70		ns	
Enable "H" level pulse width	t_{WRHW8}		70		ns	
Data setup time	t_{DS8}		40		ns	D_0 to D_{15}
Data hold time	t_{DH8}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	$\overline{CS}$
Address setup time	t_{AS8}		0		ns	$\overline{RS}$
System cycle time	t_{CYC8}		180		ns	$\overline{WR}$
Enable "L" level pulse width	t_{WRLW8}		80		ns	
Enable "H" level pulse width	t_{WRHW8}		80		ns	
Data setup time	t_{DS8}		70		ns	D_0 to D_{15}
Data hold time	t_{DH8}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Read operation (80-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	$\overline{CS}$
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	$\overline{RD}$
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data setup time	T_{RDD8}	$CL=15pF$	0	60	ns	D_0 to D_{15}
Read Data hold time	T_{RDH8}		0		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

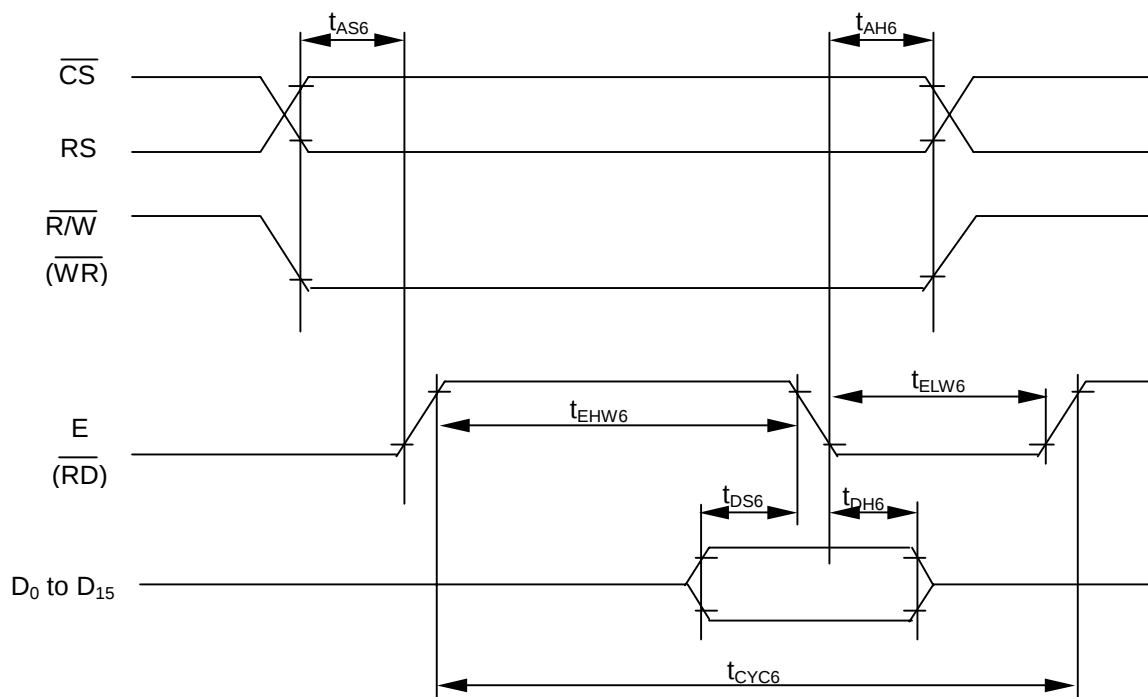
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	$\overline{CS}$
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	$\overline{RD}$
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data setup time	T_{RDD8}	$CL=15pF$	0	60	ns	D_0 to D_{15}
Read Data hold time	T_{RDH8}		0		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	$\overline{CS}$
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		250		ns	$\overline{RD}$
Enable "L" level pulse width	t_{WRLR8}		120		ns	
Enable "H" level pulse width	t_{WRHR8}		120		ns	
Read Data setup time	t_{RDD8}	$CL=15pF$	0	110	ns	D_0 to D_{15}
Read Data hold time	t_{RDH8}		0		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Write operation (68-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	$\overline{CS}$
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D_0 to D_{15}
Data hold time	t_{DH6}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

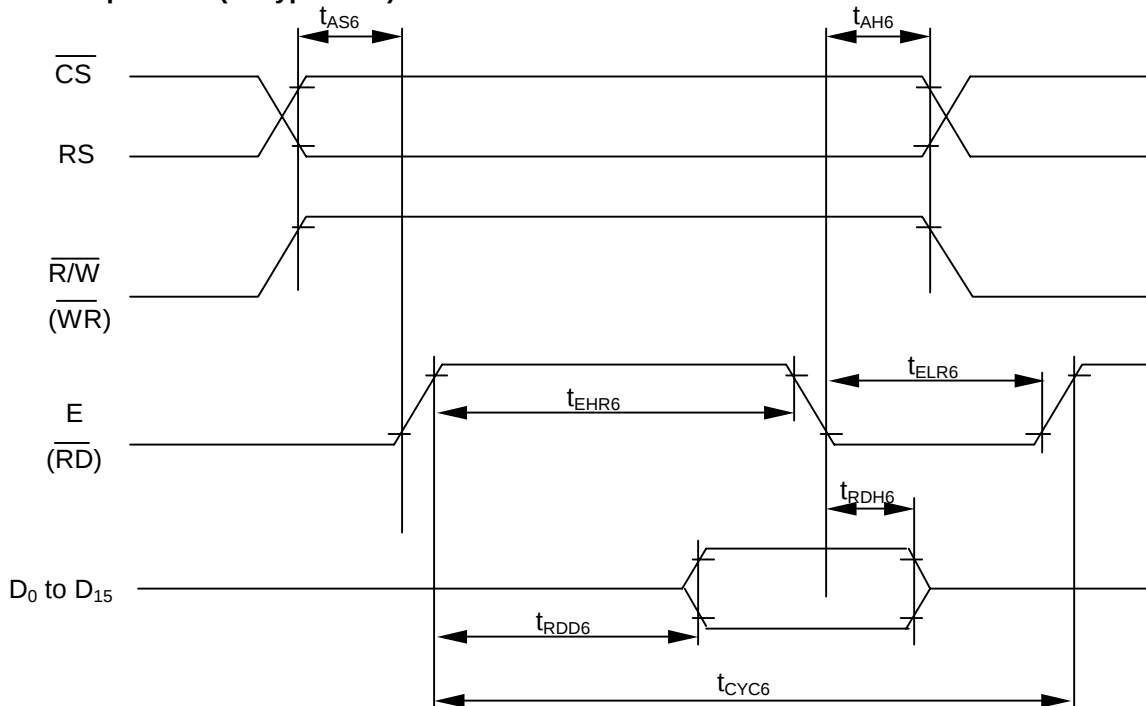
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	$\overline{CS}$
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D_0 to D_{15}
Data hold time	t_{DH6}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	$\overline{CS}$
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D_0 to D_{15}
Data hold time	t_{DH6}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Read operation (68-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^\circ C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	$\overline{CS}$
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data setup time	t_{RDD6}	$CL=15pF$	0	70	ns	D_0 to D_{15}
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^\circ C$)

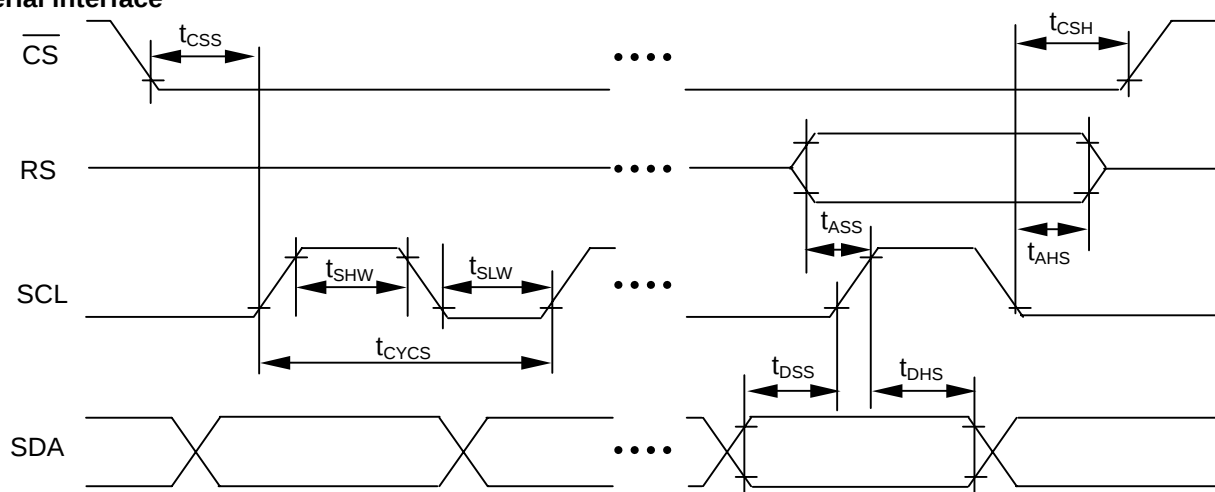
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	$\overline{CS}$
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data setup time	t_{RDD6}	$CL=15pF$	0	70	ns	D_0 to D_{15}
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^\circ C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	$\overline{CS}$
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		250		ns	E
Enable "L" level pulse width	t_{ELR6}		120		ns	
Enable "H" level pulse width	t_{EHR6}		120		ns	
Read Data setup time	t_{RDD6}	$CL=15pF$	0	110	ns	D_0 to D_{15}
Read Data hold time	t_{RDH6}				ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Serial interface



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	SCL
SCL "L" level pulse width	t_{SLW}		20		ns	SCL
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	RS
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	SDA
$\overline{CS}$ – SCL time	t_{CSS}		20		ns	$\overline{CS}$
$\overline{CS}$ hold time	t_{CSH}		20		ns	$\overline{CS}$

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

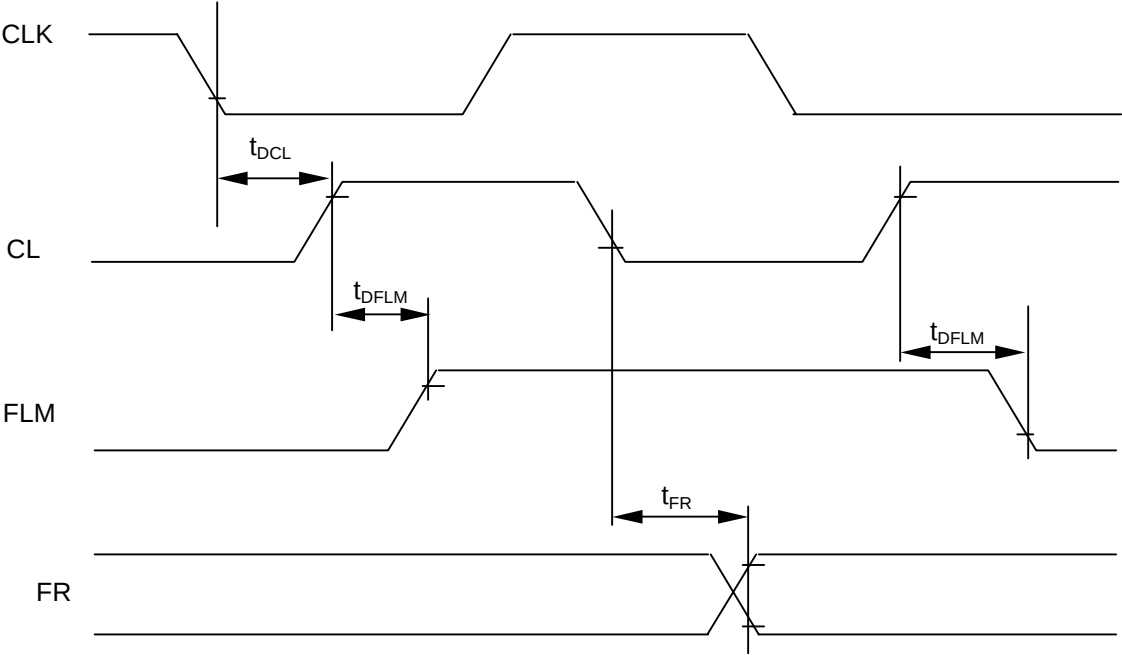
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	SCL
SCL "L" level pulse width	t_{SLW}		20		ns	SCL
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	RS
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	SDA
$\overline{CS}$ – SCL time	t_{CSS}		20		ns	$\overline{CS}$
$\overline{CS}$ hold time	t_{CSH}		20		ns	$\overline{CS}$

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	SCL
SCL "L" level pulse width	t_{SLW}		35		ns	SCL
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	RS
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	SDA
$\overline{CS}$ – SCL time	t_{CSS}		35		ns	$\overline{CS}$
$\overline{CS}$ hold time	t_{CSH}		35		ns	$\overline{CS}$

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Display control timing



Output timing (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

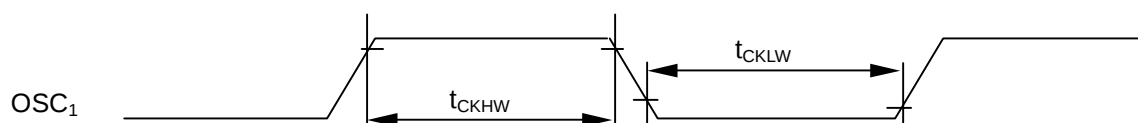
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Note) Each timing is specified based on 20% and 80% of V_{DD}.

● Input clock timing



($V_{DD}=1.7$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC ₁ "H" level pulse width (1)	t_{CKHW1}		0.70	1.02	μs	OSC ₁ *1
OSC ₁ "L" level pulse width (1)	t_{CKLW1}		0.70	1.02	μs	
OSC ₁ "H" level pulse width (2)	t_{CKHW2}		3.13	4.55	μs	OSC ₁ *2
OSC ₁ "L" level pulse width (2)	t_{CKLW2}		3.13	4.55	μs	
OSC ₁ "H" level pulse width (3)	t_{CKHW3}		21.8	31.4	μs	OSC ₁ *3
OSC ₁ "L" level pulse width (3)	t_{CKLW3}		21.8	31.4	μs	

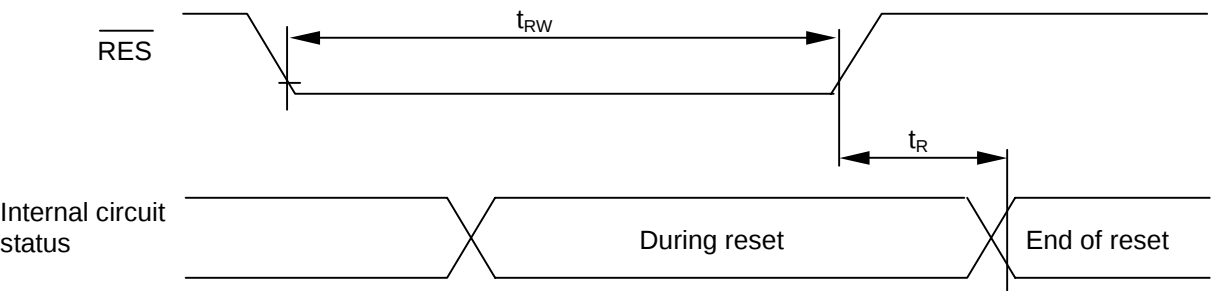
Note) Each timing is specified based on 20% and 80% of V_{DD} .

Note 1) Applied in the variable gradation mode MON="0", PWM="0"

Note 2) Applied in the fixed gradation mode MON="0", PWM="1"

Note 3) Applied in the B&W mode MON="1"

● Reset input timing



($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RES "L" level pulse width	t_{RW}		10.0		μs	$\overline{\text{RES}}$

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RES "L" level pulse width	t_{RW}		10.0		μs	$\overline{\text{RES}}$

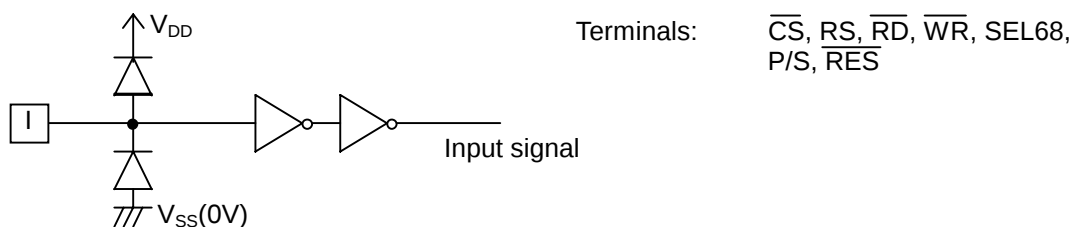
Note) Each timing is specified based on 20% and 80% of V_{DD} .

- Typical characteristic

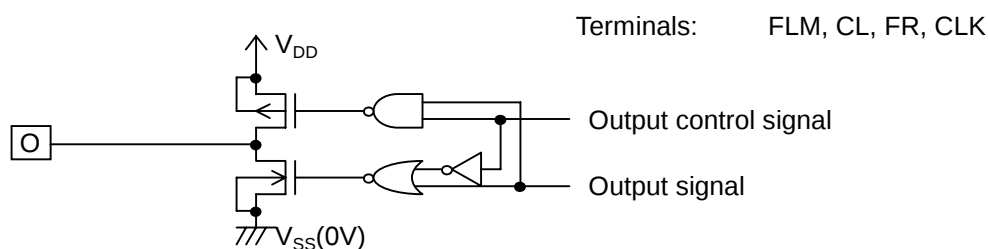
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gate	$T_a=+25^{\circ}\text{C}$, $V_{SS}=0\text{V}$, $V_{DD}=3.0\text{V}$		10		ns

- Input output terminal type

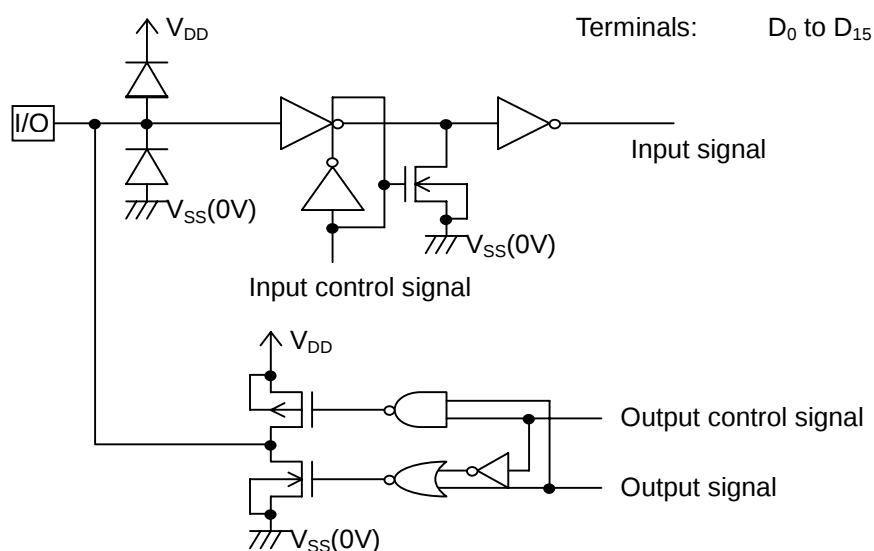
(a) Input circuit



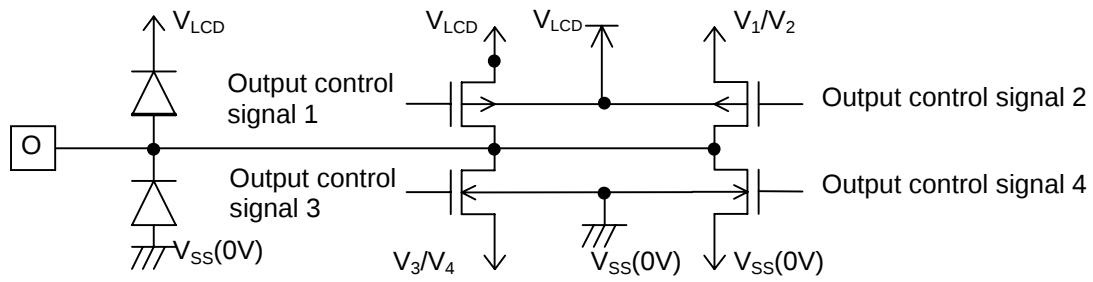
(b) Output circuit



(c) Input/Output circuit



(d) Display output circuit

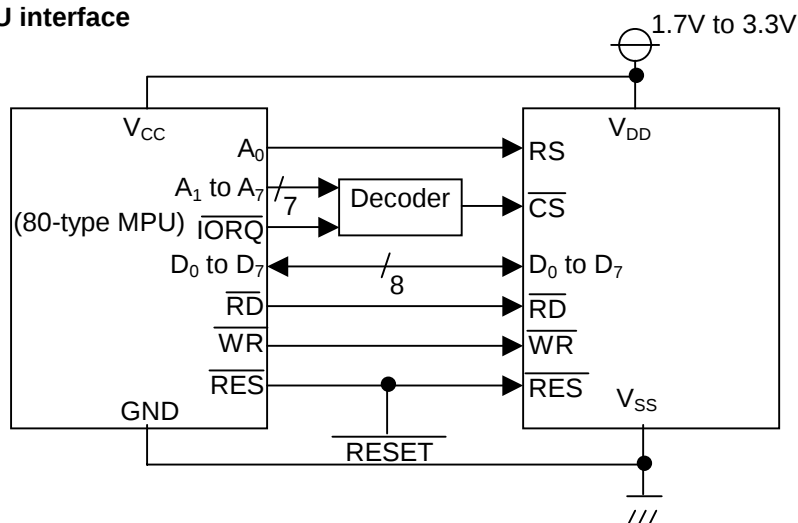


Terminals: SEGA₀ to SEGA₁₂₇
 SEGB₀ to SEGB₁₂₇
 SEGC₀ to SEGC₁₂₇
 COM₀ to COM₁₂₇
 SEGSA₀ to SEGSA₁
 SEGSB₀ to SEGSB₁
 SEGSC₀ to SEGSC₁

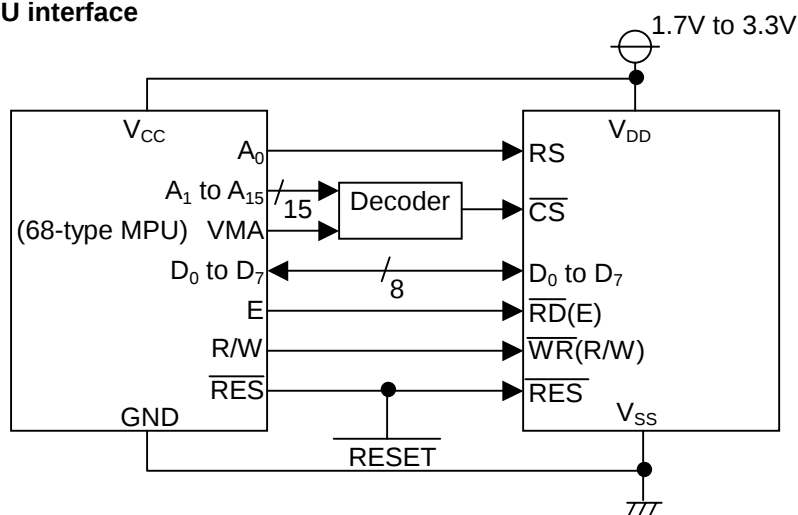
APPLICATION CIRCUIT EXAMPLES

(1) MPU Connections

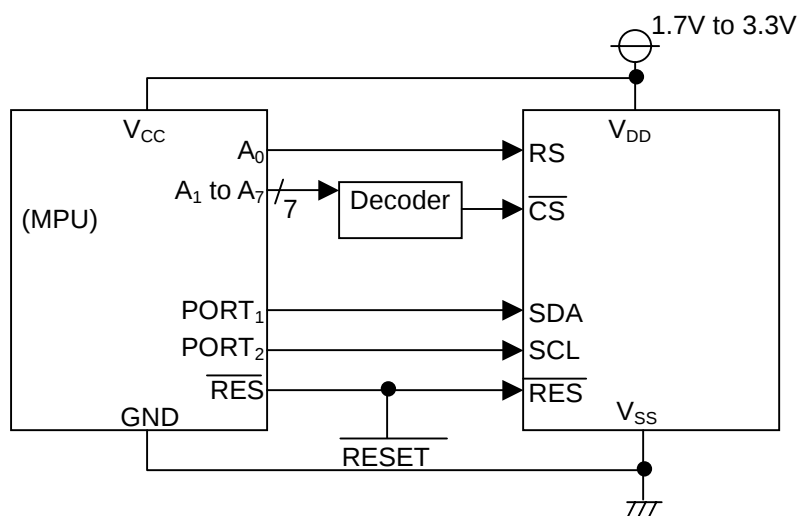
80-type MPU interface



68-type MPU interface



Serial interface



[CAUTION]

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