Product Specification

PE4259

SPDT High Power UltraCMOS™
DC – 3.0 GHz RF Switch

Product Description

The PE4259 UltraCMOS™ RF Switch is designed to cover a broad range of applications from near DC through 3000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. Using a nominal +3-volt power supply voltage, a typical input 1 dB compression point of +33.5 dBm can be achieved.

The PE4259 SPDT High Power UltraCMOS™ RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- Single-pin or complementary CMOS logic control inputs
- Low insertion loss: 0.35 dB at 1000 MHz, 0.5 dB at 2000 MHz
- Isolation of 30 dB at 1000 MHz, 20 dB at 2000 MHz
- Typical input 1 dB compression point of +33.5 dBm
- Ultra-small SC-70 package

Figure 1. Functional Diagram

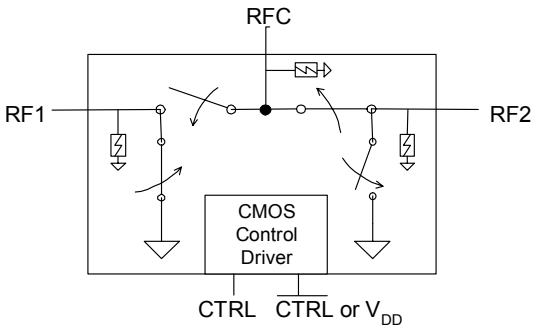


Figure 2. Package Type SC-70

6-lead SC-70

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operation Frequency[1]		DC		3000	MHz
Insertion Loss	1000 MHz 2000 MHz		0.35 0.50	0.45 0.60	dB dB
Isolation	1000 MHz 2000 MHz	29 19	30 20		dB dB
Return Loss	1000 MHz 2000 MHz	21 24	22 27		dB dB
'ON' Switching Time	50% CTRL to 0.1 dB of final value, 1 GHz		1.50		us
'OFF' Switching Time	50% CTRL to 25 dB isolation, 1 GHz		1.50		us
Video Feedthrough[2]			15		mV_{pp}
Input 1 dB Compression	1000 MHz	31.5	33.5		dBm
Input IP3	1000 MHz, 20dBm input power		55		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50 Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

Figure 3. Pin Configuration (Top View)

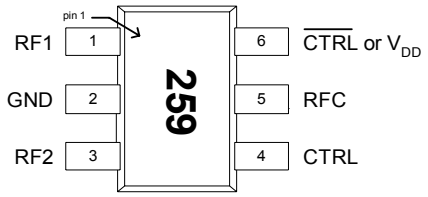


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1	RF Port1[3]
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2	RF Port2[3]
4	CTRL	Switch control input, CMOS logic level.
5	RFC	RF Common [3]
6	$\overline{\text{CTRL}}$ or V_{DD}	This pin supports two interface options: *Single-pin control mode*. A nominal 3-volt supply connection is required. *Complementary-pin control mode*. A complementary CMOS control signal to CTRL is supplied to this pin. By-passing on this pin is not required in this mode.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		+34[4]	dBm
V_{ESD}	ESD Voltage (HBM, ML_STD 883 Method 3015.7)		2000	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		250	

Notes: 3. All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

4. To maintain optimum device performance, do not exceed Max P_{IN} at desired operating frequency (see Figure 4).

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.3	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		9	20	µA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Figure 4. Maximum Input Power

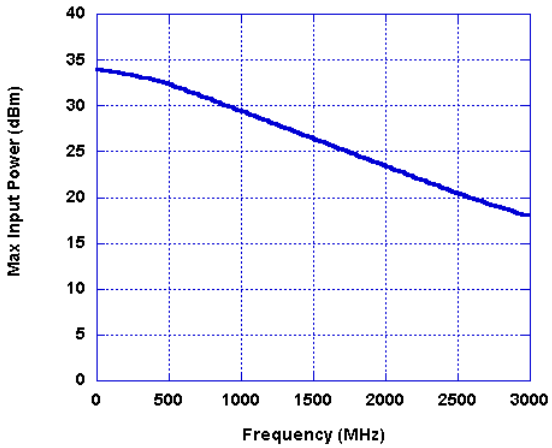


Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 ($\overline{CTRL}$ or V_{DD}) = Low Pin 4 (CTRL) = High	RFC to RF1
Pin 6 ($\overline{CTRL}$ or V_{DD}) = High Pin 4 (CTRL) = Low	RFC to RF2

Control Logic Input

The PE4259 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS µProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CTRL and $\overline{CTRL}$ (pins 4 & 6), that can be directly driven by +3-volt CMOS logic or a suitable µProcessor I/O port. This enables the PE4259 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4259 operating limits.

Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 5. Insertion Loss

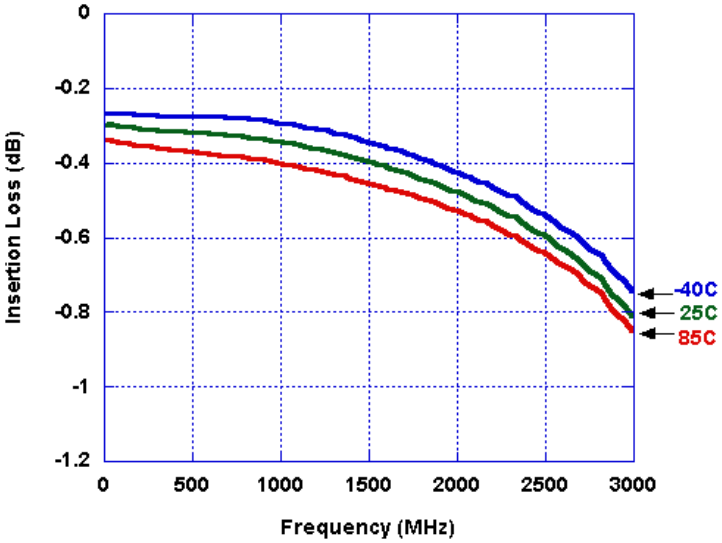


Figure 6. Isolation – Input to Output

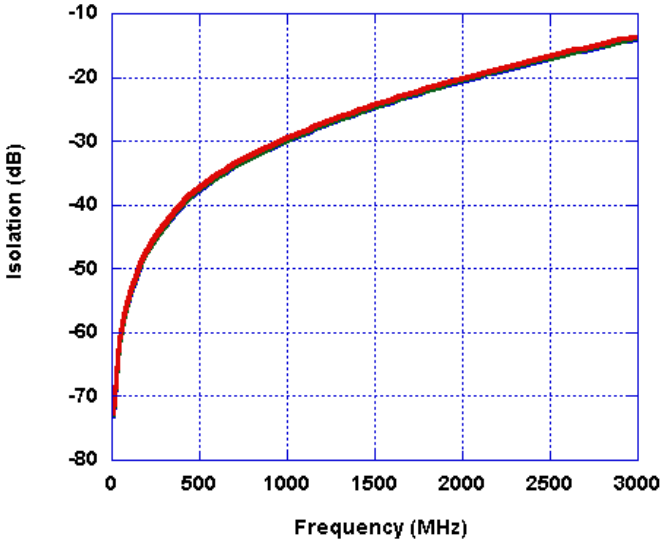


Figure 7. Isolation – Output to Output

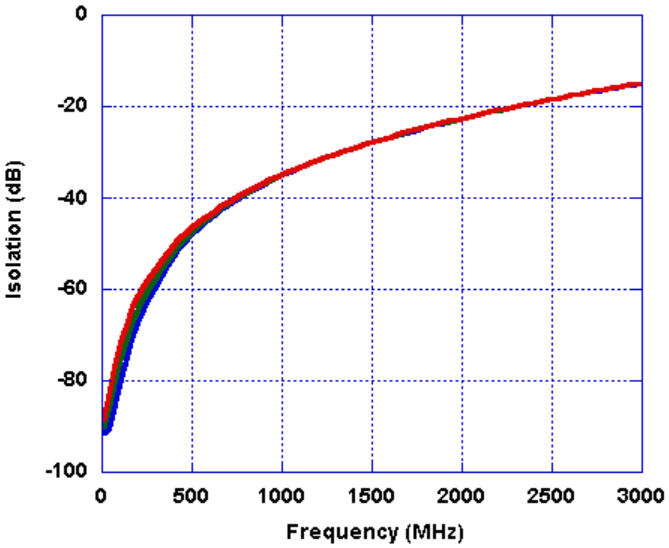
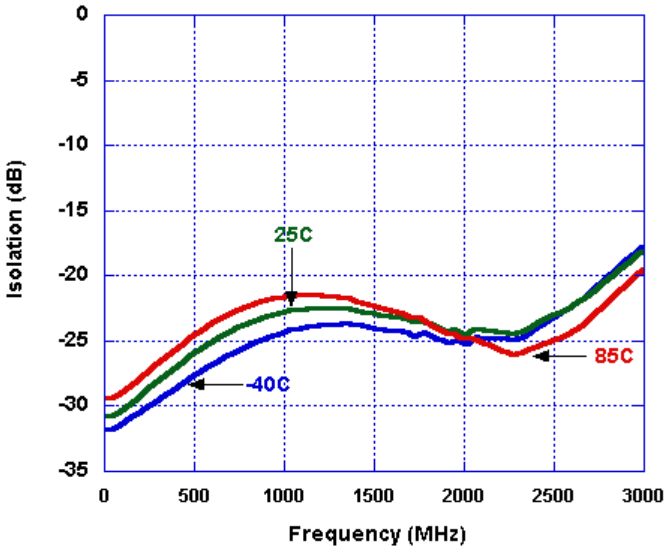


Figure 8. Return Loss (Input)



Typical Performance Data @ V_{DD} = 2.3V, T=25°C

Figure 9. Insertion Loss

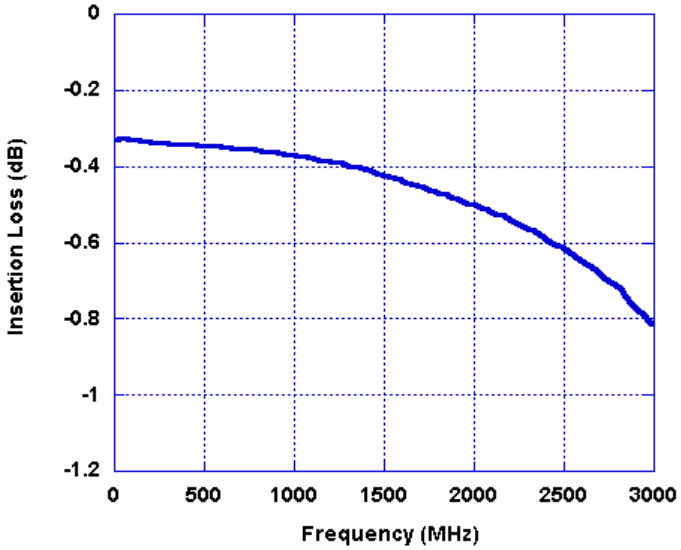


Figure 10. Isolation – Input to Output

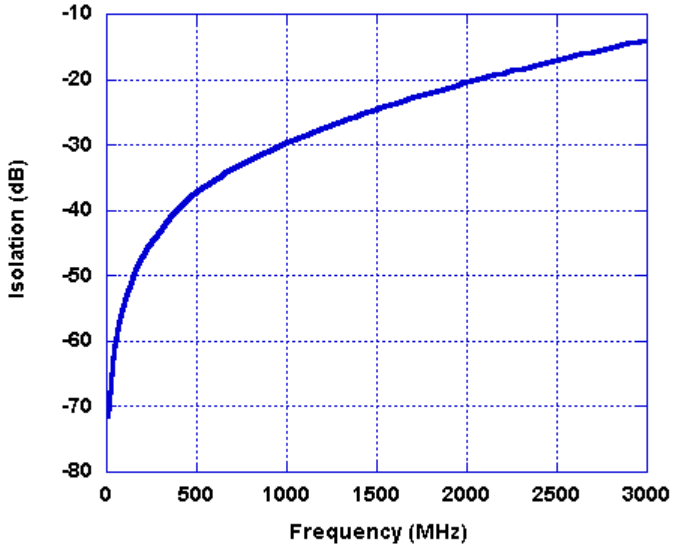


Figure 11. Isolation – Output to Output

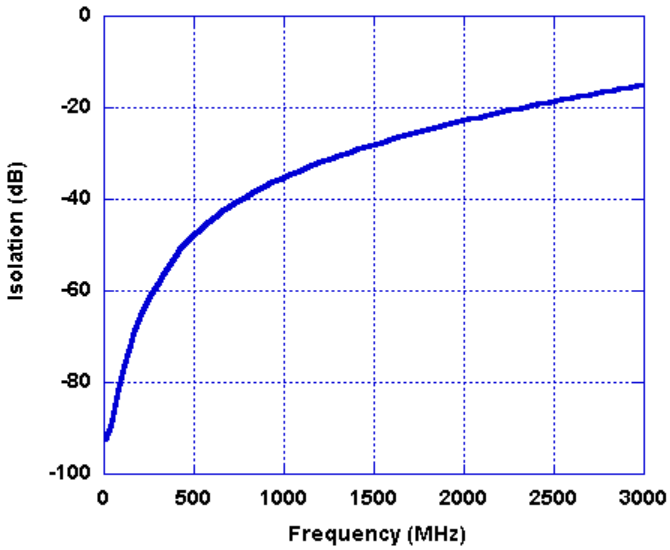
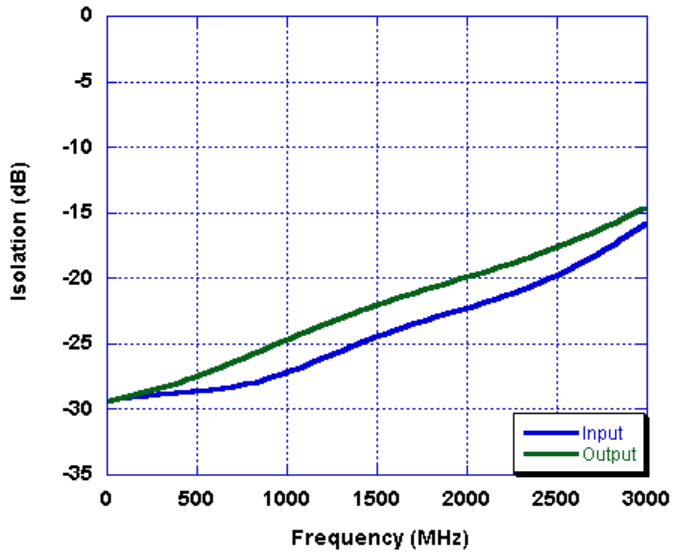


Figure 12. Return Loss (Input & Output)



Evaluation Kit

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE4259. The RF common port is connected through a 50 Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50 Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50 Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device V_{DD} or CTRL input. J7-1 is connected to the device CTRL input.

Figure 8. Evaluation Board Layouts
Peregrine Specification 101/0162

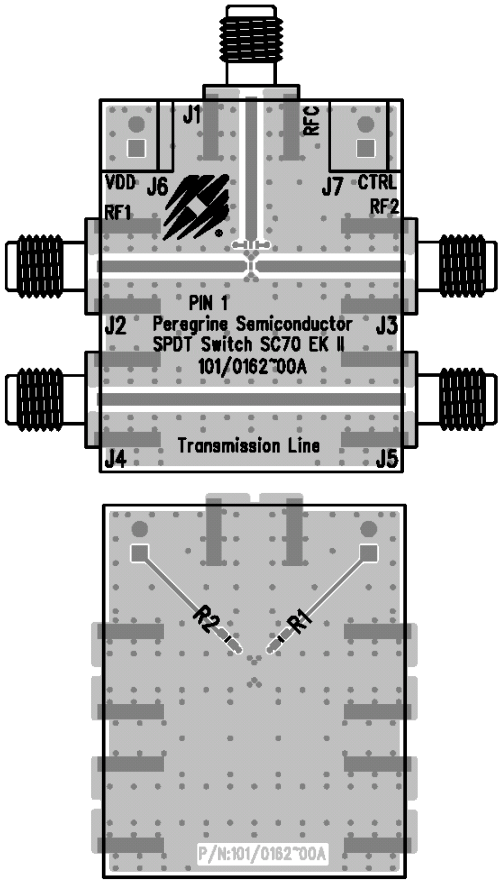


Figure 9. Evaluation Board Schematic
Peregrine Specification 102/0218

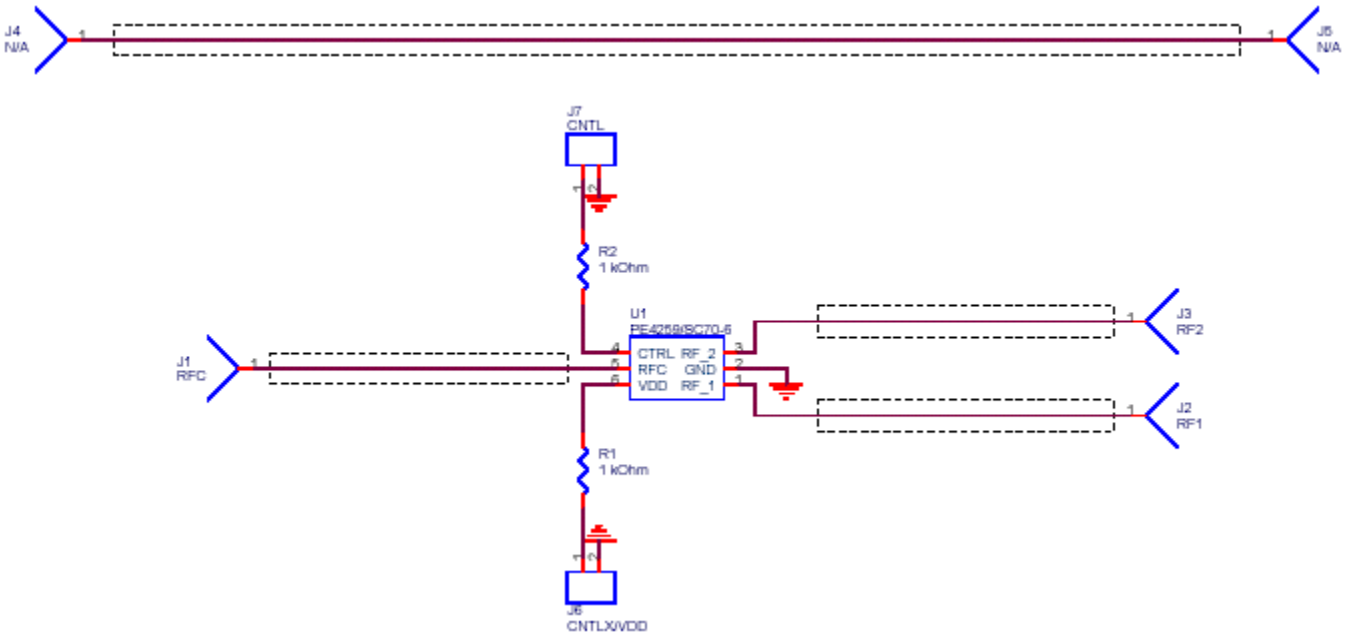


Figure 14. Package Drawing

6-lead SC-70

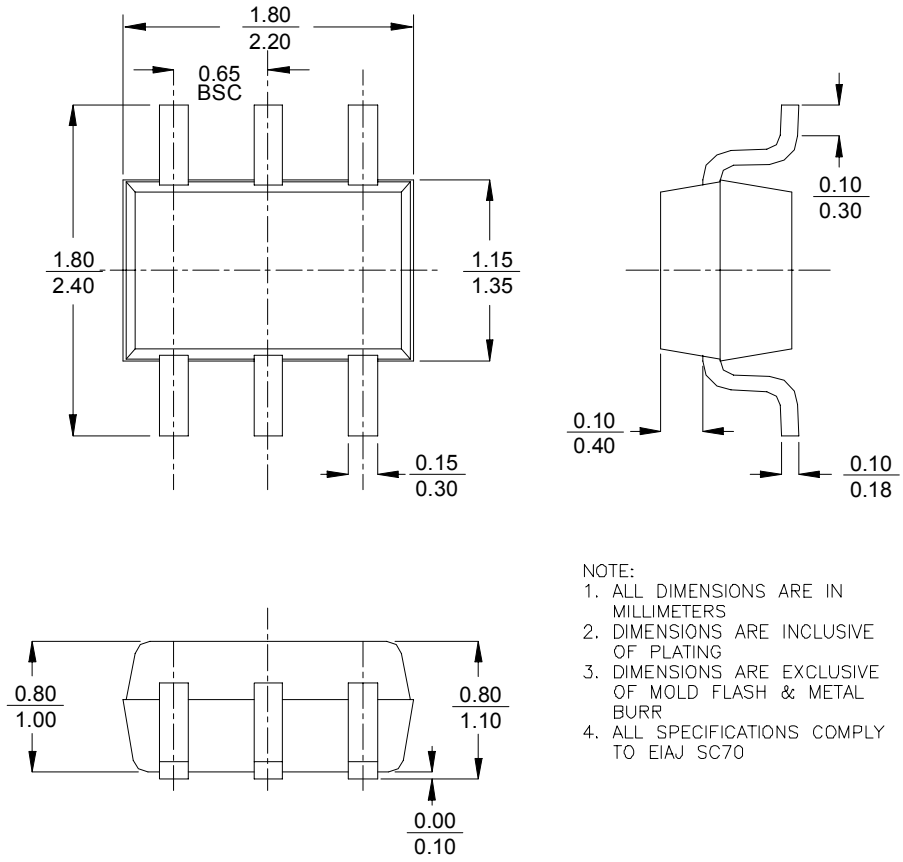


Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4259-01	259	PE4259-06SC70-7680A	6-lead SC-70	7680 units / Canister
4259-02	259	PE4259-06SC70-3000C	6-lead SC-70	3000 units / T&R
4259-00	PE4259-EK	PE4259-06SC70-EK	Evaluation Kit	1 / Box
4259-51	259	PE4259G-06SC70-7680A	Green 6-lead SC-70	7680 units / Canister
4259-52	259	PE4259G-06SC70-3000C	Green 6-lead SC-70	3000 units / T&R

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Data Sheet Identification

Advance Information

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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