PIC16C622A → PIC16F628 Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next. Table 1 shows the considerations that must be taken into account when migrating from the PIC16C622A to the PIC16F628. Table 2 shows electrical and timing differences.

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Note: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

TABLE 1: PIC16C622A → PIC16F628 FUNCTIONAL DIFFERENCES

No.	Module	Differences from PIC16C622A	H/W	S/W	Prog.
1	Oscillator	ER Osc mode	Yes	—	—
2	Oscillator	Dual Speed mode	Yes	—	—
3	Oscillator	EC Osc mode	Yes	—	—
4	Oscillator	IntRC Osc mode	Yes	—	—
5	USART	9-bit USART	Yes	—	—
6	$\overline{\text{MCLR}}$	$\overline{\text{MCLR}}$ Disable	Yes	—	—
7	Programming	Low Voltage Programming mode	—	—	Yes
8	Memory	RAM	—	—	Yes
9	Memory	EEPROM Data Memory	—	—	Yes

Legend: H/W - Issues may exist with regard to the application circuit.
S/W - Issues may exist with regard to the user program.
Prog. - Issues may exist with regard to programming.

OSCILLATOR MODULE

ER Mode

The PIC16F628 supports the new External Resistor Oscillator mode. This mode differs from the traditional RC Oscillator mode in that only a resistor to bias current is required. Designers should verify their oscillator design for suitability in the application before use. ER Oscillator mode also supports Dual Speed mode.

EC Mode

The PIC16F628 supports the new External Clock-in mode. It is designed for usage in applications where a system clock is available. This mode provides a 1x clock directly to the PIC16F628 core. There is no gain stage in-line. Designers should verify their oscillator design for suitability in the application before use.

IntRC Mode

The PIC16F628 IntRC Oscillator mode now supports Dual Speed mode also.

Dual Speed Mode

The PIC16F628 supports Dual Speed mode when configured in either ER or IntRC modes. This sub-mode of operation toggles between a fixed 37 kHz frequency and the frequency set by either ER or IntRC modes.

CONFIG Reg. bits Fosc<2:0>	Description	PCON Reg. bit OSCF	Result
111	ER mode w/clkout	1	ER bias'ed speed
111	ER mode w/clkout	0	37 kHz
110	ER mode w/o clkout	1	ER bias'ed speed
110	ER mode w/o clkout	0	37 kHz
101	IntRC w/clkout	1	4 MHz
101	IntRC w/clkout	0	37 kHz
100	IntRC w/o clkout	1	4 MHz
100	IntRC w/o clkout	0	37 kHz

USART MODULE

9-bit USART

The PIC16F628 USART now supports 9-bit mode. This mode is useful in multi-processor communications. When bits RX9 and ADEN in register RCSTA are set, multi-processor communication is enabled. The 9th bit is used to indicate whether address or data is being transmitted by the Master.

$\overline{\text{MCLR}}$ MODULE

The $\overline{\text{MCLR}}$ pin can be disabled on the PIC16F628 if LVP is disabled. If LVP is enabled, then $\overline{\text{MCLR}}$ is always enabled, regardless of the state of the $\overline{\text{MCLR}}$ disable fuse. When the $\overline{\text{MCLR}}$ is disabled, the pin becomes RA5 and is an input only pin. V_{PP} can still be applied to this pin to initiate programming. All $\overline{\text{MCLR}}$ signals are generated internally if the $\overline{\text{MCLR}}$ is disabled.

MEMORY ORGANIZATION MODULE

RAM

The PIC16F628 has 224 bytes of data RAM while the PIC16C622A has 128 bytes.

EEPROM Data

The PIC16F628 has 128 bytes of EEPROM data memory.

PROGRAMMING MODULE

Low Voltage Programming Mode

The PIC16F628 supports Low Voltage Programming mode. When the LVP bit of the configuration word is asserted, placing a '1' on the RB4/PGM pin will instruct the part to enter Low Voltage Programming mode.

Note 1: While in this mode, the RB4 pin can no longer be used as a general purpose I/O pin.

2: V_{DD} must be 5.0V ±10% during erase/program operations while in Low Voltage Programming mode.

TABLE 2: PIC16C622A → PIC16F628 ELECTRICAL SPECIFICATION DIFFERENCES

Parm. No.	Sym.	Characteristic	PIC16C622A Data Sheet			PIC16F628 Data Sheet			Units	Conditions
			Min	Typ†	Max	Min	Typ†	Max		
D010	IDD	**Supply Current (Note 1)**	—	0.4	1.2	—	—	0.7	mA	FOSC = 4 MHz, VDD = 3.0V, WDT Disabled, XT Osc mode
			—	1.0	2.0	—	—	2.0	mA	FOSC = 10 MHz, VDD = 3.0V, WDT Disabled, HS Osc mode
D023	ΔIWDT	**WDT Current (Note 3)**	—	6.0	10	—	6.0	20	µA	VDD = 4.0V
			—	—	12	—	—	25	µA	(125°)
	ΔICOMP	**Comparator Current for each Comparator (Note 3)**	—	30	60	—	30	50	µA	VDD = 4.0V
	ΔIVREF	**VREF Current (Note 3)**	—	80	135	—	—	135	µA	VDD = 4.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

2: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

3: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

4: Commercial temperature range only.

5: Includes EE static current. Does not include EE reads or writes.

TABLE 3: PIC16LC622A → PIC16LF628 ELECTRICAL SPECIFICATION DIFFERENCES

Parm. No.	Sym.	Characteristic	PIC16LC622A Data Sheet			PIC16LF628 Data Sheet			Units	Conditions
			Min	Typ†	Max	Min	Typ†	Max		
D010	IDD	**Supply Current (Note 1)**	—	—	1.1	—	—	0.6	mA	FOSC = 4 MHz, VDD = 2.5V, WDT Disabled, XT Osc mode
D023	ΔIWDT	**WDT Current (Note 3)**	—	—	—	—	6.0	15	µA	VDD = 3.0V
			—	6.0	10	—	—	—	µA	VDD = 4.0V
			—	—	12	—	—	—	µA	(125°)
	ΔICOMP	**Comparator Current for each Comparator (Note 3)**	—	—	—	—	30	50	µA	VDD = 3.0V
			—	30	60	—	—	—	µA	VDD = 4.0V
	ΔIVREF	**VREF Current (Note 3)**	—	—	—	—	—	135	µA	VDD = 3.0V
			—	80	135	—	—	—	µA	VDD = 4.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
MCLR = VDD; WDT enabled/disabled as specified.

2: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

3: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

4: Includes EE static current. Does not include EE reads or writes.

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