MIC45205

26V/6A DC/DC Power Module

Features

- No Compensation Required
- Up to 6A Output Current
- >93% Peak Efficiency
- Output Voltage: 0.8V to 0.85 x V_{IN} with ±1% Accuracy
- Adjustable Switching Frequency from 200 kHz to 600 kHz
- Enable Input and Open-Drain Power Good Output
- HyperLight Load (MIC45205-1) Improves Light Load Efficiency
- Hyper Speed Control (MIC45205-2) Architecture Enables Fast Transient Response
- Supports Safe Startup into Pre-Biased Output
- –40°C to +125°C Junction Temperature Range
- Thermal Shutdown Protection
- Short-Circuit Protection with Hiccup Mode
- Adjustable Current-Limit
- Available in 52-pin 8 mm × 8 mm × 3 mm QFN Package

Applications

- High Power Density Point-of-Load Conversion
- Servers, Routers, Networking, and Base Stations
- FPGAs, DSP, and Low-Voltage ASIC Power Supplies
- Industrial and Medical Equipment

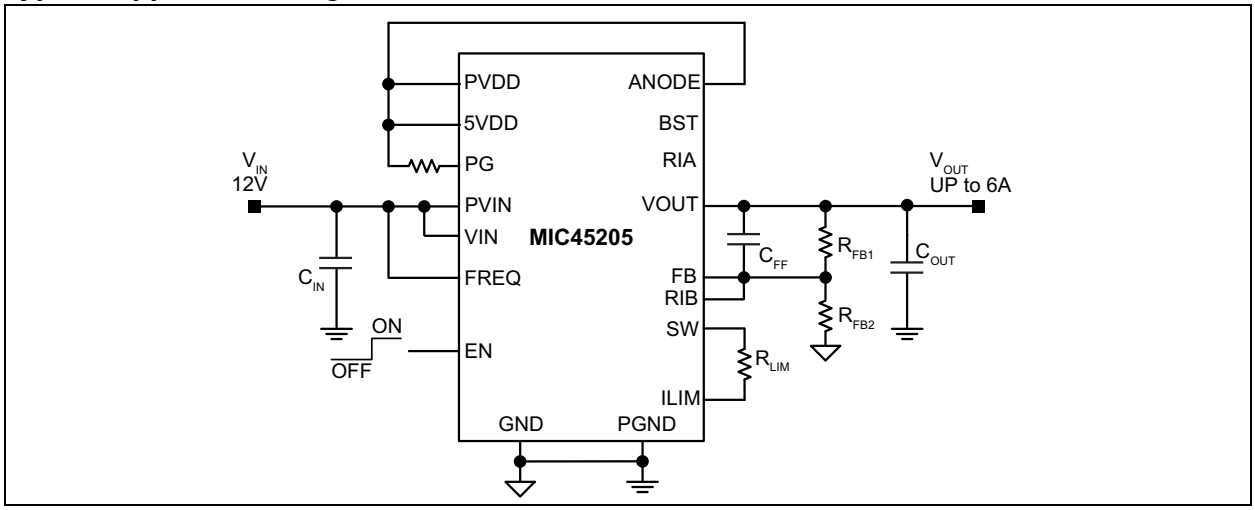
General Description

MIC45205 is a synchronous step-down regulator module, featuring a unique adaptive ON-time control architecture. The module incorporates a DC/DC controller, power MOSFETs, bootstrap diode, bootstrap capacitor, and an inductor in a single package; simplifying the design and layout process for the end user.

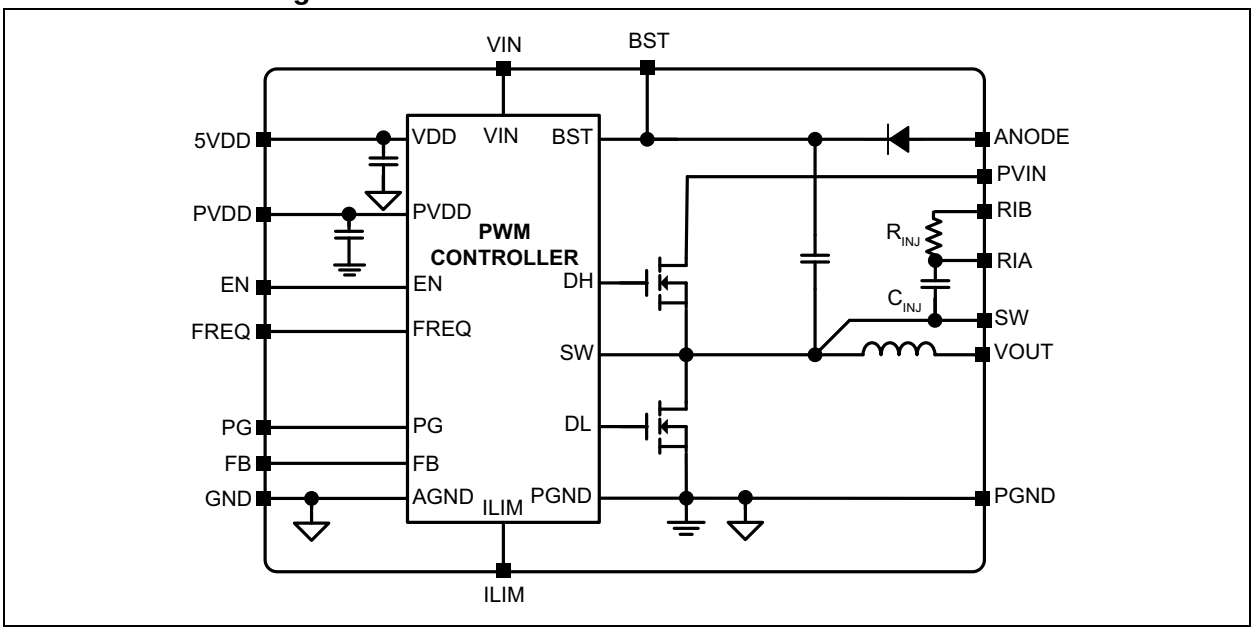
This highly integrated solution expedites system design and improves product time-to-market. The internal MOSFETs and inductor are optimized to achieve high efficiency at a low output voltage. The fully optimized design can deliver up to 6A current under a wide input voltage range of 4.5V to 26V, without requiring additional cooling.

The MIC45205-1 uses Microchip's HyperLight Load® (HLL) and the MIC45205-2 uses Microchip's Hyper Speed Control® architecture that enables ultra-fast load transient response, allowing for a reduction of output capacitance. The MIC45205 offers 1% output accuracy that can be adjusted from 0.8V to 0.85 x V_{IN} with two external resistors. Additional features include thermal shutdown protection, input undervoltage lockout, adjustable current-limit, and short-circuit protection. The MIC45205 allows for safe start-up into a pre-biased output.

Typical Application Diagram



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{PVIN}, V_{VIN} to PGND ..... –0.3V to +30V
V_{PVDD}, V_{5VDD}, V_{ANODE} to PGND ..... –0.3V to +6V
V_{SW}, V_{FREQ}, V_{ILIM}, V_{EN} to PGND ..... –0.3V to (V_{IN} + 0.3V)
V_{BST} to V_{SW} ..... –0.3V to +6V
V_{BST} to PGND ..... –0.3V to +36V
V_{PG} to PGND ..... –0.3V to ($5V_{DD}$ + 0.3V)
V_{FB}, V_{RIB} to PGND ..... –0.3V to ($5V_{DD}$ + 0.3V)
PGND to GND ..... –0.3V to +0.3V

Operating Ratings ‡

Supply Voltage (V_{PVIN}, V_{VIN}) ..... +4.5V to +26V
Output Current 6A
Enable Input (V_{EN}) ..... 0V to V_{IN}
Power Good (V_{PG}) ..... 0V to $5V_{DD}$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, V_{BST} – V_{SW} = 5V, T_J = +25ºC. **Bold** values indicate –40ºC < T_J < +125ºC, unless otherwise noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range	V_{IN}, PV_{IN}	**4.5**	—	**26**	V	—
Quiescent Supply Current (MIC45205-1)	I_Q	—	0.35	**0.75**	mA	V_{FB} = 1.5V
Quiescent Supply Current (MIC45205-2)	I_Q	—	2.1	**3**	mA	V_{FB} = 1.5V
Operating Current	I_{IN}	—	31	—	mA	V_{PVIN} = V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 0A f_{SW} = 600 kHz (MIC45205-2)
Shutdown Supply Current	I_{SHDN}	—	0.1	**10**	µA	SW = unconnected, V_{EN} = 0V
$5V_{DD}$ Output						
$5V_{DD}$ Output Voltage	V_{DD}	**4.8**	5.1	**5.4**	V	V_{IN} = 7V to 26V, I_{5VDD} = 10 mA
$5V_{DD}$ UVLO Threshold	UVLO	**3.8**	4.2	**4.6**	V	V_{5VDD} rising
$5V_{DD}$ UVLO Hysteresis	UVLO_HYS	—	400	—	mV	V_{5VDD} falling
LDO Load Regulation	$V_{DD(LR)}$	0.6	2	3.6	%	I_{5VDD} = 0 mA to 40 mA
Reference						
Feedback Reference Voltage	V_{FB}	0.792	0.8	0.808	V	T_J = +25°C
		0.784	0.8	**0.816**		–40°C ≤ T_J ≤ +125°C
FB Bias Current	I_{FB_BIAS}	—	5	**500**	nA	V_{FB} = 0.8V
Enable Control						
EN Logic Level High	EN_{HIGH}	**1.8**	—	—	V	—

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{EN} = 12V$, $V_{OUT} = 3.3V$, $V_{BST} – V_{SW} = 5V$, $T_J = +25ºC$. **Bold** values indicate $–40ºC < T_J < +125ºC$, unless otherwise noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
EN Logic Level Low	EN_{LOW}	—	—	**0.6**	V	—
EN Hysteresis	EN_{HYS}	—	200	—	mV	—
EN Bias Current	I_{ENBIAS}	—	5	**10**	µA	$V_{EN} = 12V$
Oscillator						
Switching Frequency	f_{SW}	**400**	600	**750**	kHz	$V_{FREQ} = V_{IN}$, $I_{OUT} = 2A$
		—	350	—		$V_{FREQ} = 50\% V_{IN}$, $I_{OUT} = 2A$
Maximum Duty Cycle	D_{MAX}	—	85	—	%	—
Minimum Duty Cycle	D_{MIN}	—	0	—	%	$V_{FB} = 1V$
Minimum Off-Time	$t_{OFF(MIN)}$	140	200	260	ns	—
Soft-Start						
Soft-Start Time	t_{SS}	—	5	—	ms	FB from 0V to 0.8V
Short-Circuit Protection						
Current-Limit Threshold	V_{CL_OFFSET}	–30	–14	0	mV	$V_{FB} = 0.79V$
Short-Circuit Threshold	V_{SC}	–23	–7	9	mV	$V_{FB} = 0V$
Current-Limit Source Current	I_{CL}	55	70	85	µA	$V_{FB} = 0.79V$
Short-Circuit Source Current	I_{SC}	25	35	45	µA	$V_{FB} = 0V$
Leakage						
SW, BST Leakage Current	$I_{SW\_LEAKAGE}$	—	—	10	µA	—
FREQ Leakage Current	I_{FREQ_LEAK}	—	—	10	µA	—
Power Good (PG)						
PG Threshold Voltage	V_{PG_TH}	**85**	90	**95**	% V_{OUT}	Sweep V_{FB} from Low-to-High
PG Hysteresis	V_{PG_HYS}	—	6	—	% V_{OUT}	Sweep V_{FB} from High-to-Low
PG Delay Time	t_{PG_DLY}	—	100	—	µs	Sweep V_{FB} from Low-to-High
PG Low Voltage	V_{PG_LOW}	—	70	**200**	mV	$V_{FB} < 90\% \times V_{NOM}$, $I_{PG} = 1$ mA
Thermal Protection						
Overtemperature Shutdown	T_{SHD}	—	160	—	°C	T_J rising
Overtemperature Shutdown Hysteresis	T_{SHD_HYS}	—	15	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature Range	T_J	–40	—	+125	°C	—
Maximum Junction Temperature	—	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance QFN-52	θ_{JA}	—	21.7	—	°C/W	Note 2
Thermal Resistance QFN-52	θ_{JC}	—	5.0	—	°C/W	Note 2

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: θ_{JA} and θ_{JC} were measured using the MIC45205 evaluation board.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

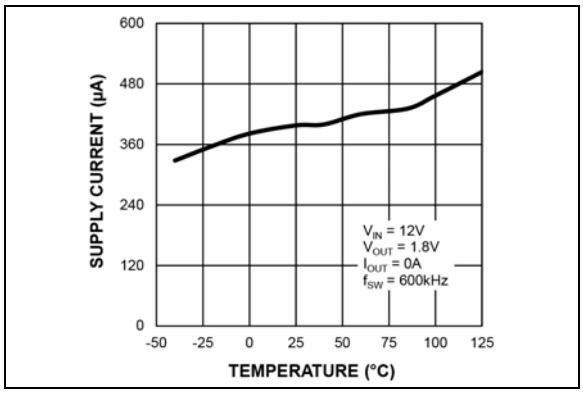


FIGURE 2-1: *V_{IN} Operating Supply Current vs. Temperature (MIC45205-1).*

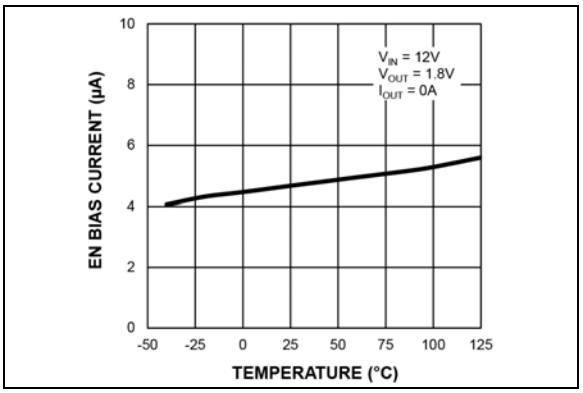


FIGURE 2-4: *EN Bias Current vs. Temperature.*

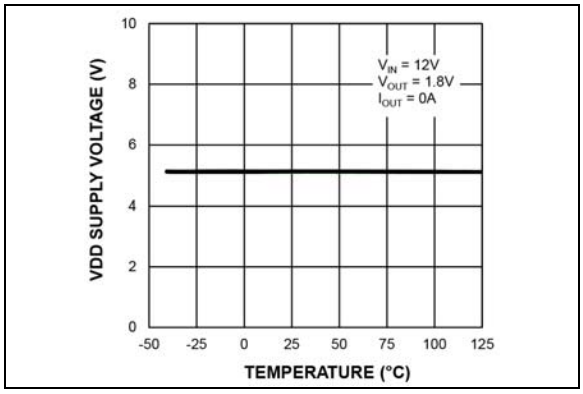


FIGURE 2-2: *V_{DD} Supply Voltage vs. Temperature.*

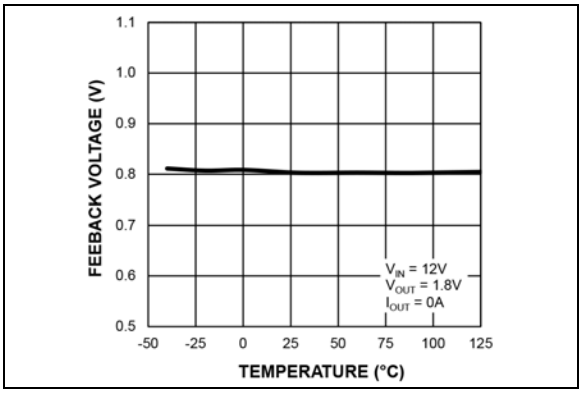


FIGURE 2-5: *Feedback Voltage vs. Temperature.*

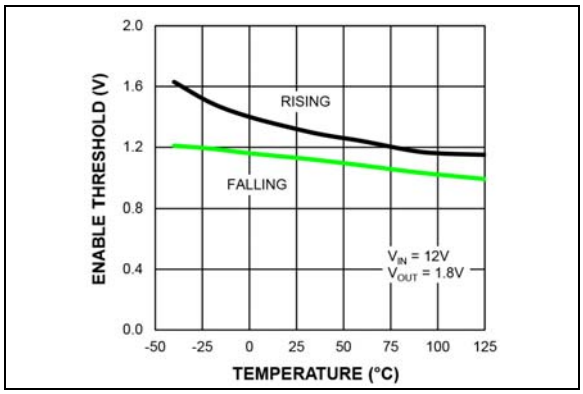


FIGURE 2-3: *Enable Threshold vs. Temperature.*

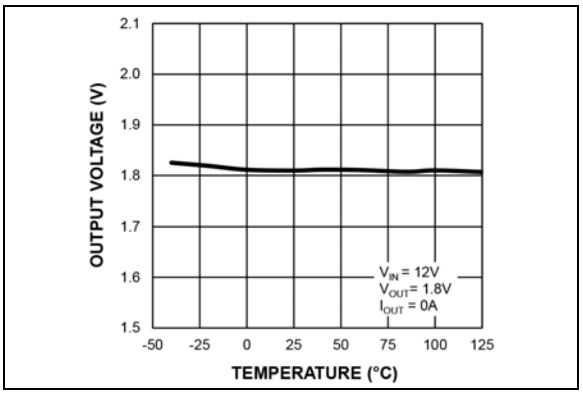


FIGURE 2-6: *Output Voltage vs. Temperature.*

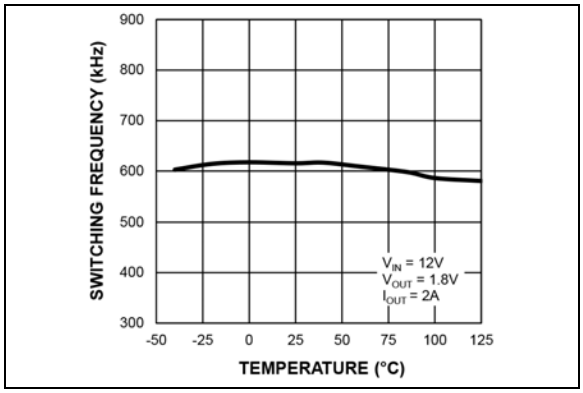


FIGURE 2-7: *Switching Frequency vs. Temperature.*

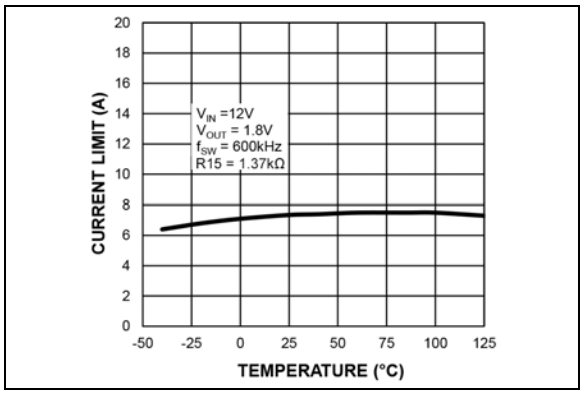


FIGURE 2-8: *Output Peak Current Limit vs. Temperature.*

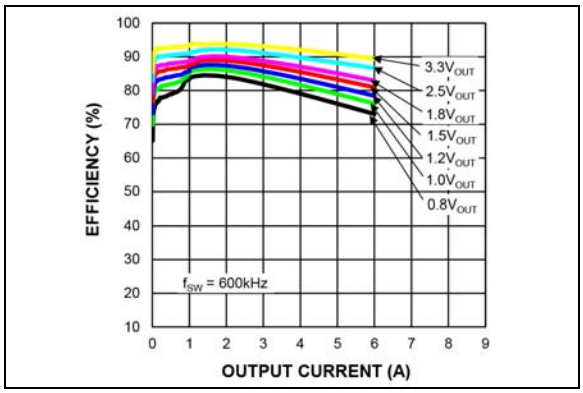


FIGURE 2-9: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC45205-1).*

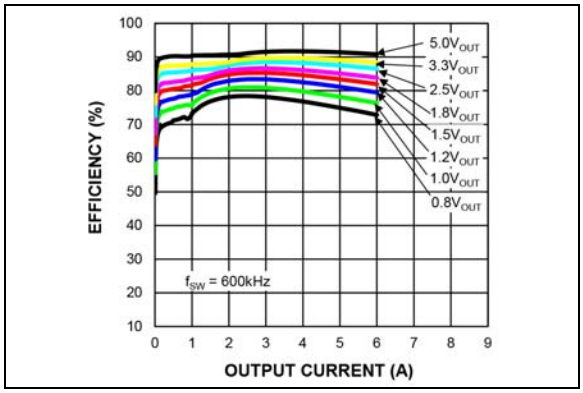


FIGURE 2-10: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC45205-1).*

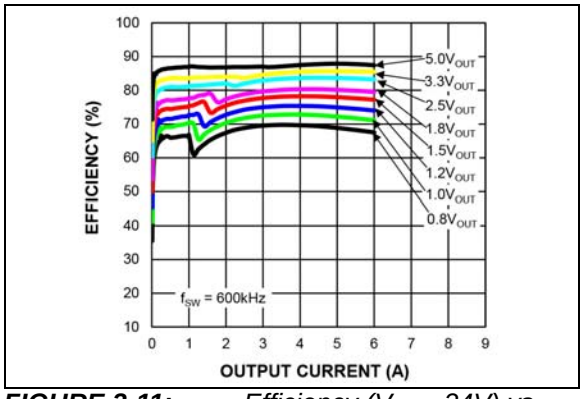


FIGURE 2-11: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC45205-1).*

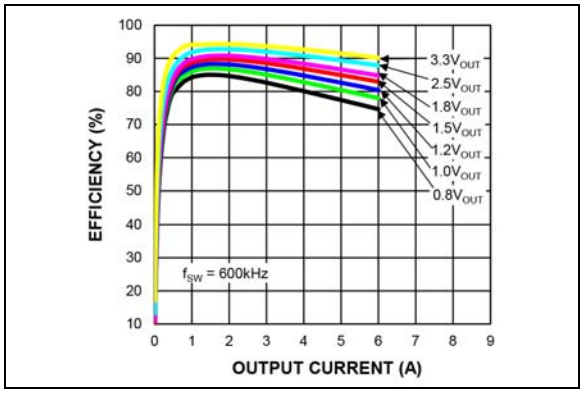


FIGURE 2-12: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC45205-2).*

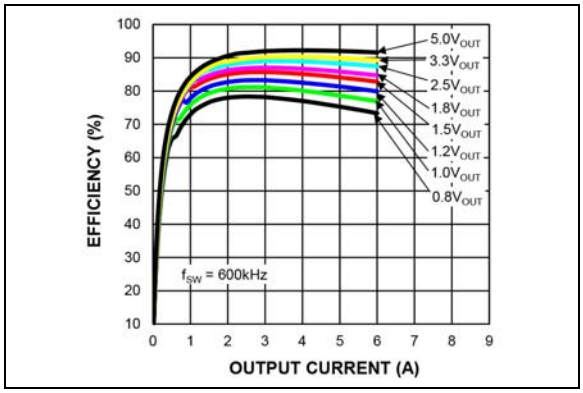


FIGURE 2-13: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC45205-2).*

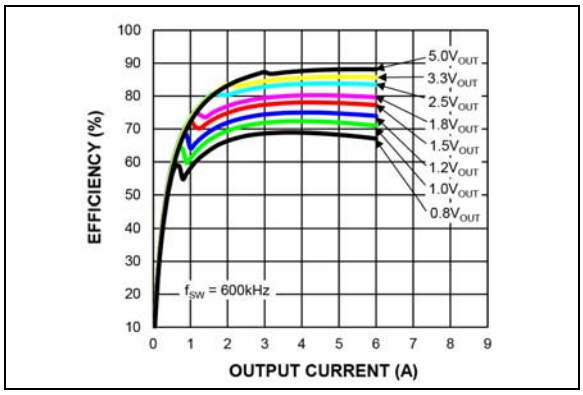


FIGURE 2-14: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC45205-2).*

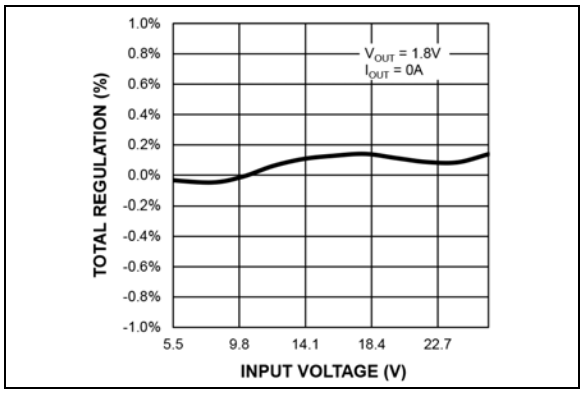


FIGURE 2-15: *Line Regulation.*

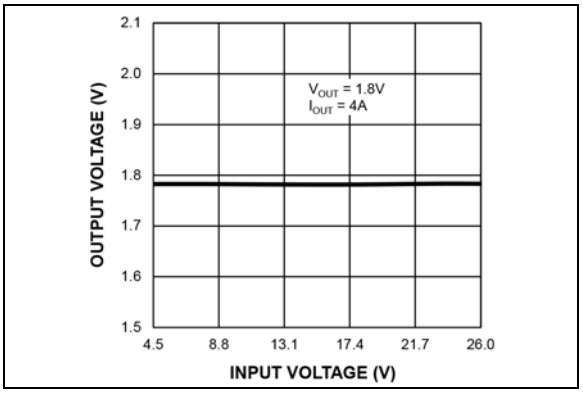


FIGURE 2-16: *Output Voltage vs. Input Voltage.*

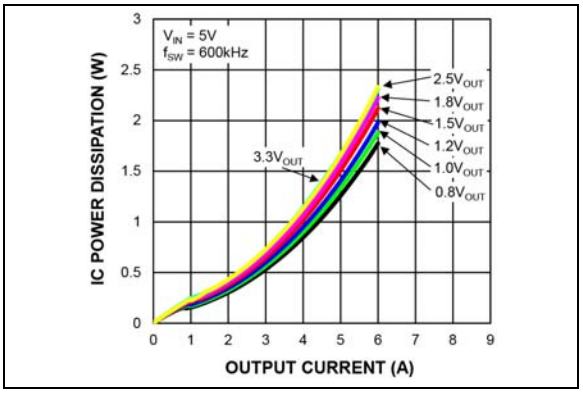


FIGURE 2-17: *IC Power Dissipation (V_{IN} = 5V) vs. Output Current.*

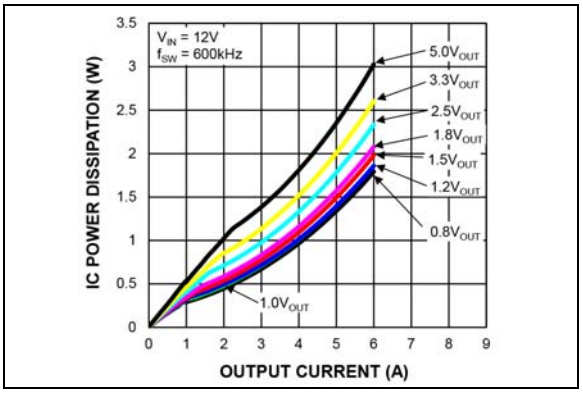


FIGURE 2-18: *IC Power Dissipation (V_{IN} = 12V) vs. Output Current.*

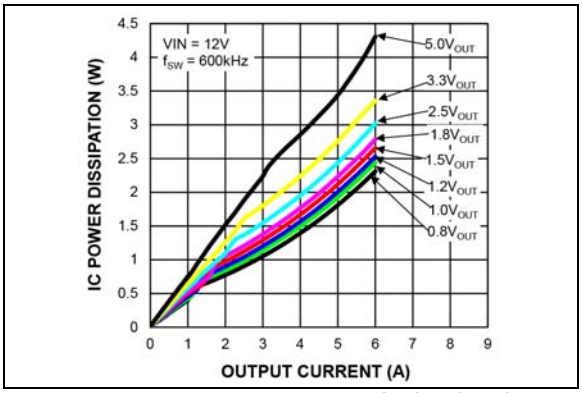


FIGURE 2-19: *IC Power Dissipation (V_{IN} = 24V) vs. Output Current.*

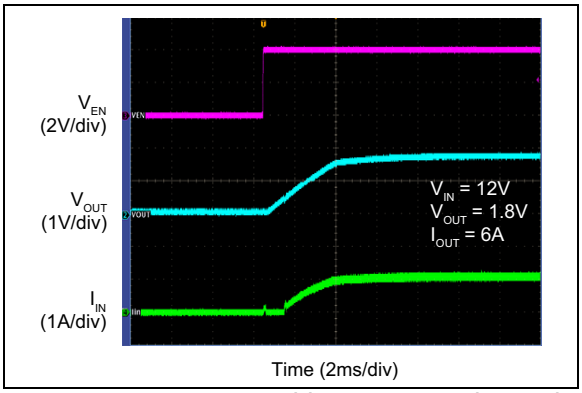


FIGURE 2-22: *Enable Turn-On Delay and Rise Time.*

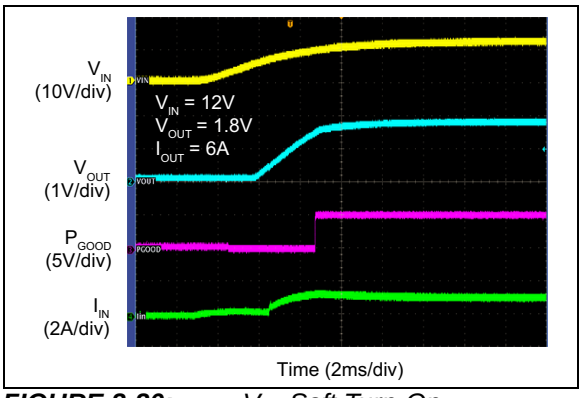


FIGURE 2-20: *V_{IN} Soft Turn-On.*

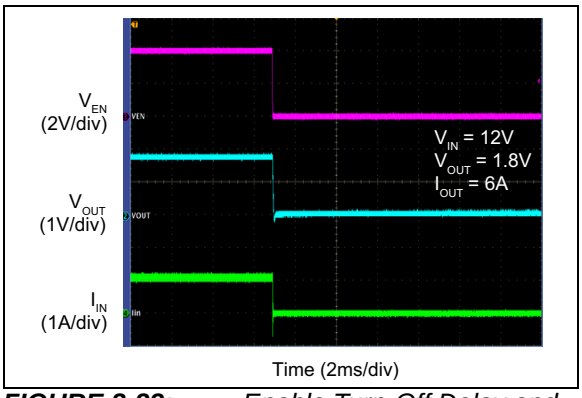


FIGURE 2-23: *Enable Turn-Off Delay and Fall Time.*

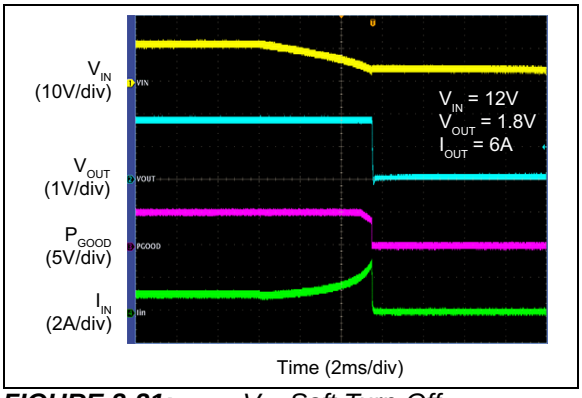


FIGURE 2-21: *V_{IN} Soft Turn-Off.*

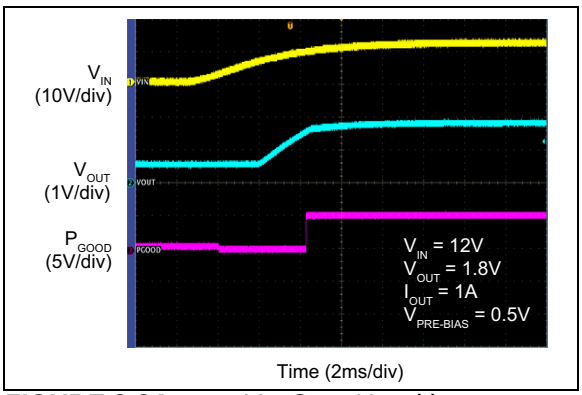


FIGURE 2-24: *V_{IN} Start-Up with Pre-Biased Output.*

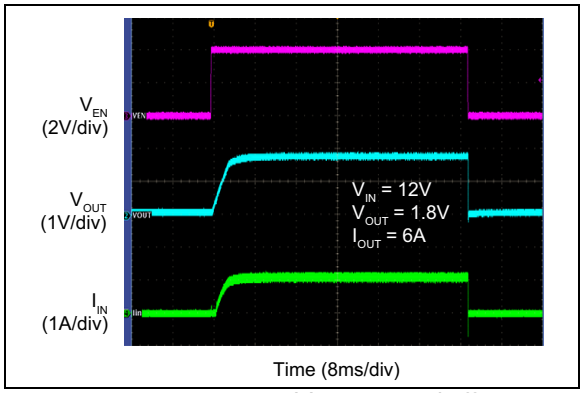


FIGURE 2-25: *Enable Turn-On/Off.*

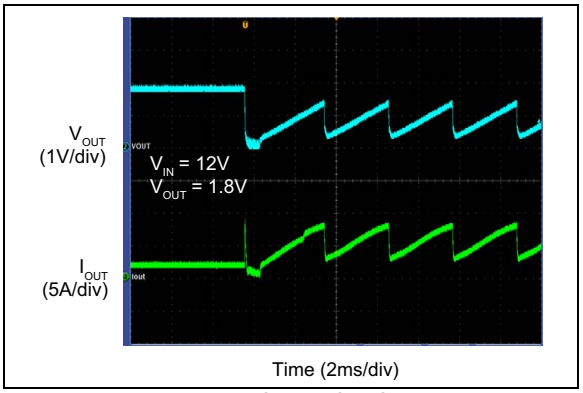


FIGURE 2-28: *Short-Circuit.*

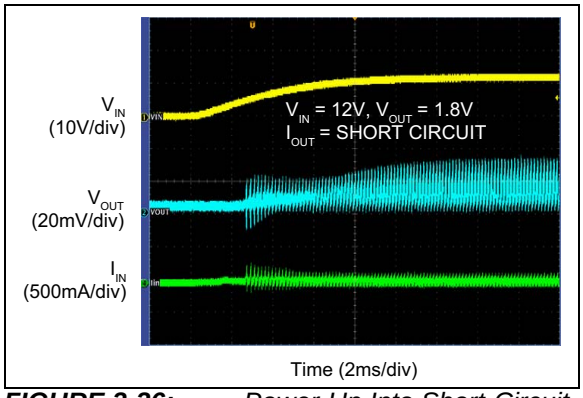


FIGURE 2-26: *Power-Up Into Short-Circuit.*

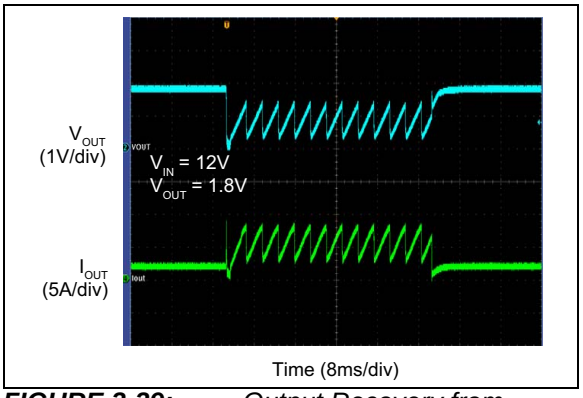


FIGURE 2-29: *Output Recovery from Short-Circuit.*

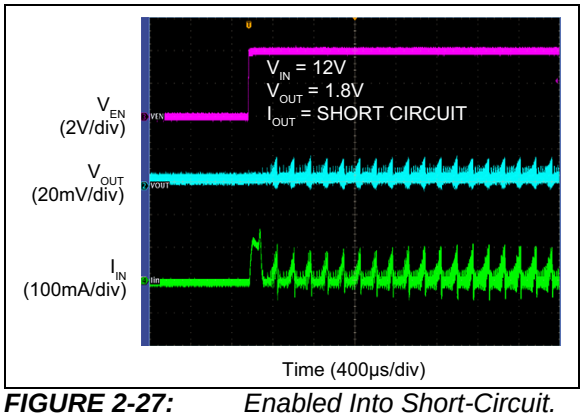


FIGURE 2-27: *Enabled Into Short-Circuit.*

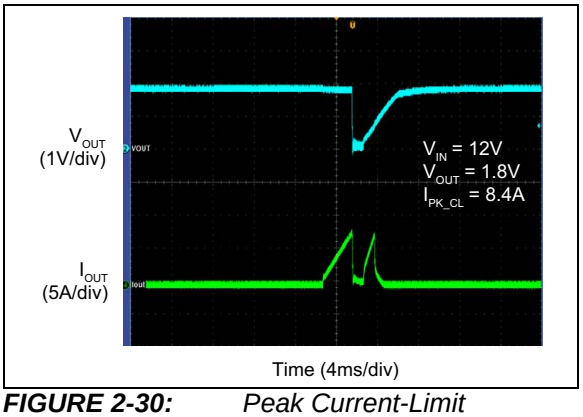


FIGURE 2-30: *Peak Current-Limit Threshold.*

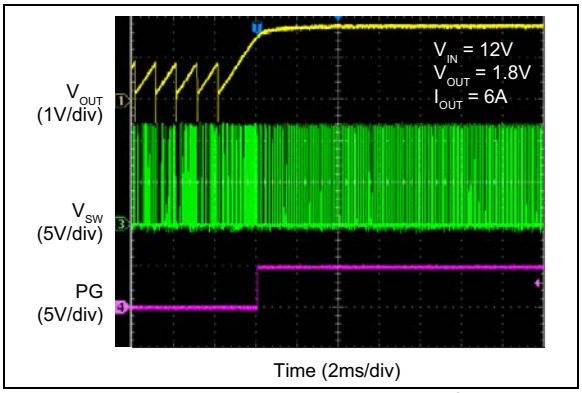


FIGURE 2-31: *Output Recovery from Thermal Shutdown.*

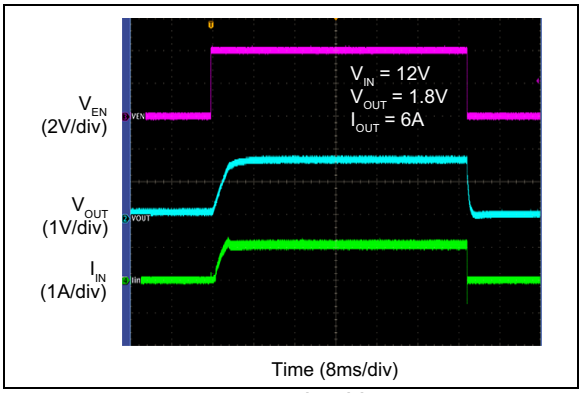


FIGURE 2-34: *Inrush with C_{OUT} = 3000 µF.*

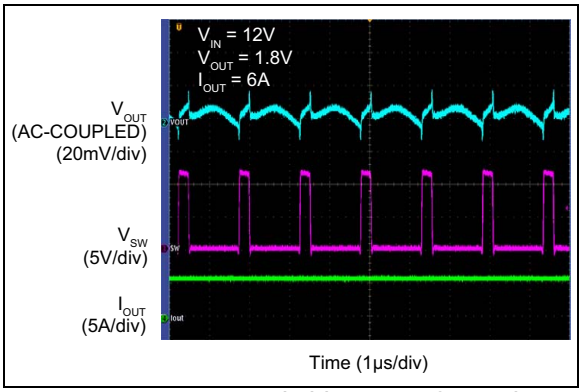


FIGURE 2-32: *Switching Waveforms (I_{OUT} = 6A).*

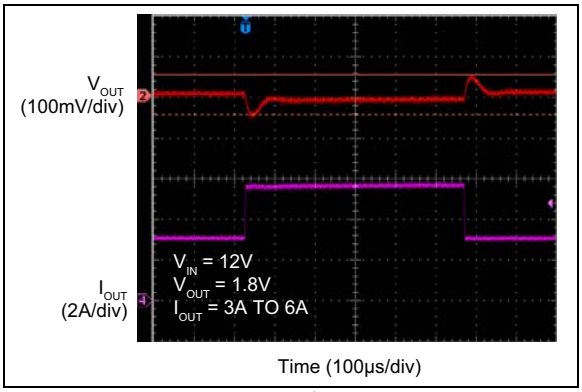


FIGURE 2-35: *Transient Response, MIC45205-1 (I_{OUT} = 3A to 6A).*

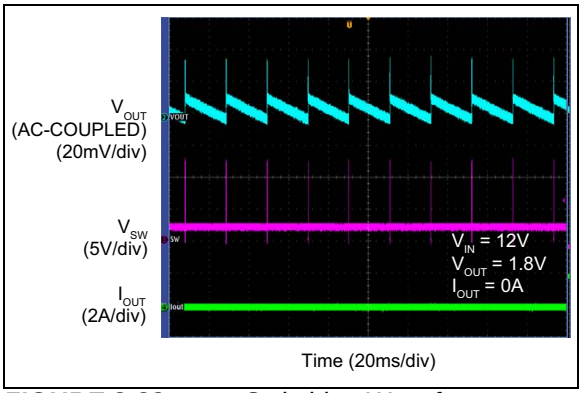


FIGURE 2-33: *Switching Waveforms, MIC45205-1 (I_{OUT} = 0A).*

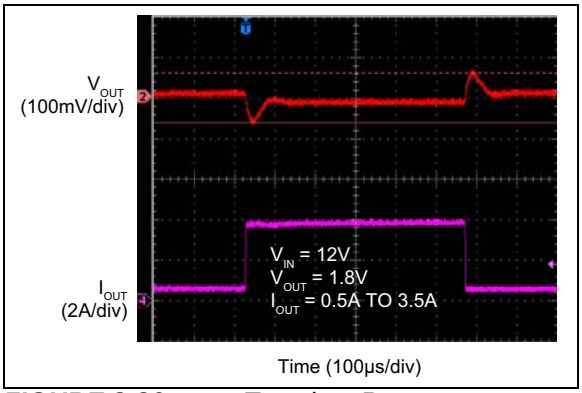


FIGURE 2-36: *Transient Response, MIC45205-1 (I_{OUT} = 0.5A to 3.5A).*

3.0 PIN DESCRIPTIONS

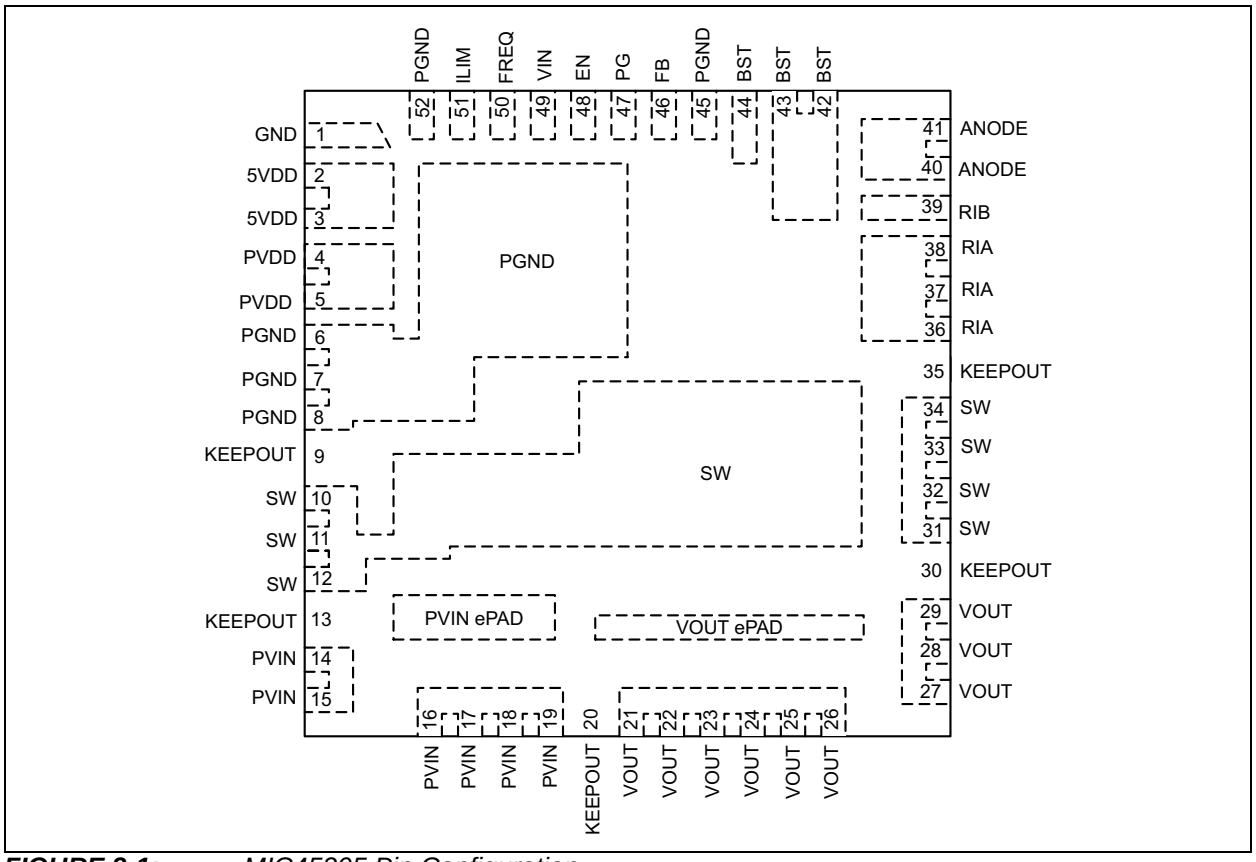


FIGURE 3-1: *MIC45205 Pin Configuration.*

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	GND	Analog Ground. Connect bottom feedback resistor to GND. GND and PGND are internally connected.
2, 3	$5V_{DD}$	Internal +5V Linear Regulator Output. Powered by V_{IN}, $5V_{DD}$ is the internal supply bus for the device. In the applications with V_{IN} < +5.5V, $5V_{DD}$ should be tied to V_{IN} to bypass the linear regulator.
4, 5	PV_{DD}	PV_{DD}. Supply input for the internal low-side power MOSFET driver.
6, 7, 8, 45, 52	PGND	Power Ground. PGND is the return path for the step-down power module power stage. The PGND pin connects to the sources of internal low-side power MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
10, 11, 12, 31, 32, 33, 34	SW	The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time.
14, 15, 16, 17, 18, 19	PV_{IN}	Power Input Voltage. Connection to the drain of the internal high-side power MOSFET. Connect an input capacitor from PV_{IN} to PGND.
21, 22, 23, 24, 25, 26, 27, 28, 29	V_{OUT}	Output Voltage. Connected to the internal inductor, the output capacitor should be connected from this pin to PGND as close to the module as possible.
36, 37, 38	RIA	Ripple Injection Pin A. Leave floating, no connection.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
39	RIB	Ripple Injection Pin B. Connect this pin to FB.
40, 41	ANODE	Anode Bootstrap Diode. Anode connection of internal bootstrap diode, this pin should be connected to the PV_{DD} pin.
42, 43, 44	BST	Connection to the internal bootstrap circuitry and high-side power MOSFET drive circuitry. Connect all three BST pins together.
46	FB	Feedback. Input to the transconductance amplifier of the control loop. The FB pin is referenced to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. Connect the bottom resistor from FB to GND.
47	PG	Power Good. Open-drain output. If used, connect to an external pull-up resistor of at least 10 kΩ between PG and the external bias voltage.
48	EN	Enable. A logic signal to enable or disable the step-down regulator module operation. The EN pin is TTL/CMOS compatible. Logic-high = enable, logic-low = disable or shutdown. EN pin has an internal 1 MΩ (typical) pull-down resistor to GND. Do not leave floating.
49	V_{IN}	Internal 5V Linear Regulator Input. A 1 µF ceramic capacitor from V_{IN} to GND is required for decoupling.
50	FREQ	Switching Frequency Adjust. Use a resistor divider from V_{IN} to GND to program the switching frequency. Connecting FREQ to V_{IN} sets frequency at 600 kHz.
51	ILIM	Current Limit. Connect a resistor between ILIM and SW to program the current limit.
9, 13, 20, 30, 35	KEEPOUT	Depopulated pin positions.
—	PV_{IN} ePAD	PV_{IN} Exposed Pad. Internally connected to PV_{IN} pins. Please see PCB Layout Guidelines section.
—	V_{OUT} ePAD	V_{OUT} Exposed Pad. Internally connected to V_{OUT} pins. Please see PCB Layout Guidelines section.

4.0 FUNCTIONAL DESCRIPTION

The MIC45205 is an adaptive on-time synchronous buck regulator module built for high-input voltage to low-output voltage conversion applications. The MIC45205 is designed to operate over a wide input voltage range, from 4.5V to 26V, and the output is adjustable with an external resistor divider. An adaptive on-time control scheme is employed to obtain a constant switching frequency in steady state and to simplify the control compensation. Hiccup mode overcurrent protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown. The module has integrated switching FETs, inductor, bootstrap diode, resistor, and capacitor.

4.1 Theory of Operation

As shown in Figure 4-1 (in association with Equation 4-1), the output voltage is sensed by the MIC45205 feedback pin (FB) via the voltage divider R_{FB1} and R_{FB2} and compared to a 0.8V reference voltage (V_{REF}) at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases, and the amplifier output falls below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

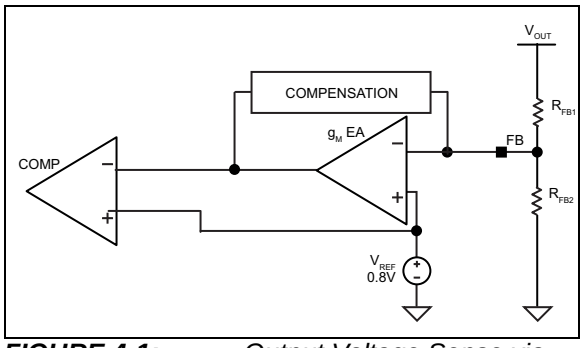


FIGURE 4-1: *Output Voltage Sense via FB Pin.*

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT}	Output Voltage
V_{IN}	Power Stage Input Voltage
f_{SW}	Switching Frequency

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier falls below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(MIN)}$, which is about 200 ns, the MIC45205 control logic will apply the $t_{OFF(MIN)}$ instead. $t_{OFF(MIN)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 200 ns $t_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{200ns}{t_S}$$

Where:

t_S $1/f_{SW}$

It is not recommended to use MIC45205 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC45205 during steady state operation. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 4-2 shows the MIC45205 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

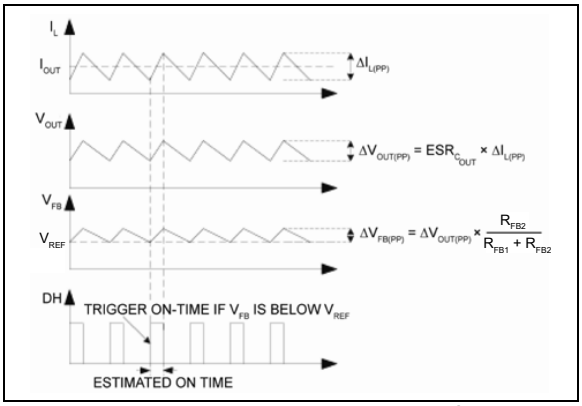


FIGURE 4-2: *MIC45205 Control Loop Timing.*

Figure 4-3 shows the operation of the MIC45205 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(MIN)}$ is generated to charge the bootstrap capacitor (C_{BST}) because the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small. Note that the instantaneous switching frequency during load transient remains bounded and cannot increase arbitrarily. The minimum is limited by $t_{ON} + t_{OFF(MIN)}$. Because the variation in V_{OUT} is relatively limited during load transient, t_{ON} stays virtually close to its steady-state value.

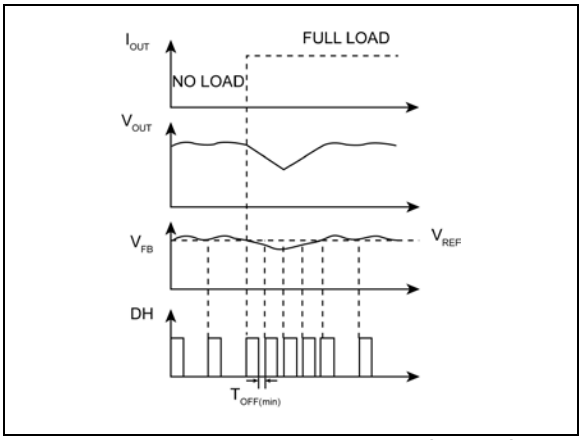


FIGURE 4-3: *MIC45205 Load Transient Response.*

Unlike true current-mode control, the MIC45205 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC45205 feedback voltage ripple should be in phase with the inductor current ripple and are large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV~100 mV over full input voltage range. If a low ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the Ripple Injection subsection in the Application Information section for more details about the ripple injection technique.

4.2 Discontinuous Mode (MIC45205-1 Only)

In continuous mode, the inductor current is always greater than zero. However, at light loads, the MIC45205-1 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 4-4. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current as the switching frequency is reduced. The MIC45205-1 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC45205-1 has a zero crossing comparator (ZC) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC45205-1 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC45205-1 goes into discontinuous mode, both DL and DH are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, and then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4-4 shows the control loop timing in discontinuous mode.

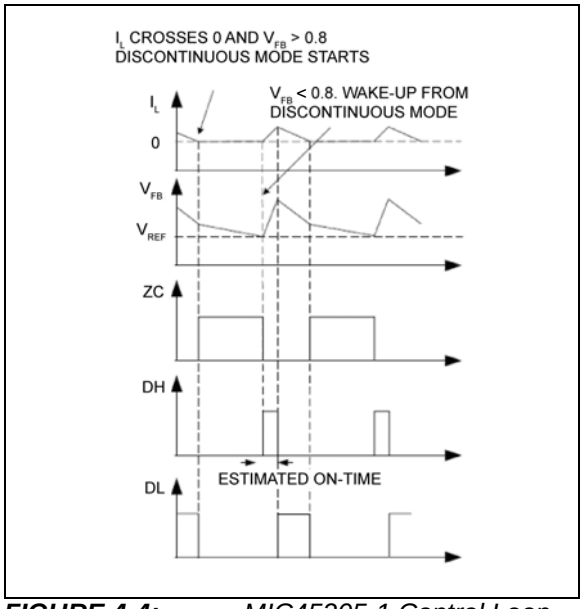


FIGURE 4-4: *MIC45205-1 Control Loop Timing (Discontinuous Mode).*

During discontinuous mode, the bias current of most circuits is substantially reduced. As a result, the total power supply current during discontinuous mode is only about 350 µA, allowing the MIC45205-1 to achieve high efficiency in light load applications.

4.3 Soft-Start

Soft-start reduces the input power supply surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up.

The MIC45205 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 5 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. PV_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

4.4 Current-Limit

The MIC45205 uses the $R_{DS(ON)}$ of the low-side MOSFET and external resistor connected from ILIM pin to SW node to set the current limit.

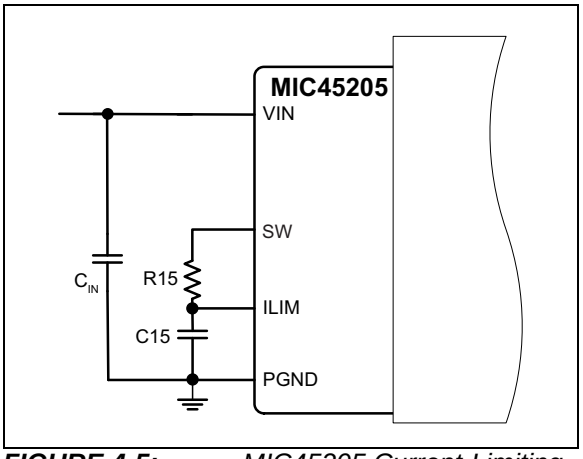


FIGURE 4-5: *MIC45205 Current-Limiting Circuit.*

In each switching cycle of the MIC45205, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage V_{ILIM} is compared with the power ground (PGND) after a blanking time of 150 ns. In this way the drop voltage over the resistor R15 (V_{CL}) is compared with the drop over the bottom FET generating the short current limit. The small capacitor (C15) connected from ILIM pin to PGND filters the switching node ringing during the off-time allowing a better short-limit measurement. The time constant created by R15 and C15 should be much less than the minimum off time.

The V_{CL} drop allows programming of short limit through the value of the resistor (R15). If the absolute value of the voltage drop on the bottom FET becomes greater than V_{CL}, and the V_{ILIM} falls below PGND, an overcurrent is triggered causing the IC to enter hiccup mode. The hiccup sequence including the soft-start reduces the stress on the switching FETs and protects the load and supply for severe short conditions.

The short-circuit current-limit can be programmed by using Equation 4-3.

EQUATION 4-3:

$$R15 = \frac{(I_{CLIM} - \Delta I_{L(PP)} \times 0.5) \times R_{DS(ON)} + V_{CL\_OFFSET}}{I_{CL}}$$

Where:

I_{CLIM}	Desired current limit.
$R_{DS(ON)}$	On-resistance of low-side power MOSFET, 16 mΩ typically.
V_{CL_OFFSET}	Current-limit threshold (typ. 14 mV).
I_{CL}	Current-limit source current (typ. 70 µA).
$\Delta I_{L(PP)}$	Inductor current peak-to-peak.

Because the inductor is integrated, use Equation 4-4 to calculate the inductor ripple current.

EQUATION 4-4:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The MIC45205 has a 1.0 µH inductor integrated into the module. In case of a hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft-start is under the folded short limit; otherwise the supply will go in hiccup mode and may not finish the soft-start successfully.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to I_{CLIM} in Equation 4-3 to avoid false current limiting due to increased MOSFET junction temperature rise.

With R15 = 1.37 kΩ and C15 = 15 pF, the typical output current-limit is 8A.

5.0 APPLICATION INFORMATION

5.1 Setting the Switching Frequency

The MIC45205 switching frequency can be adjusted by changing the value of resistors R1 and R2.

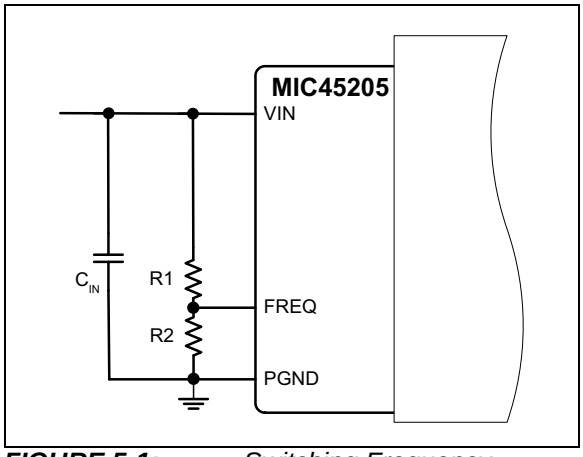


FIGURE 5-1: *Switching Frequency Adjustment.*

Equation 5-1 gives the estimated switching frequency:

EQUATION 5-1:

$$f_{SW} = f_O \times \frac{R2}{R1 + R2}$$

Where:

f_O	600 kHz (typical per the Electrical Characteristics table).
R1	100 kΩ is recommended.
R2	Needs to be selected in order to set the required switching frequency.

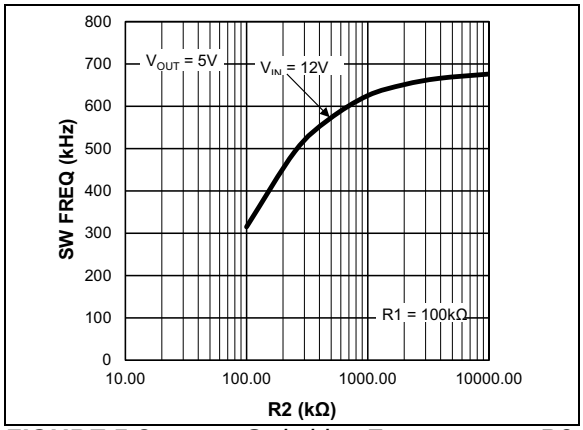


FIGURE 5-2: *Switching Frequency vs. R2.*

5.2 Output Capacitor Selection

The type of the output capacitor is usually determined by the application and its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are MLCC, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The MIC45205 requires ripple injection and the output capacitor ESR affects the control loop from a stability point of view.

The maximum value of ESR is calculated as in Equation 5-2:

EQUATION 5-2:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$	Peak-to-peak output voltage ripple
$\Delta I_{L(PP)}$	Peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-3:

EQUATION 5-3:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + (\Delta I_{L(PP)} \times ESR_{COUT})^2}$$

Where:

C_{OUT}	Output Capacitance Value
f_{SW}	Switching Frequency

As described in the Theory of Operation subsection in the Functional Description, the MIC45205 requires at least 20 mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to the Ripple Injection subsection in the Application Information section for more details.

The output capacitor RMS current is calculated in Equation 5-4:

EQUATION 5-4:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-5:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^{2} \times ESR_{COUT}$$

5.3 Input Capacitor Selection

The input capacitor for the power stage input PV_{IN} should be selected for ripple current rating and voltage rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-6:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-7:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

Where:

D	Duty cycle

The power dissipated in the input capacitor is:

EQUATION 5-8:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^{2} \times ESR_{CIN}$$

The general rule is to pick the capacitor with a ripple current rating equal to or greater than the calculated worst-case RMS capacitor current.

Equation 5-9 should be used to calculate the input capacitor. Also it is recommended to keep some margin on the calculated value:

EQUATION 5-9:

$$C_{IN} \approx \frac{I_{OUT(MAX)} \times (1 - D)}{f_{SW} \times dV}$$

Where:

dV	Input ripple
f_{SW}	Switching frequency

5.4 Output Voltage Setting Components

The MIC45205 requires two resistors to set the output voltage as shown in Figure 5-3:

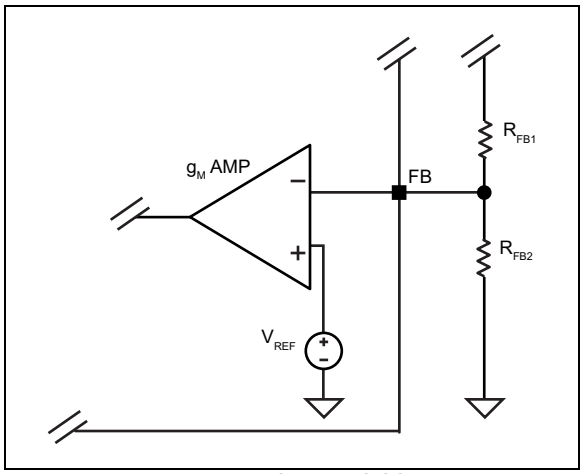


FIGURE 5-3: *Voltage-Divider Configuration.*

The output voltage is determined by Equation 5-10:

EQUATION 5-10:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Where:

V_{FB} 0.8V

A typical value of R_{FB1} used on the standard evaluation board is 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R_{FB1} is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_{FB1} is selected, R_{FB2} can be calculated using Equation 5-11:

EQUATION 5-11:

$$R_{FB2} = \frac{V_{FB} \times R_{FB1}}{V_{OUT} - V_{FB}}$$

For fixed R_{FB1} = 10 kΩ, output voltage can be selected by R_{FB2}. Table 5-1 provides R_{FB2} values for some common output voltages.

TABLE 5-1: V_{OUT} PROGRAMMING RESISTOR LOOK-UP

R_{FB2}	V_{OUT}
OPEN	0.8V
40.2 kΩ	1.0V
20 kΩ	1.2V
11.5 kΩ	1.5V
8.06 kΩ	1.8V
4.75 kΩ	2.5V
3.24 kΩ	3.3V
1.91 kΩ	5.0V

5.5 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC45205 g_m amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally too small to provide enough ripple amplitude at the FB pin and this issue is more visible in lower output voltage applications. If the feedback voltage ripple is so small that the g_m amplifier and error comparator cannot sense it, then the MIC45205 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into two situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors:

As shown in Figure 5-4, the converter is stable without any ripple injection.

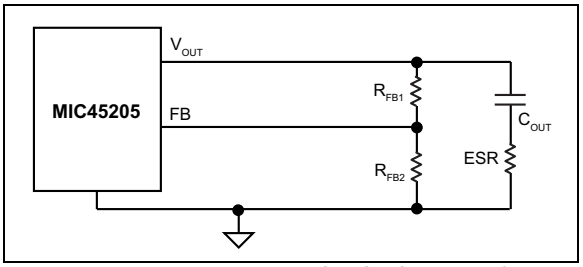


FIGURE 5-4: *Enough Ripple at FB from ESR.*

The feedback voltage ripple is:

EQUATION 5-12:

$$\Delta V_{FB(PP)} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times ESR_{COUT} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$ The peak-to-peak value of the inductor current ripple

2. Virtually no or inadequate ripple at the FB pin voltage due to the very-low ESR of the output capacitors, such is the case with ceramic output capacitor. In this case, the V_{FB} ripple waveform needs to be generated by injecting suitable signal. MIC45205 has provisions to enable an internal series RC injection network, R_{INJ} and C_{INJ} as shown in Figure 5-5 by connecting RIB to the FB pin. This network injects a square-wave current waveform into the FB pin, which, by means of integration across the capacitor (C14), generates an appropriate sawtooth FB ripple waveform.

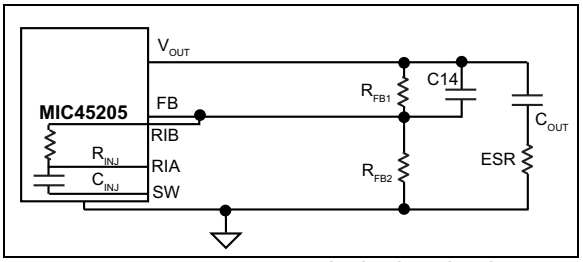


FIGURE 5-5: *Internal Ripple Injection at FB via RIB Pin.*

The injected ripple is:

EQUATION 5-13:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{div} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Where:

V_{IN}	Power stage input voltage
D	Duty cycle
f_{SW}	Switching frequency
τ	$(R_{FB1}//R_{FB2}//R_{INJ})$ x C14 R_{INJ} = 10 kΩ, C_{INJ} = 0.1 µF

EQUATION 5-14:

$$K_{div} = \frac{R_{FB1}//R_{FB2}}{R_{INJ} + R_{FB1}//R_{FB2}}$$

Where:

R_{INJ}	10 kΩ

In Equation 5-14 and Equation 5-15, it is assumed that the time constant associated with C14 must be much greater than the switching period:

EQUATION 5-15:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

If the voltage divider resistors R_{FB1} and R_{FB2} are in the kΩ range, then a C14 of 1 nF to 100 nF can easily satisfy the large time constant requirements.

5.6 Thermal Measurements and Safe Operating Area (SOA)

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36-gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

The safe operating area (SOA) of the MIC45205 is shown in Figure 5-6 through Figure 5-10. These thermal measurements were taken on MIC45205 evaluation board. Since the MIC45205 is an entire system comprised of switching regulator controller, MOSFETs and inductor, the part needs to be considered as a system. The SOA curves will give guidance to reasonable use of the MIC45205.

SOA curves should only be used as a point of reference. SOA data was acquired using the MIC45205 evaluation board. Thermal performance depends on the PCB layout, board size, copper thickness, number of thermal vias, and actual airflow.

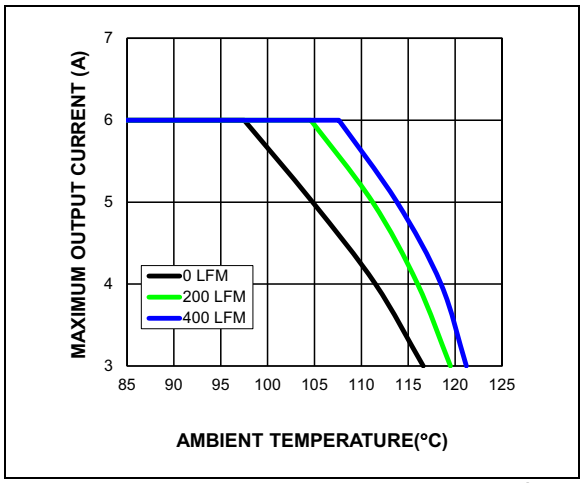


FIGURE 5-6: *MIC45205 Power Derating vs. Airflow (5V_{IN} to 1.5V_{OUT}).*

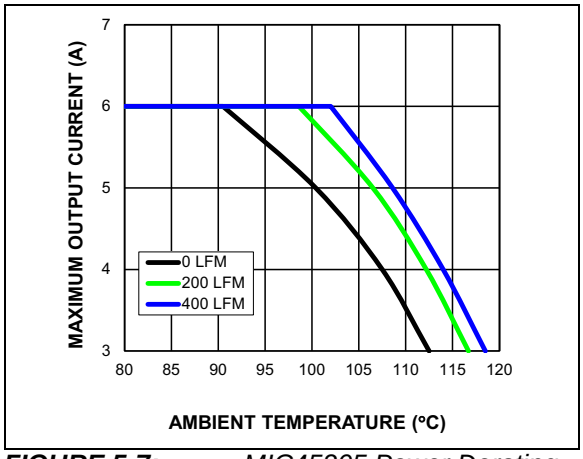


FIGURE 5-7: *MIC45205 Power Derating vs. Airflow (12V_{IN} to 1.5V_{OUT}).*

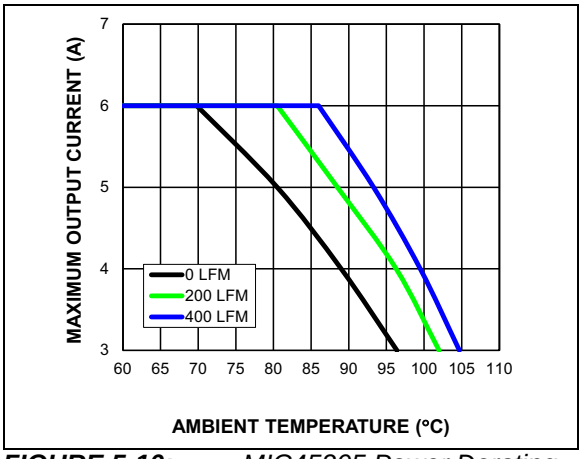


FIGURE 5-10: *MIC45205 Power Derating vs. Airflow (24V_{IN} to 3.3V_{OUT}).*

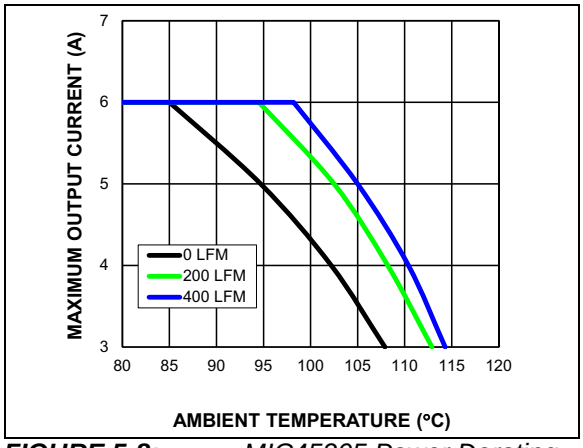


FIGURE 5-8: *MIC45205 Power Derating vs. Airflow (12V_{IN} to 3.3V_{OUT}).*

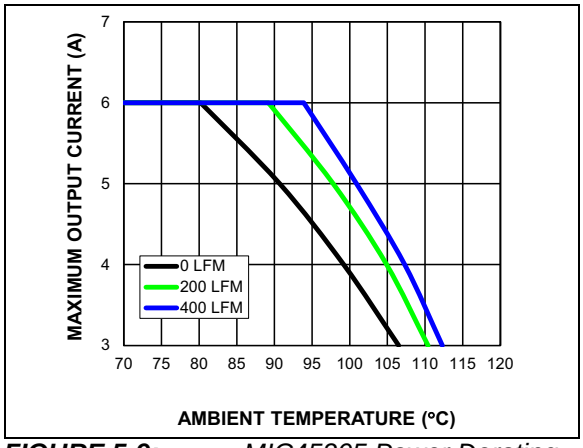


FIGURE 5-9: *MIC45205 Power Derating vs. Airflow (24V_{IN} to 1.5V_{OUT}).*

6.0 PCB LAYOUT GUIDELINES

To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

Figure 6-1 is optimized from a small form factor point of view shows top and bottom layer of a four layer PCB. It is recommended to use mid layer 1 as a continuous ground plane.

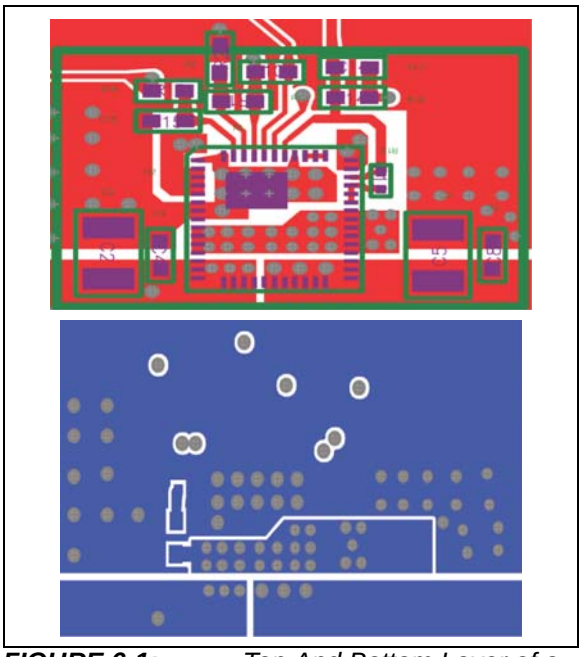


FIGURE 6-1: *Top And Bottom Layer of a Four-Layer Board.*

The following guidelines should be followed to insure proper operation of the MIC45205 module:

6.1 IC

- The analog ground pin (GND) must be connected directly to the ground planes. Place the IC close to the point-of-load (POL).
- Use thick traces to route the input and output power lines.
- Analog and power grounds should be kept separate and the analog ground (GND) and power ground (PGND) are internally connected.

6.2 Input Capacitor

- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the ceramic input capacitor.
- If a non-ceramic input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage.
- In “Hot-Plug” applications, an Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied. If hot-plugging is the normal operation of the system, using an appropriate hot-swap IC is recommended.

6.3 RC Snubber (Optional)

- Depending on the operating conditions, a RC snubber on the same side of the board can be used. Place the RC and as close to the SW pin as possible if needed.

6.4 SW Node

- Do not route any digital lines underneath or close to the SW node.
- Keep the switch node (SW) away from the feedback (FB) pin.

6.5 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

6.6 PCB Layout Recommendations

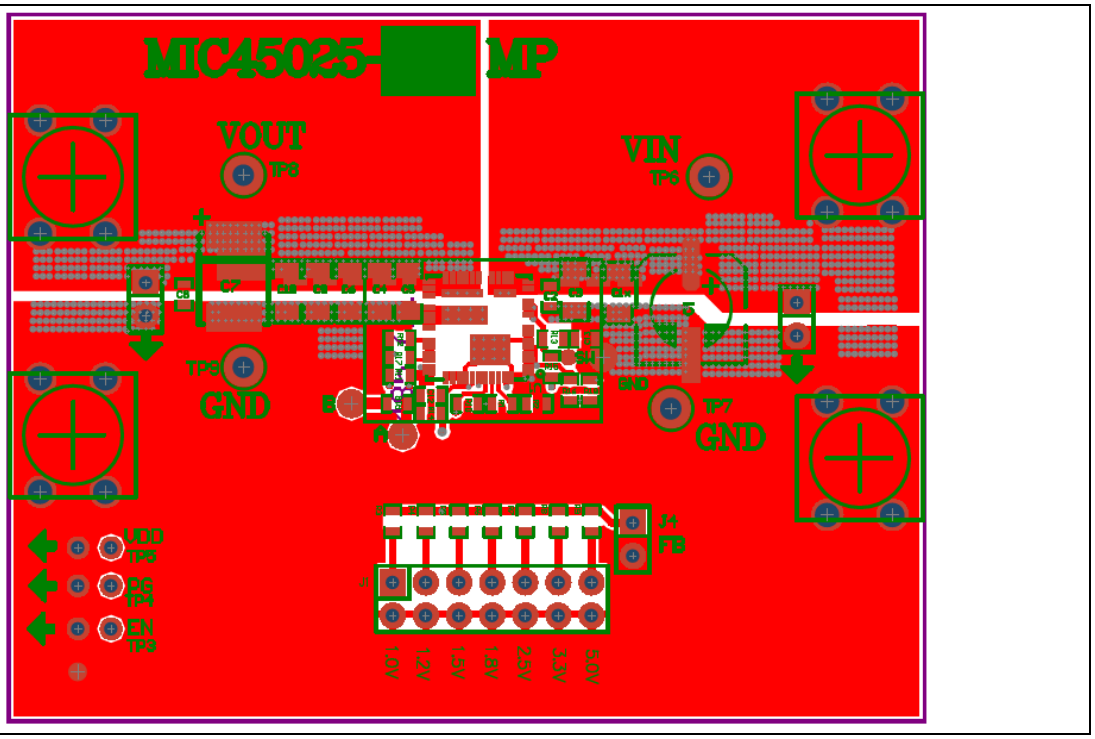


FIGURE 6-2: *Top Copper Layer 1.*

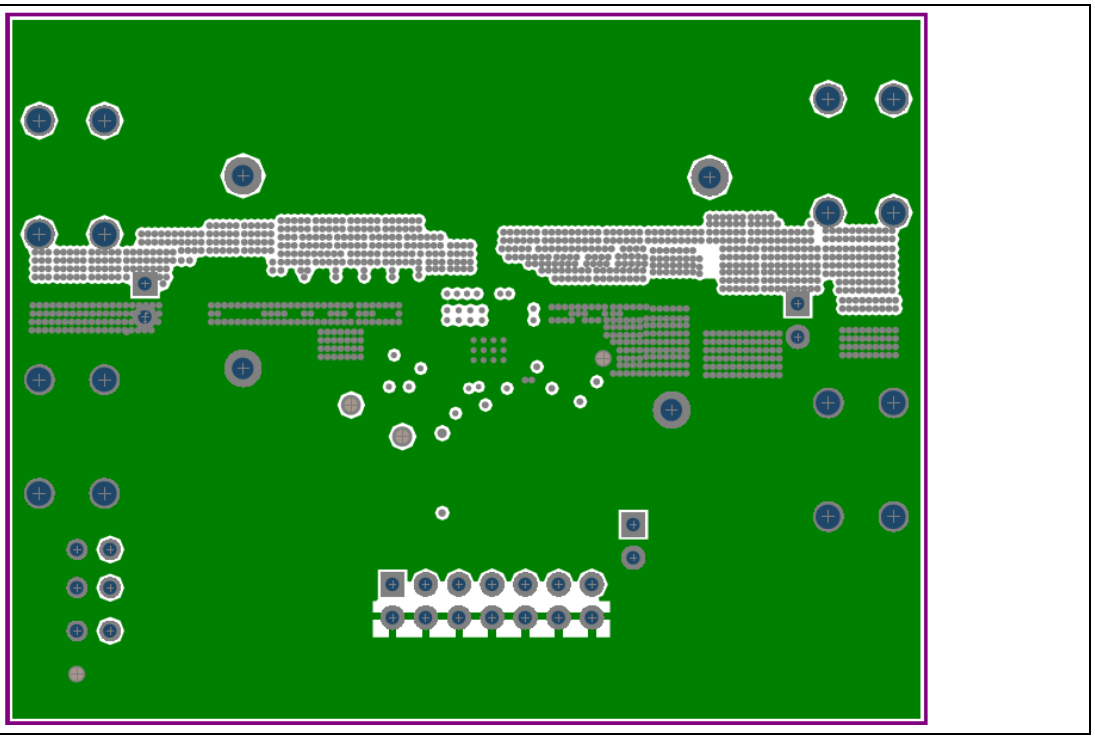


FIGURE 6-3: *Copper Layer2.*

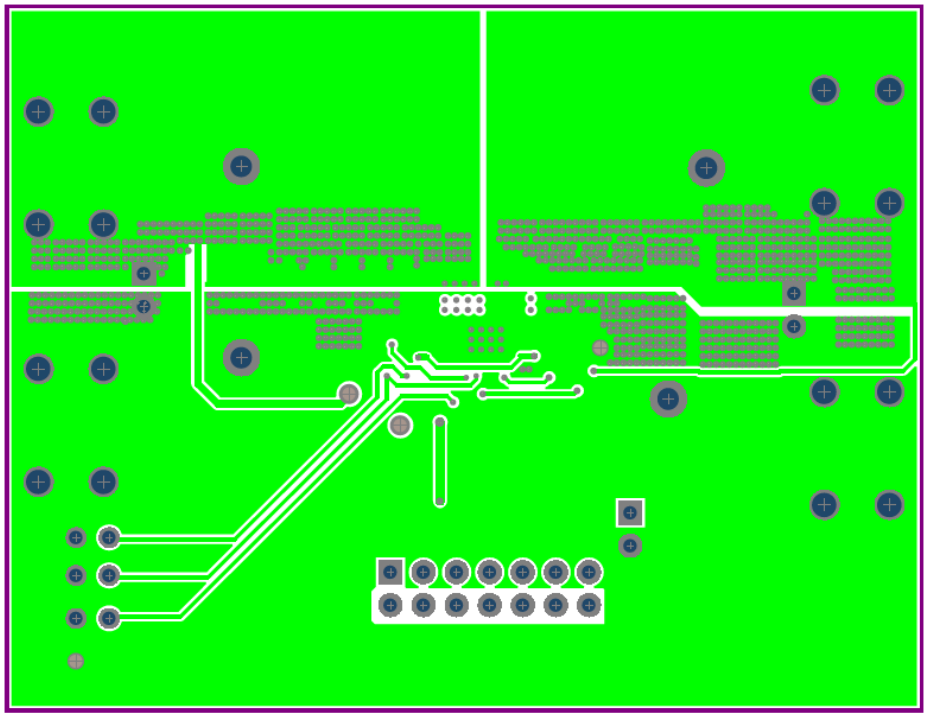


FIGURE 6-4: *Copper Layer 3.*

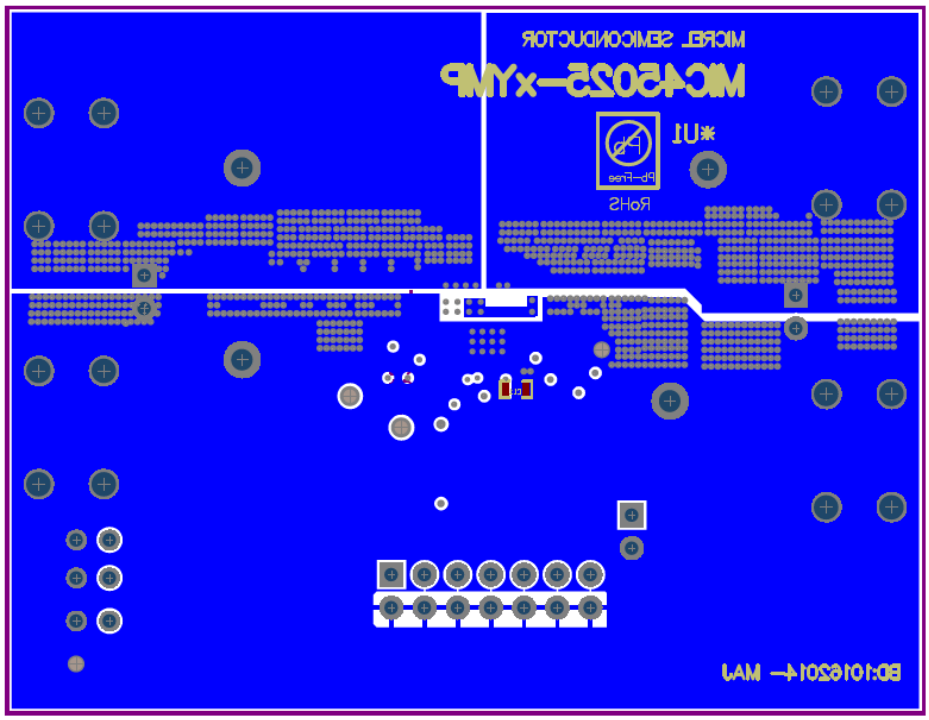


FIGURE 6-5: *Bottom Copper Layer 4.*

7.0 SIMPLIFIED PCB DESIGN RECOMMENDATIONS

7.1 Periphery I/O Pad Layout and Large Pad for Exposed Heatsink

The board design should begin with copper/metal pads that sit beneath the periphery leads of a mounted QFN. The board pads should extend outside the QFN package edge a distance of approximately 0.20 mm per side:

Total pad length = 8.00 mm + (0.20 mm per side × 2 sides) = 8.40 mm.

After completion of the periphery pad design, the larger exposed pads will be designed to create the mounting surface of the QFN exposed heatsink. The primary transfer of heat out of the QFN will be directly through the bottom surface of the exposed heatsink. To aid in the transfer of generated heat into the PCB, the use of an array of plated through-hole vias beneath the mounted part is recommended. The typical via hole diameter is 0.30 mm to 0.35 mm, with center-to-center pitch of 0.80 mm to 1.20 mm.

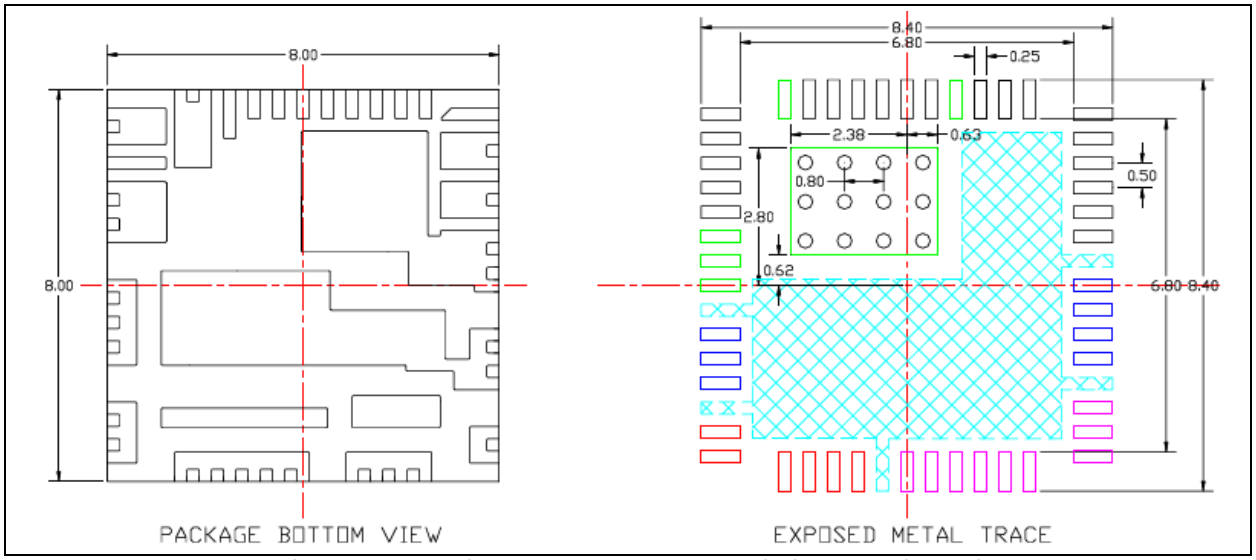


FIGURE 7-1: *Package Bottom View vs. PCB Recommended Exposed Metal Trace.*

Please note that the exposed metal trace is a “mirror image” of the package bottom view.

7.2 Solder Paste Stencil Design (Recommend Stencil Thickness = 112.5 µm ±12.5 µm)

The solder stencil aperture openings should be smaller than the periphery or large PCB exposed pads to reduce any chance of build-up of excess solder at the large exposed pad area which can result to solder bridging.

The suggested reduction of the stencil aperture opening is typically 0.20 mm smaller than exposed metal trace.

Please note that a critical requirement is to *not* duplicate land pattern of the exposed metal trace as solder stencil opening as the design and dimension values are different.

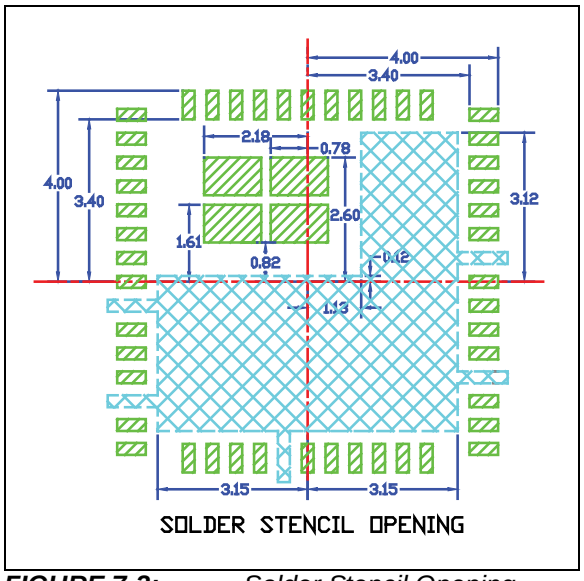


FIGURE 7-2: *Solder Stencil Opening.*

Note that the cyan-colored shaded pad indicates exposed trace keep out area.

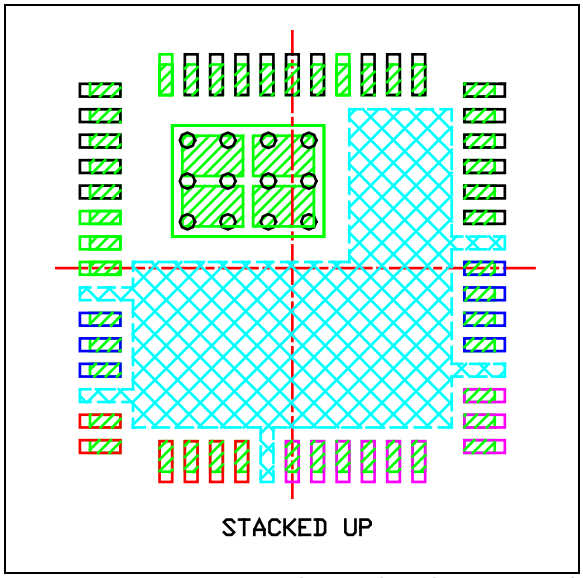


FIGURE 7-3: *Stack-Up of Pad Layout and Solder Paste Stencil.*

8.0 EVALUATION BOARD SCHEMATIC AND BOM

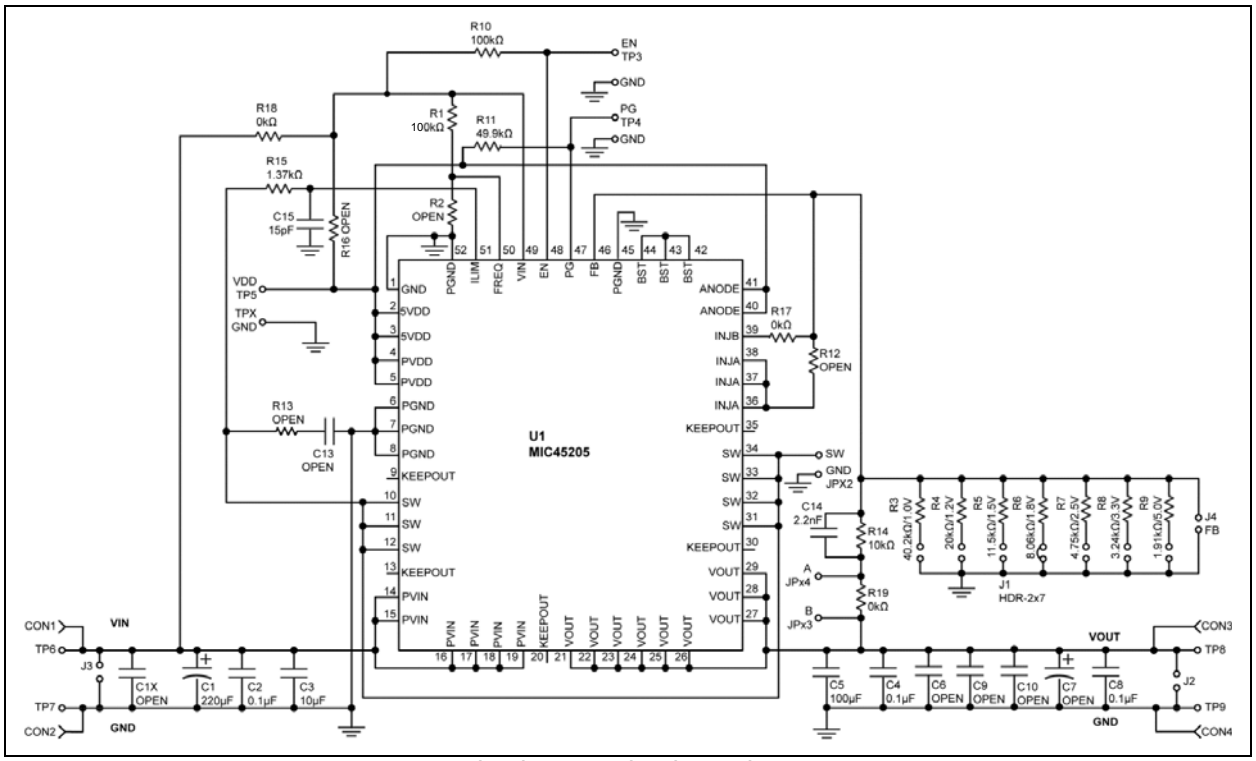


FIGURE 8-1: *MIC45205YML Evaluation Board Schematic.*

TABLE 8-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Quantity
C1	EEE-FK1V221P	Panasonic	220 µF/35V, ALE Capacitor (optional)	1
C1X, C6, C9, C10, C7, C13	—	—	Open	6
C3	C3216X5R1H106M160AB	TDK	10 µF/50V, 1206, X5R, 10%, MLCC	1
C2, C4, C8	GRM188R71H104KA93D	Murata	0.1 µF/50V, X7R, 0603, 10%, MLCC	3
C5	C3216X5R0J107M160AB	TDK	100 µF/6.3V, X5R, 1206, 20%, MLCC	1
C14	C1608C0G1H222JT	TDK	2.2 nF/50V, NP0, 0603, 5%, MLCC	1
C11	GRM1885C1H150JA01D	Murata	15 pF/50V, NP0, 0603, 5%, MLCC	3
CON1,CON2, CON3,CON4	8174	Keystone	15A, 4-Prong Through-Hole Screw Terminal	4
J1	M50-3500742	Harwin	Header 2x7	1
J2, J3, J4, TP3 – TP5	90120-0122	Molex	Header 2	6
JPx1, JPx2	—	—	Open	2
R1, R10	CRCW0603100K0FKEA	Vishay Dale	100 kΩ, 1%, 1/10W, 0603, Thick Film	2
R2, R12, R13, R16	—	—	Open	4
R3	CRCW060340K2FKEA	Vishay Dale	40.2 kΩ, 1%, 1/10W, 0603, Thick Film	1
R4	CRCW060320K0FKEA	Vishay Dale	20 kΩ, 1%, 1/10W, 0603, Thick Film	1
R5	CRCW060311K5FKEA	Vishay Dale	11.5 kΩ, 1%, 1/10W, 0603, Thick Film	1
R6	CRCW06038K06FKEA	Vishay Dale	8.06 kΩ, 1%, 1/10W, 0603, Thick Film	1
R7	CRCW06034K75FKEA	Vishay Dale	4.75 kΩ, 1%, 1/10W, 0603, Thick Film	1

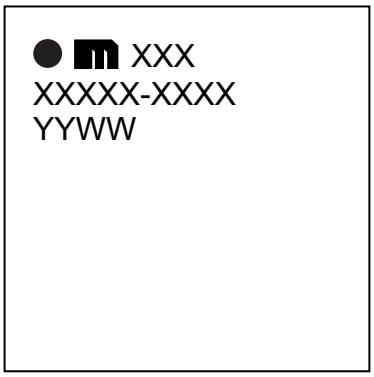
TABLE 8-1: BILL OF MATERIALS (CONTINUED)

Item	Part Number	Manufacturer	Description	Quantity
R8	CRCW06033K24FKEA	Vishay Dale	3.24 kΩ, 1%, 1/10W, 0603, Thick Film	1
R9	CRCW06031K91FKEA	Vishay Dale	1.91 kΩ, 1%, 1/10W, 0603, Thick Film	1
R11	CRCW060349K9FKEA	Vishay Dale	49.9 kΩ, 1%, 1/10W, 0603, Thick Film	1
R14	CRCW060310K0FKEA	Vishay Dale	10 kΩ, 1%, 1/10W, 0603, Thick Film	1
R15	CRCW06031K37FKEA	Vishay Dale	1.37 kΩ, 1%, 1/10W, 0603, Thick Film	1
R17, R18, R19	RCG06030000Z0EA	Vishay Dale	0Ω Resistor, 1%, 1/10W, 0603, Thick Film	3
TP6 – TP9, JPx3, JPx4	1502-2	Keystone	Single-End, Through-Hole Terminal	6
U1	MIC45205-1YMP	Microchip	26V/6A DC/DC Power Module	1
	MIC45205-2YMP			

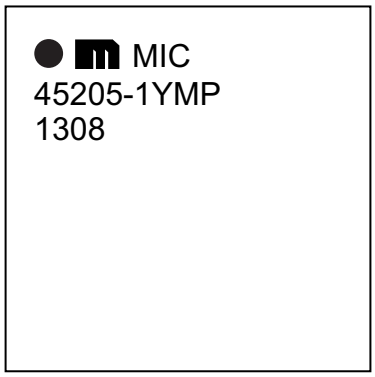
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

52-Pin QFN*



Example

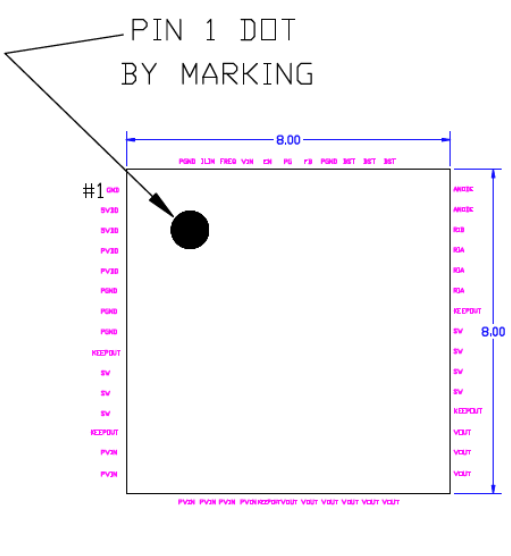


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

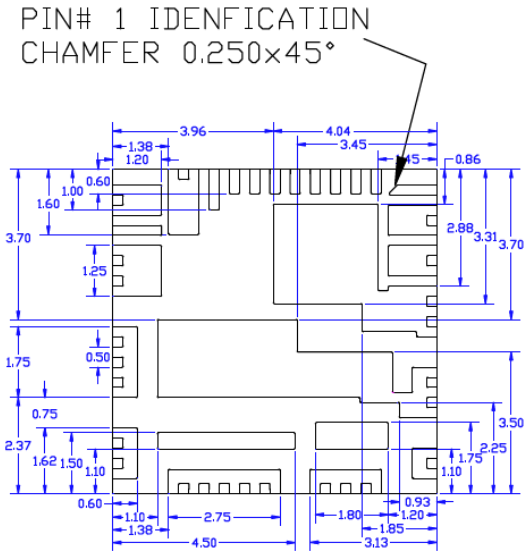
52-Lead 8 mm x 8 mm H3QFN Package Outline and Recommended Land Pattern

TITLE
52 LEAD H3QFN 8x8mm PACKAGE (Module) OUTLINE & RECOMMENDED LAND PATTERN

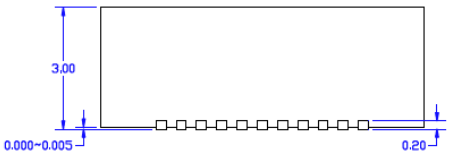
DRAWING #	H3QFN88-52LD-PL-1	**UNIT**	MM
Lead Frame	Copper	**Lead Finish**	Matte Tin



Top View
NOTE: 1, 2, 3



Bottom View
NOTE: 1, 2, 3

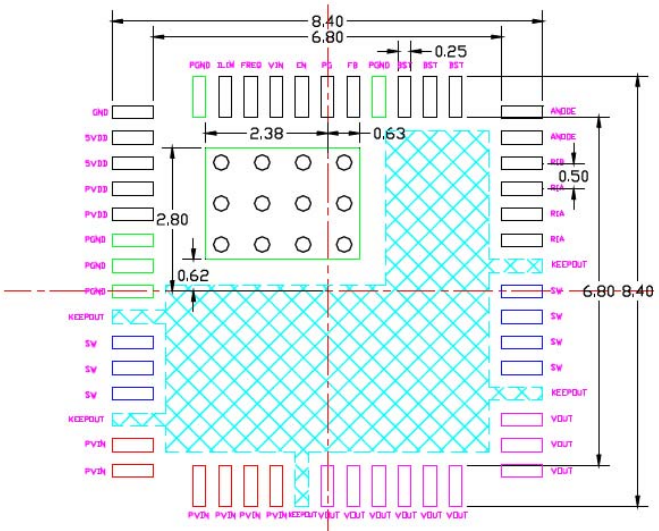


Side View
NOTE: 1, 2, 3

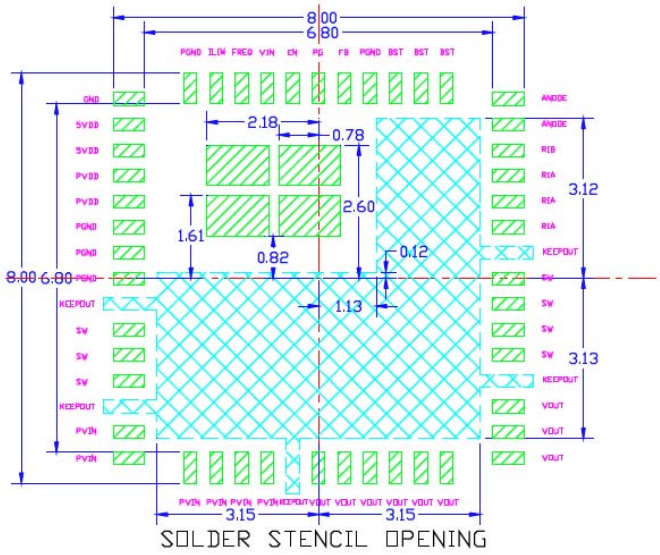
Recommended Land Pattern

NOTE: 4, 5, 6

Simplified LP



EXPOSED METAL TRACE



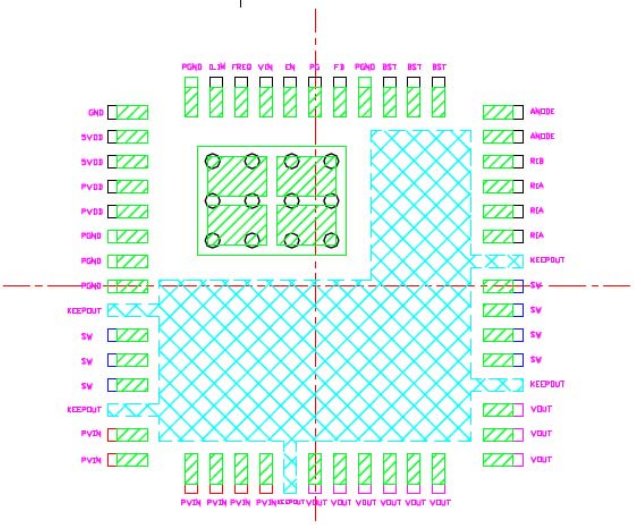
SOLDER STENCIL OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

Recommended Land Pattern

NOTE: 4, 5, 6

Simplified LP



STACKED UP

NOTE:

1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. BLACK CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, RECOMMENDED SIZE IS 0.30-0.35mm, AT 0.80mm PITCH & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. CYAN COLORED SHADED PAD REPRESENT EXPOSED TRACE KEEP OUT AREA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

Thermally Enhanced Land Pattern

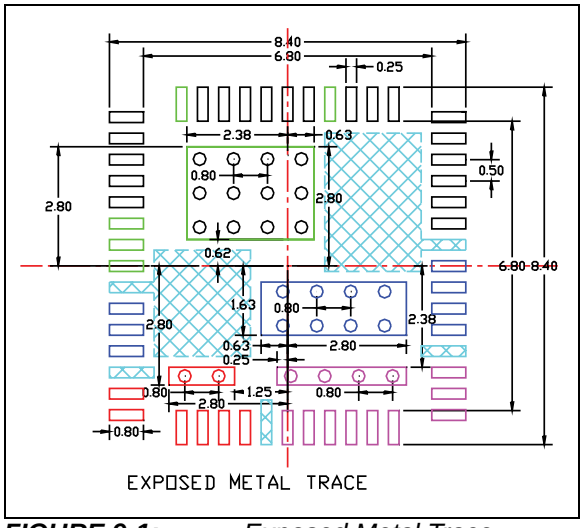


FIGURE 9-1: *Exposed Metal Trace.*

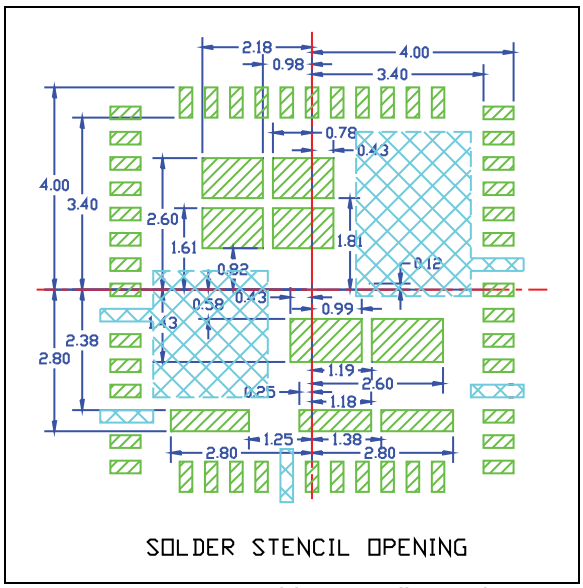


FIGURE 9-2: *Solder Stencil Opening.*

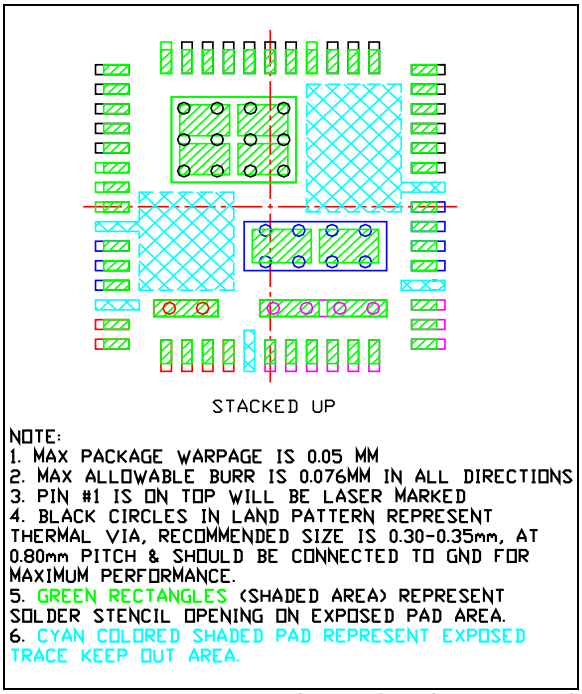


FIGURE 9-3: *Stack-Up of Pad Layout and Solder Paste Stencil and Notes.*

APPENDIX A: REVISION HISTORY

Revision A (June 2017)

- Converted Micrel document MIC45205 to Microchip data sheet DS20005798A.
- Minor text changes throughout.
- Updated maximum output voltage from 5.5V to 0.85 x V_{IN} in Features and General Description.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–X	X	XX	–XX
Device	Features	Temperature	Package	Media Type

Device:	MIC45205:		26V/6A DC/DC Power Module
Features:	1	=	HyperLight Load
	2	=	Hyper Speed Control
Temperature:	Y	=	–40°C to +125°C
Package:	MP	=	52-Lead 8 mm x 8 mm x 3 mm QFN
Media Type:	T1	=	100/Reel
	TR	=	1,500/Reel

Examples:

a) MIC45205-1YMP-T1: 26V/6A DC/DC Power Module, HyperLight Load, –40°C to +125°C, 52-Lead 8 mm x 8 mm x 3 mm QFN, 100/Reel

b) MIC45205-1YMP-TR: 26V/6A DC/DC Power Module, HyperLight Load, –40°C to +125°C, 52-Lead 8 mm x 8 mm x 3 mm QFN, 1,500/Reel

c) MIC45205-2YMP-T1: 26V/6A DC/DC Power Module, Hyper Speed Control, –40°C to +125°C, 52-Lead 8 mm x 8 mm x 3 mm QFN, 100/Reel

d) MIC45205-2YMP-TR: 26V/6A DC/DC Power Module, Hyper Speed Control, –40°C to +125°C, 52-Lead 8 mm x 8 mm x 3 mm QFN, 1,500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-1845-0

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820