

HIGH FREQUENCY HALF-BRIDGE GATE DRIVER WITH PROGRAMMABLE DEADTIME IN W-DFN3030-10 (Type TH)

Description

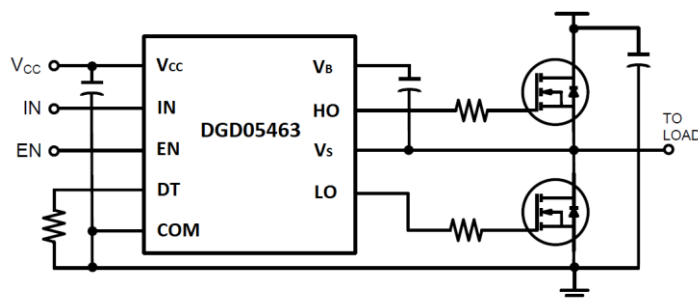
The DGD05463 is a high-frequency half-bridge gate driver capable of driving N-channel MOSFETs in a half-bridge configuration. The floating high-side driver is rated up to 50V.

The DGD05463 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. UVLO for high-side and low-side will protect a MOSFET with loss of supply. To protect MOSFETs, cross conduction prevention logic prevents the HO and LO outputs being on at the same time.

Fast and well-matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design using smaller associated components. The DGD05463 is offered in the W-DFN3030-10 (Type TH) package and operates over an extended -40°C to +125°C temperature range.

Applications

- DC-DC Converters
- Motor Controls
- Battery Powered Hand Tools
- eCig Devices
- Class D Power Amplifiers



Typical Configuration

Features

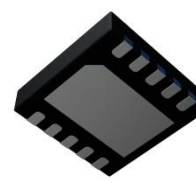
- 50V Floating High-Side Driver
- Drives Two N-Channel MOSFETs in a Half-Bridge Configuration
- 1.5A Source / 2.5A Sink Output Current Capability
- Internal Bootstrap Diode Included
- Undervoltage Lockout for High-Side and Low-Side Drivers
- Programmable Deadtime to Protect MOSFETs
- Logic Input (IN and EN) 3.3V Capability
- Ultra Low Standby Currents (<1µA)
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

- Case: W-DFN3030-10 (Type TH)
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish—Matte Tin Finish. Solderable per MIL-STD-202, Method 208③
- Weight: 0.017 grams (Approximate)



Top View



Bottom View

W-DFN3030-10 (Type TH)

Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DGD05463FN-7	DGD05463	7	8	3000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



DGD05463 = Product Type Marking Code
YY = Year (ex: 18 = 2018)
WW = Week (01 to 53)

Pin	Function
1	V _{CC}
2	V _B
3	HO
4	V _S
5	NC
10	LO
9	COM
8	IN
7	EN
6	DT

Top View: W-DFN3030-10 (Type TH)

Pin Number	Pin Name	Function
1	V _{CC}	Low-Side and Logic Supply
2	V _B	High-Side Floating Supply
3	HO	High-Side Gate Drive Output
4	V _S	High-Side Floating Supply Return
5	NC	No Connection (No Internal Connection)
6	DT	Deadtime Control
7	EN	Logic Input Enable, a Logic Low Turns Off Gate Driver
8	IN	Logic Input for High-Side and Low-Side Gate Driver Outputs (HO and LO), in Phase with HO
9	COM	Low-Side and Logic Return
10	LO	Low-Side Gate Drive Output
PAD	Substrate	Connect to COM on PCB

The schematic diagram of the DGD05463 driver IC illustrates its internal components and external connections. The IC is powered by VCC and VBB, with VSS and COM as ground references. The input pins IN, DT, and EN are connected to the internal logic through inverters and buffers. The output pins HO and LO are connected to the external load through transistors. The internal logic includes a DEAD TIME CONTROL block, an HV LEVEL SHIFT block, and two S-Q flip-flops. A dashed box labeled 'High Side Well' encloses the HV LEVEL SHIFT and the top S-Q flip-flop. The UV DETECT block is connected to VCC and VBB. The DELAY block is connected to the output of the DEAD TIME CONTROL block and the input of the bottom S-Q flip-flop.

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V _B	-0.3 to +60	V
High-Side Floating Negative Supply Voltage	V _S	V _B -14 to V _B +0.3	V
High-Side Floating Output Voltage	V _{HO}	V _S -0.3 to V _B +0.3	V
Offset Supply Voltage Transient	dV _S / dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V _{CC}	-0.3 to +14	V
Low-Side Output Voltage	V _{LO}	-0.3 to V _{CC} +0.3	V
Logic Input Voltage (IN and EN)	V _{IN}	-0.3 to V _{CC} +0.3	V

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P _D	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	R _{θJC}	42	°C/W
Operating Temperature	T _J	+150	°C
Lead Temperature (Soldering, 10s)	T _L	+300	
Storage Temperature Range	T _{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V _B	V _S + 4.2	V _S + 14	V
High-Side Floating Supply Offset Voltage	V _S	(Note 6)	50 (Note 7)	V
High-Side Floating Output Voltage	V _{HO}	V _S	V _B	V
Logic and Low Side Fixed Supply Voltage	V _{CC}	4.5 (Note 8)	14	V
Low-Side Output Voltage	V _{LO}	0	V _{CC}	V
Logic Input Voltage (IN and EN)	V _{IN}	0	5	V
Ambient Temperature	T _A	-40	+125	°C

- Notes:
- Logic operation for V_S of -5V to +50V.
 - Provided V_B doesn't exceed absolute maximum rating of 60V.
 - For operation of V_{CC} = 4.5V to 4.9V, an external bootstrap Schottky diode (0.3V V_{FD}, 1A) is necessary, see Figure 3. For operation V_{CC} ≥ 4.9V, the external Schottky diode is not required.

DC Electrical Characteristics

($V_{CC} = V_{BS} = 12V$, $COM = V_S = 0V$, @ $T_A = +25^\circ C$, unless otherwise specified.) (Note 9)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Logic "1" Input Voltage	V_{IH}	2.4	—	—	V	—
Logic "0" Input Voltage	V_{IL}	—	—	0.8	V	—
Enable Logic "1" Input Voltage	V_{ENIH}	1.5	—	—	V	—
Enable Logic "0" Input Voltage	V_{ENIL}	—	—	0.7	V	—
Input Voltage Hysteresis	V_{INHYS}	—	0.6	—	V	—
High Level Output Voltage, $V_{BIAS} - V_O$	V_{OH}	—	0.45	0.6	V	$I_{O+} = 100mA$
Low Level Output Voltage, V_O	V_{OL}	—	0.15	0.22	V	$I_{O-} = 100mA$
Offset Supply Leakage Current	I_{LK}	—	10	50	μA	$V_B = V_S = 60V$
V_{CC} Shutdown Supply Current	I_{CCSD}	—	0	1	μA	$V_{IN} = 0V$ or $5V$, $V_{EN} = 0V$
V_{CC} Quiescent Supply Current	I_{CCQ}	—	0.28	0.5	mA	$V_{IN} = 0V$ or $5V$, $R_{DT} = 100k\Omega$
V_{CC} Operating Supply Current	I_{CCOP}	—	7.6	—	mA	$f_s = 500kHz$, $C_L = 1000pF$
V_{BS} Quiescent Supply Current	I_{BSQ}	—	32	100	μA	$V_{IN} = 0V$ or $5V$
V_{BS} Operating Supply Current	I_{BSOP}	—	7.6	—	mA	$f_s = 500kHz$, $C_L = 1000pF$
Logic "1" Input Bias Current	I_{IN+}	—	25	60	μA	$V_{IN} = 5V$
Logic "0" Input Bias Current	I_{IN-}	—	0	1	μA	$V_{IN} = 0V$
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	3.3	3.8	4.2	V	—
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	2.9	3.3	3.9	V	—
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	3.3	3.8	4.2	V	—
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	2.9	3.3	3.9	V	—
Output High Short-Circuit Pulsed Current	I_{O+}	1.0	1.5	—	A	$V_O = 0V$, $PW \leq 10\mu s$
Output Low Short-Circuit Pulsed Current	I_{O-}	1.9	2.5	—	A	$V_O = 15V$, $PW \leq 10\mu s$
Forward Voltage of Bootstrap Diode	V_{F1}	—	0.67	—	V	$I_F = 100\mu A$
Forward Voltage of Bootstrap Diode	V_{F2}	—	1.7	—	V	$I_F = 100mA$

Note: 9. The V_{IN} and I_{IN} parameters are applicable to the two logic pins: IN and EN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO.

AC Electrical Characteristics

($V_{CC} = V_{BS} = 12V$, $COM = V_S = 0V$, $C_L = 1000pF$, @ $T_A = +25^\circ C$, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Turn-on Propagation Delay, HO & LO	t_{ON}	65	96	125	ns	$R_{DT} = 10k\Omega$
		350	463	580	ns	$R_{DT} = 100k\Omega$
Turn-off Propagation Delay, HO & LO	t_{OFF}	—	22	56	ns	—
Turn-on Rise Time	t_R	—	17	35	ns	—
Turn-off Fall Time	t_F	—	12	25	ns	—
Delay Matching	t_{DM}	—	—	50	ns	—
Deadtime: $t_{DT LO-HO}$ & $t_{DT HO-LO}$	t_{DT}	40	70	100	ns	$R_{DT} = 10k\Omega$
		300	430	560	ns	$R_{DT} = 100k\Omega$
Deadtime Matching	t_{MDT}	—	—	50	ns	$R_{DT} = 100k\Omega$

Timing Waveforms

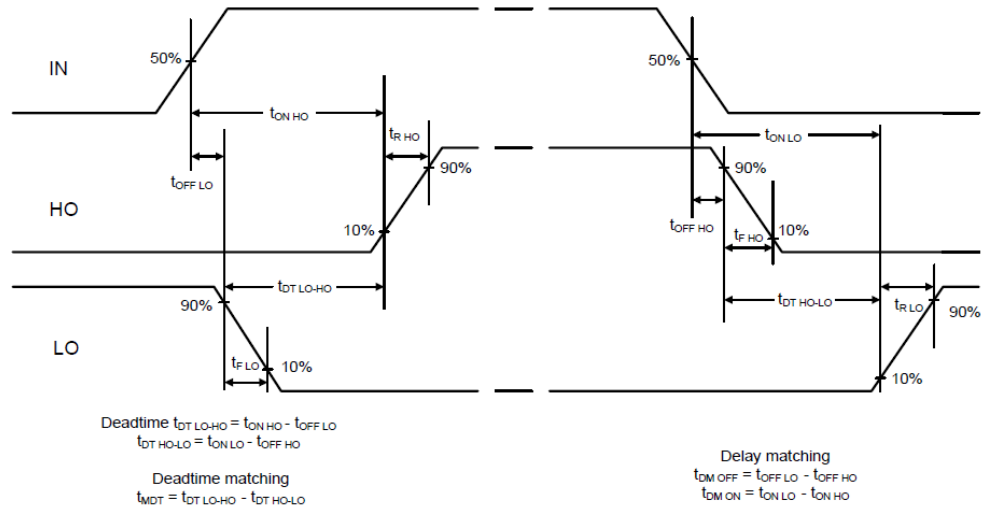


Figure 1. Switching Time Waveform Definitions

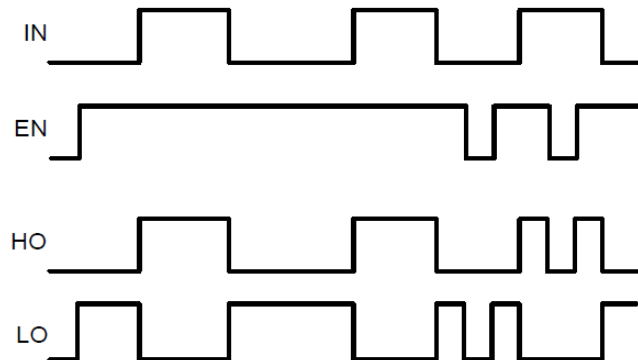


Figure 2. Input / Output Timing Diagram

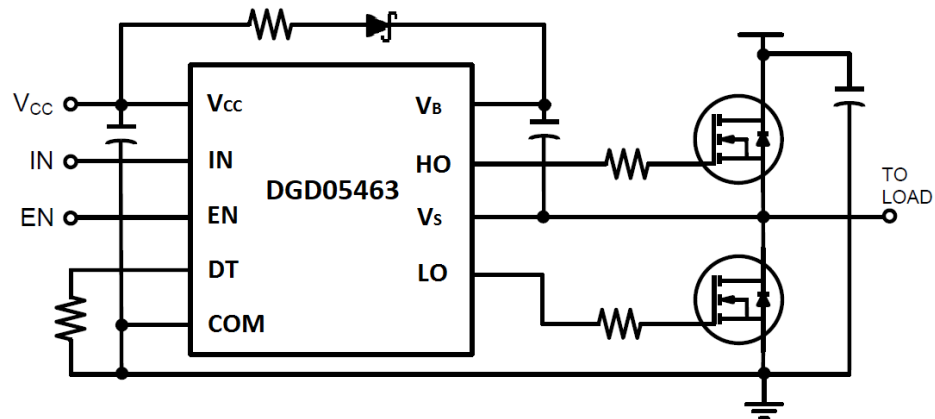


Figure 3. Typical application necessary for $V_{CC} = 4.5V$ to $4.9V$ operation. For $V_{CC} \geq 4.9V$, the bootstrap Schottky diode (0.3V Voltage drop, 1A) and resistor are not required.

Typical Performance Characteristics (@T_A = +25°C, unless otherwise specified.)

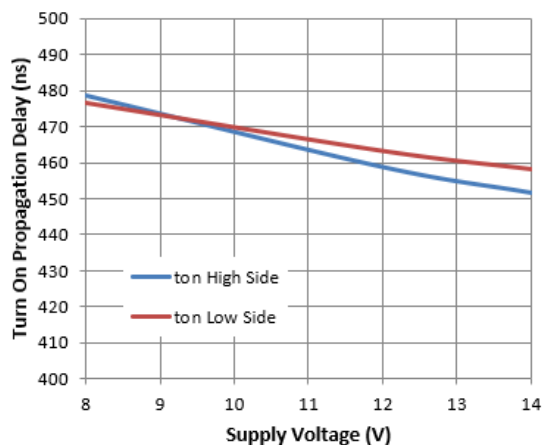


Figure 4. Turn-on Propagation Delay vs. Supply Voltage

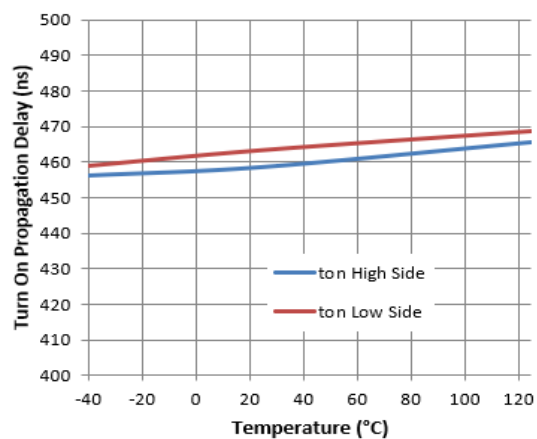


Figure 5. Turn-on Propagation Delay vs. Temperature

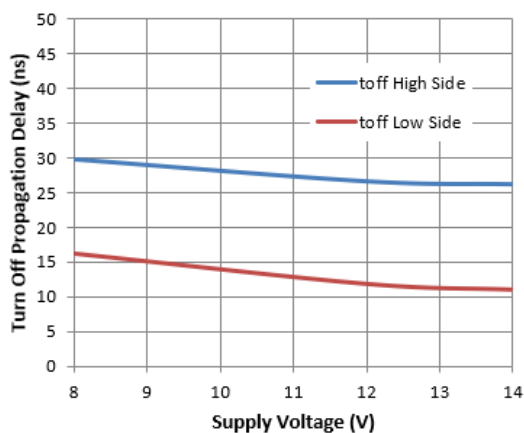


Figure 6. Turn-off Propagation Delay vs. Supply Voltage

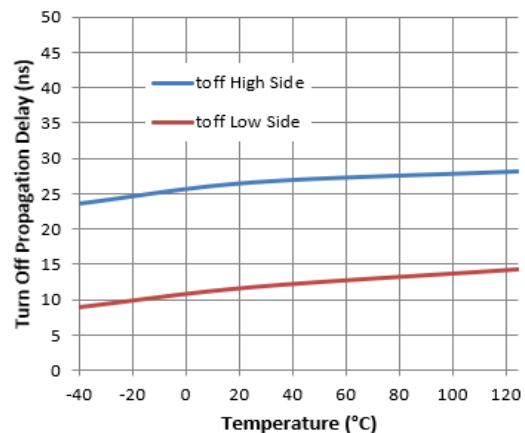


Figure 7. Turn-off Propagation Delay vs. Temperature

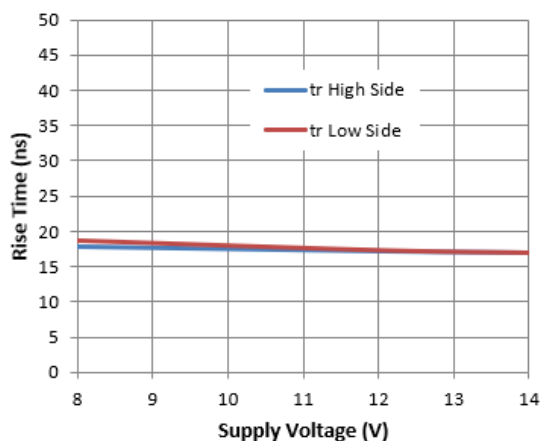


Figure 8. Rise Time vs. Supply Voltage

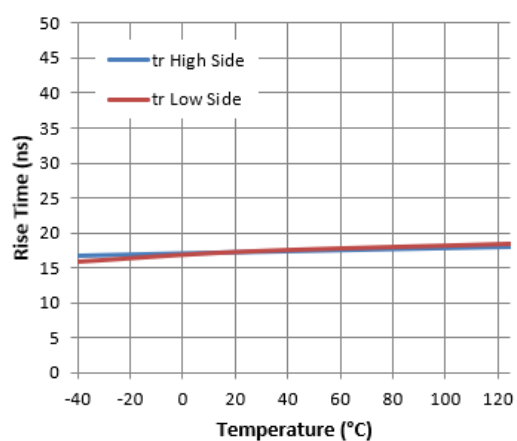


Figure 9. Rise Time vs. Temperature

Typical Performance Characteristics (Cont.)

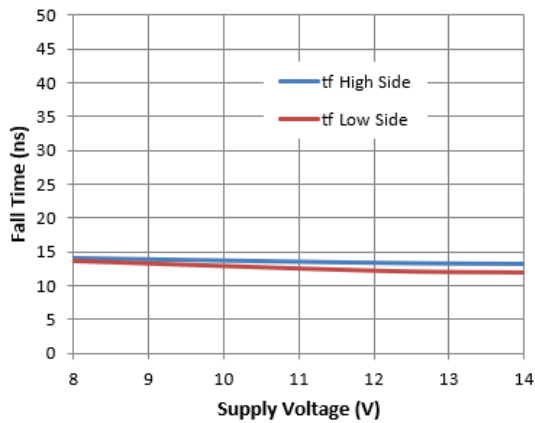


Figure 10. Fall Time vs. Supply Voltage

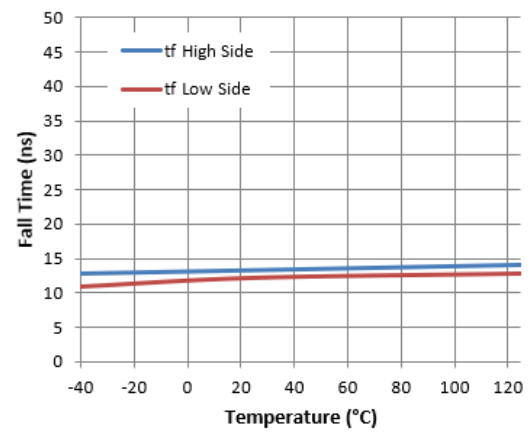


Figure 11. Fall Time vs. Temperature

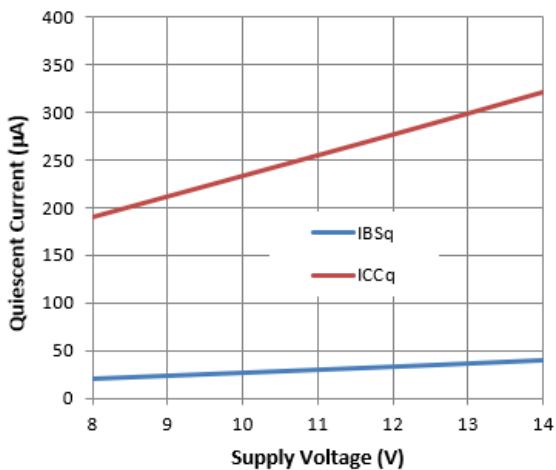


Figure 12. Quiescent Current vs. Supply Voltage

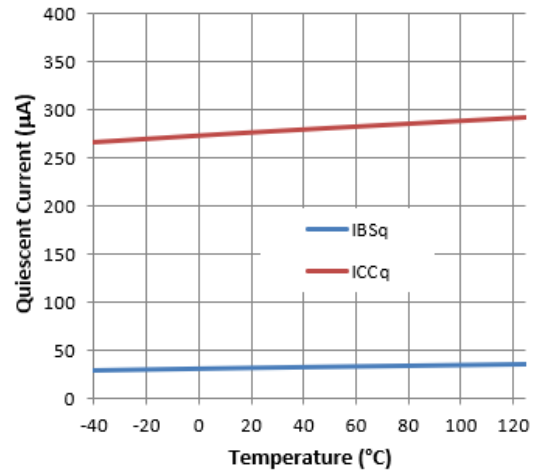


Figure 13. Quiescent Current vs. Temperature

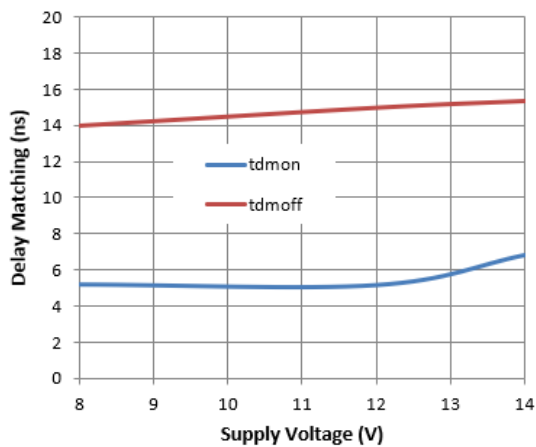


Figure 14. Delay Matching vs. Supply Voltage

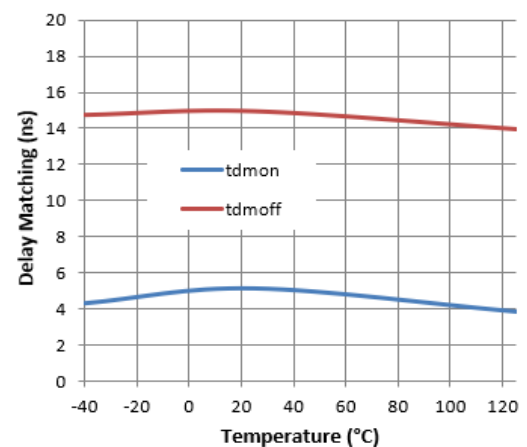


Figure 15. Delay Matching vs. Temperature

Typical Performance Characteristics (Cont.)

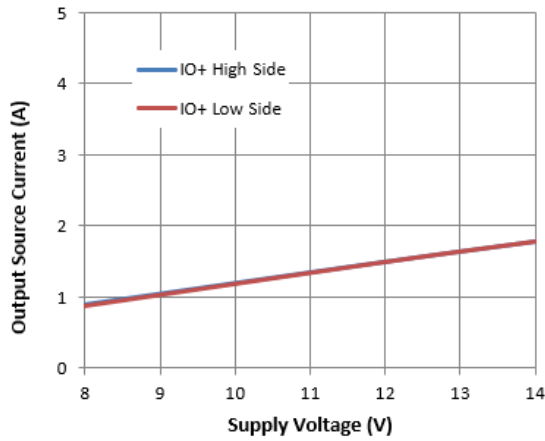


Figure 16. Output Source Current vs. Supply Voltage

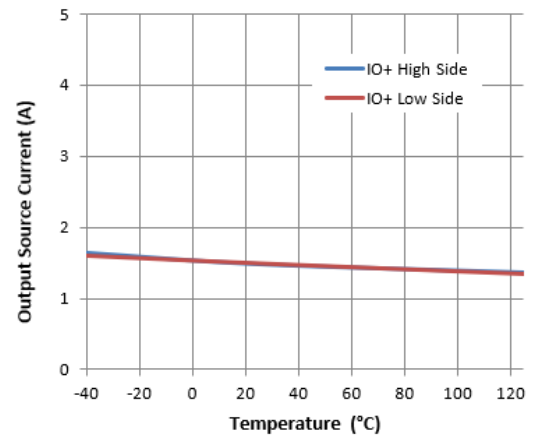


Figure 17. Output Source Current vs. Temperature

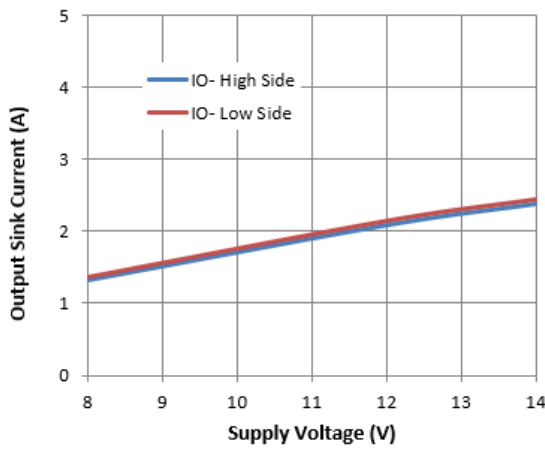


Figure 18. Output Sink Current vs. Supply Voltage

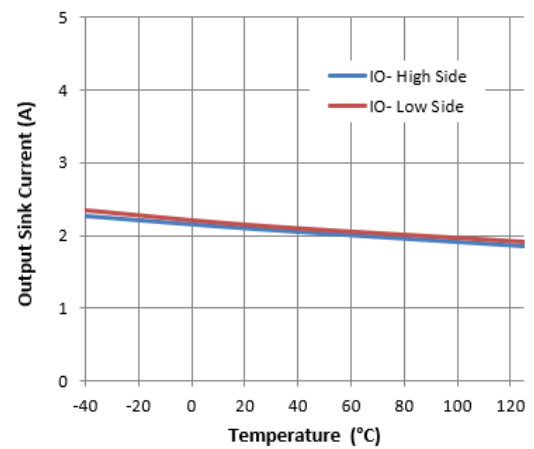


Figure 19. Output Sink Current vs. Temperature

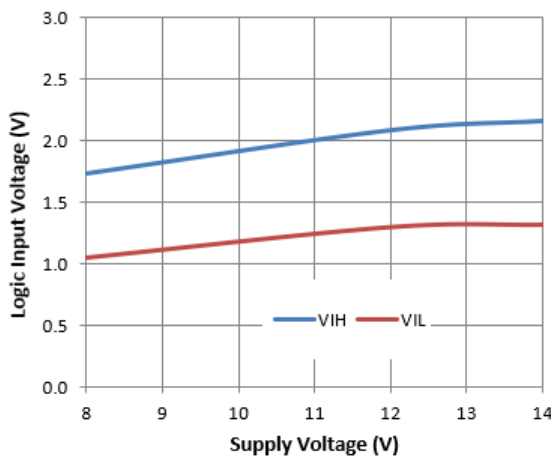


Fig 20. Logic Input Voltage vs. Supply Voltage

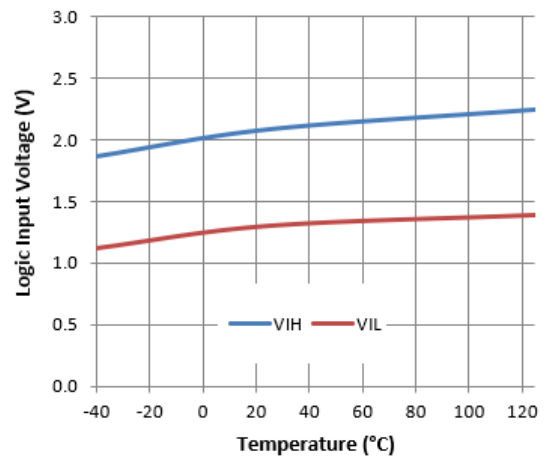


Fig 21. Logic Input Voltage vs. Temperature

Typical Performance Characteristics (Cont.)

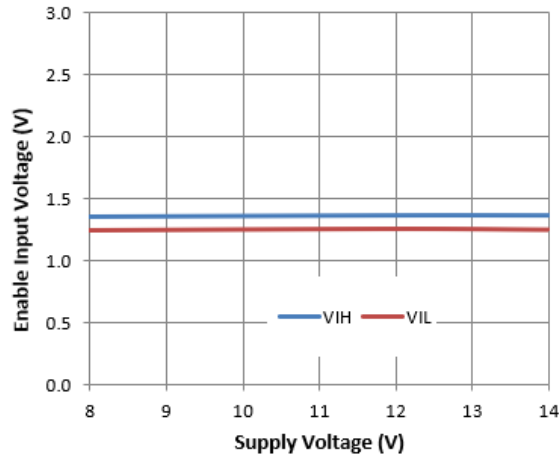


Fig 22. Enable Input Voltage vs. Supply Voltage

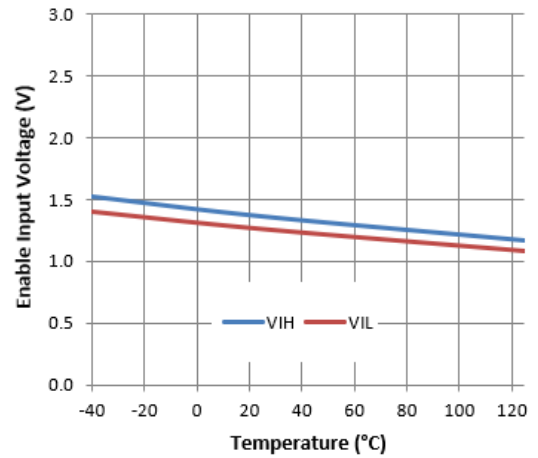


Fig 23. Enable Input Voltage vs. Temperature

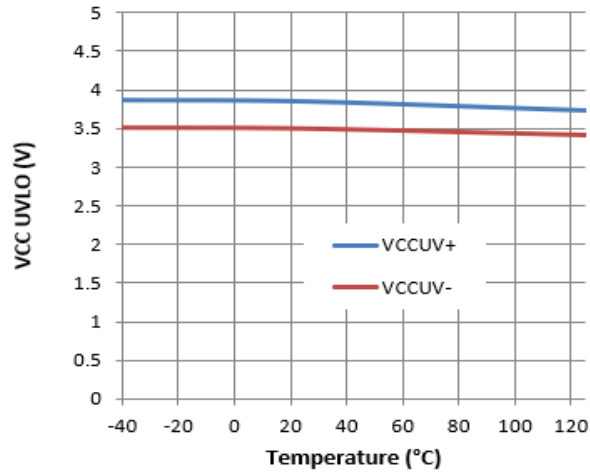


Figure 24. VCC UVLO vs. Temperature

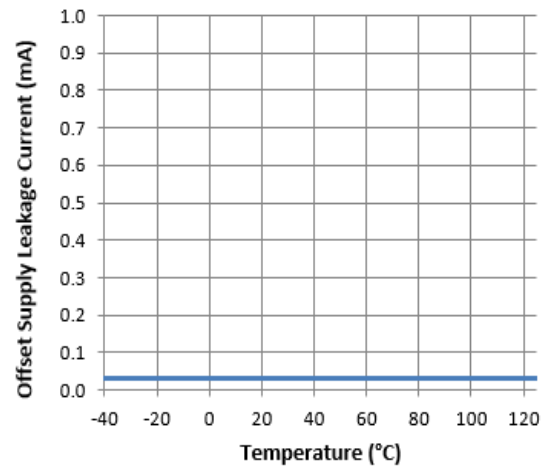
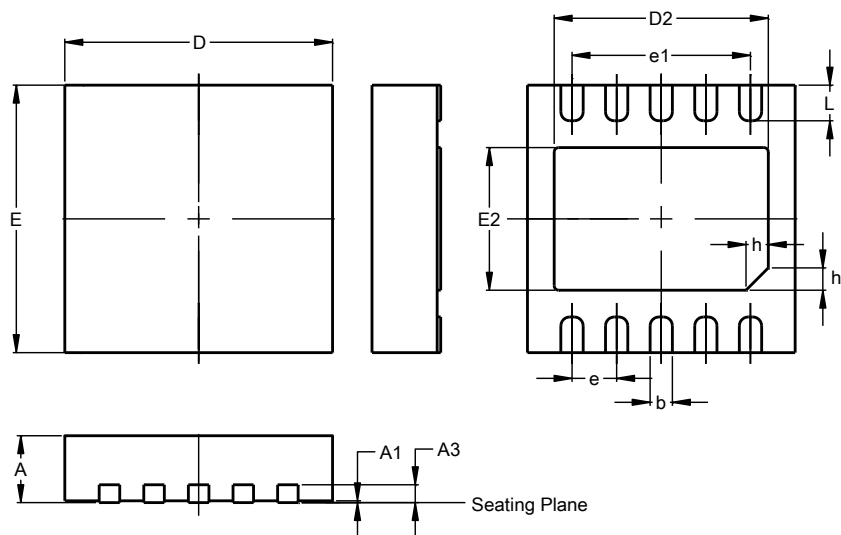


Figure 25. Offset Supply Leakage Current vs. Temperature

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-10 (Type TH)

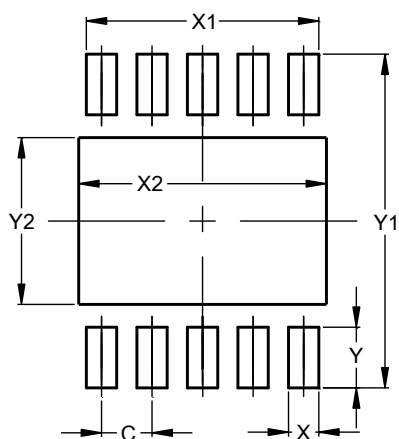


W-DFN3030-10 (Type TH)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	--	0.05	0.02
A3	0.18	0.25	0.20
b	0.18	0.30	0.25
D	2.90	3.10	3.00
D2	2.40	2.60	2.50
e	0.50BSC		
e1	2.00BSC		
E	2.90	3.10	3.00
E2	1.45	1.65	1.55
h	0.20	0.30	0.25
L	0.30	0.50	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-10 (Type TH)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	2.300
X2	2.600
Y	0.600
Y1	3.300
Y2	1.650

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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