Data Sheet April 2001 File Number 4658.3

12-Bit, 130MSPS, Dual High Speed CMOS D/A (2.7V-5.5V)

The HI5828 is a Dual 12-bit, 130MSPS (Mega Samples Per Second), high speed, low power, D/A converter which is implemented in an advanced CMOS process. Operating from a single +3V to +5V supply, the converter provides 20mA of full scale output current and includes edge-triggered CMOS input data latches. Low glitch energy and excellent frequency domain performance is achieved by the HI5828's segmented current source architecture.

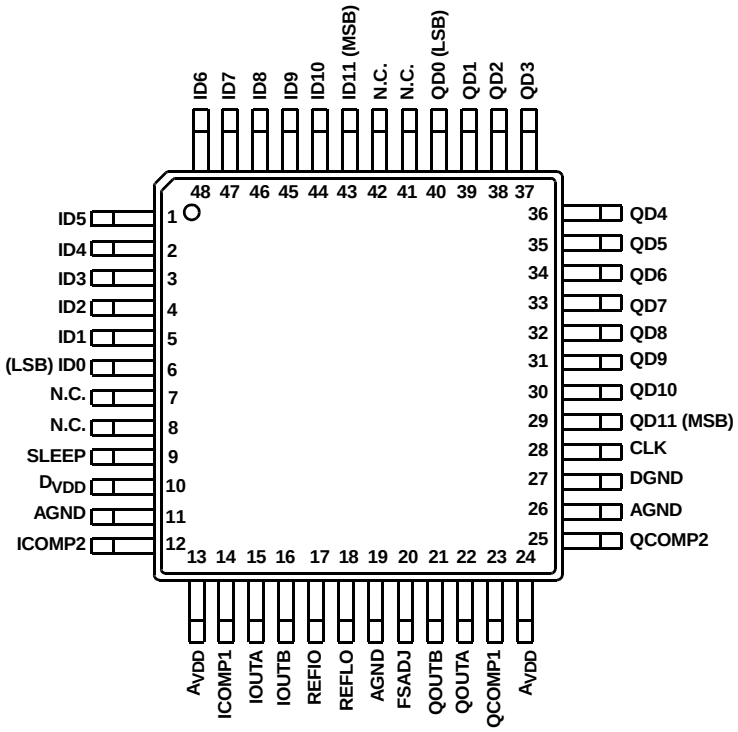
This device complements the HI5x60 and HI5x28 family of high speed converters, which includes 8, 10, 12, and 14-bit devices.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.	CLOCK SPEED
HI5828IN	-40 to 85	48 Ld LQFP	Q48.7x7A	130MSPS
HI5828EVAL2	25	Evaluation Platform		130MSPS

Pinout

HI5828
(LQFP)
TOP VIEW



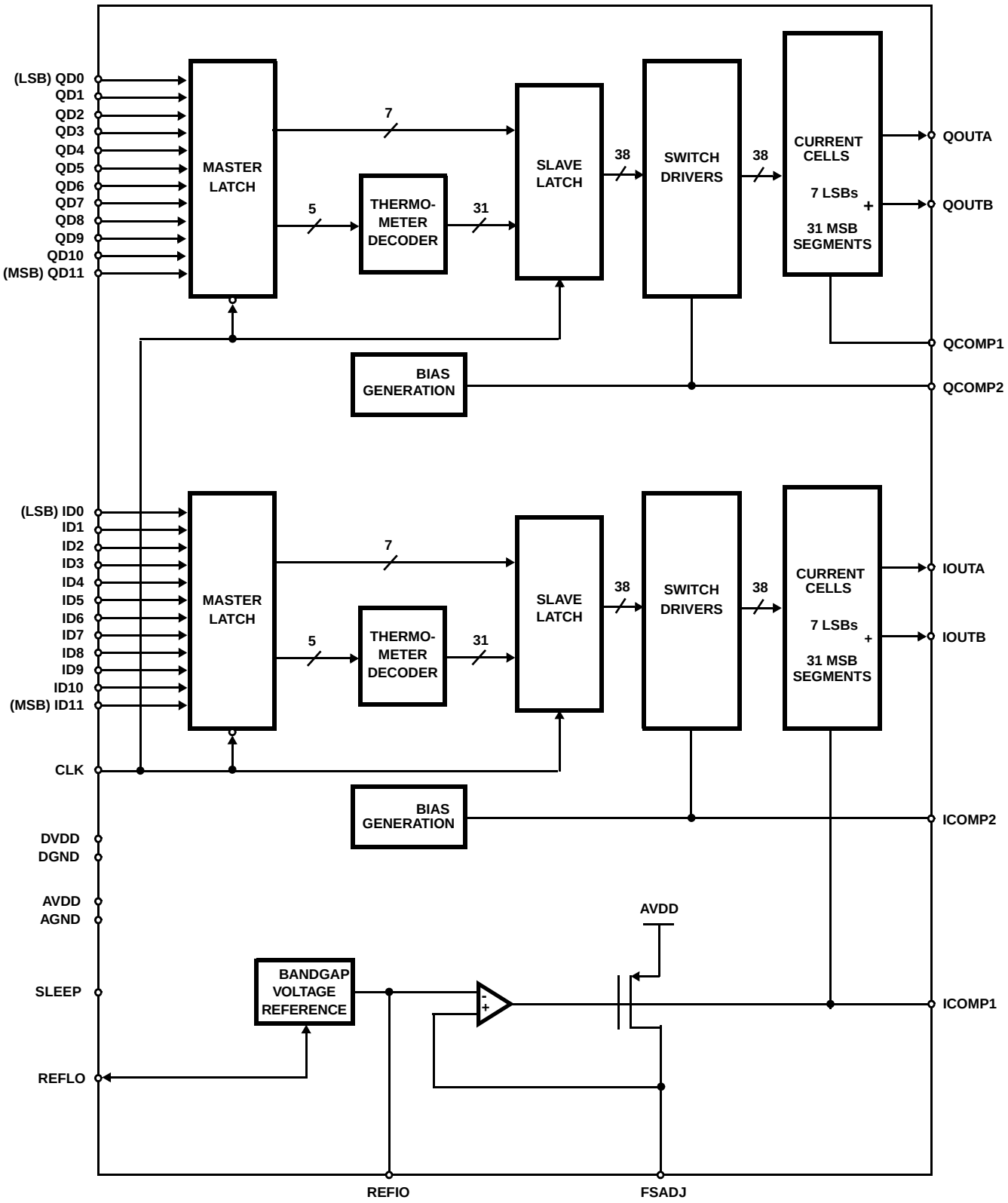
Features

- Throughput Rate 130MSPS
- Low Power . . . . .312mW at 5V, 46mW at 3V (at 60MSPS)
- Integral Linearity Error . . . . . ±0.75 LSB (Typ)
- Adjustable Full Scale Output Current . . . . . 2mA to 20mA
- Internal 1.2V Bandgap Voltage Reference
- Single or Dual Power Supply from +3V to +5V
- Power Down Mode
- CMOS Compatible Inputs
- Excellent Spurious Free Dynamic Range (76dBc, f_S = 50MSPS, f_{OUT} = 2.51MHz)
- Excellent Multitone Intermodulation Distortion

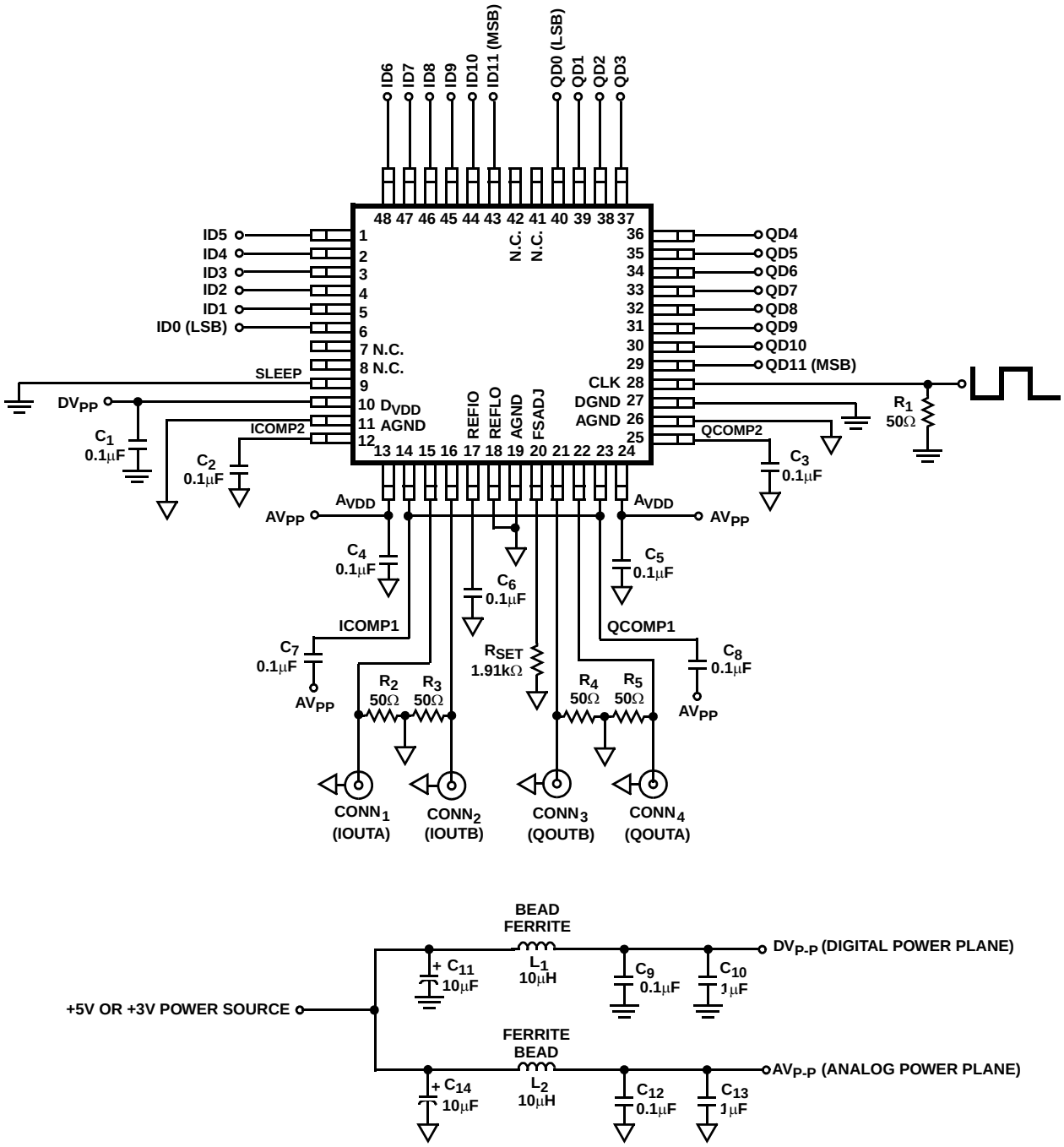
Applications

- Basestations (Cellular, WLL)
- Quadrature Modulation
- Wireless Communications Systems
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Medical/Test Instrumentation
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Functional Block Diagram



Typical Applications Circuit



NOTE: Separate analog and digital grounds should be used, in which case the grounds should be tied together at a single point near the device. The analog and digital grounds should be connected together by a thin single trace and never connected together by an inductor.

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
11, 19, 26	AGND	Analog Ground.
13, 24	A_{VDD}	Analog Supply (+2.7V to +5.5V).
28	CLK	Clock Input. The master and slave latches shown in the functional block diagram are simple D-latches. Input data to the DAC passes through the “master” latches when the clock is low and is latched into the “master” latches when the clock is high. Data presented to the “slave” latch passes through when the clock is logic high and is latched into the “slave” latches when the clock is logic low. Adequate setup time must be allowed for the MSBs to pass through the thermometer decoder before the clock goes high. This master-slave arrangement comprises an edge-triggered flip-flop, with the DAC being updated on the rising clock edge. It is recommended that the clock edge be skewed such that setup time is larger than hold time for optimum spectral performance.
27	DGND	Connect to Digital Ground.
10	D_{VDD}	Digital Supply (+2.7V to +5.5V).
20	FSADJ	Full Scale Current Adjust. Use a resistor to analog ground to adjust full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}. Where V_{FSADJ} is the voltage at this pin. V_{FSADJ} tracks the voltage on the REFIO pin (refer to the functional block diagram); which is typically 1.2V if the internal reference is used.
14, 23	ICOMP1, QCOMP1	Compensation Pin for Use in Reducing Bandwidth/Noise. Each pin should be individually decoupled to AVDD with a 0.1µF capacitor. To minimize crosstalk, the part was designed so that these pins **must** be connected externally, ideally directly under the device packaging. The voltage on these pins is used to drive the gates of the PMOS devices that make up the current cells. Only the ICOMP1 pin is driven and therefore QCOMP1 needs to be connected to ICOMP1, but de-coupled separately to minimize crosstalk. If placed equally close to both pins, then only one decoupling capacitor might be necessary.
12, 25	ICOMP2, QCOMP2	Compensation Pin for Internal Bias Generation. Each pin should be individually decoupled to AGND with a 0.1µF capacitor. The voltage generated at these pins represents the voltage used to supply power to the switch drivers (refer to the functional block diagram) which is 2.0V nominal. This arrangement helps to minimize clock feedthrough to the current cell transistors for reduced glitch energy and improved spectral performance.
43-48, 1-6, 29-40	ID11-ID0, QD11-QD0	Digital Data Input Ports. Bit 11 is Most Significant Bit (MSB) and bit 0 is the Least Significant Bit (LSB).
15, 22	IOUTA, QOUTA	Current Outputs of the Device. Full scale output current is achieved when all input bits are set to binary 1.
16, 21	IOUTB, QOUTB	Complementary Current Outputs of the Device. Full scale output current is achieved on the complementary outputs when all input bits are set to binary 0.
7, 8, 41, 42	N.C.	No Connection. Future LSBs for dual 14-bit DAC.
17	REFIO	Reference voltage input if Internal reference is disabled. The internal reference is not intended to drive an external load. Use 0.1µF cap to ground when internal reference is enabled.
18	REFLO	Reference Low Select. When the internal reference is enabled, this pin serves as the precision ground reference point for the internal voltage reference circuitry and therefore needs to have a good connection to analog ground to enable internal 1.2V reference. To disable the internal reference circuitry this pin should be connected to A_{VDD}.
9	SLEEP	Control Pin for Power-Down Mode. Sleep Mode is active high; connect to ground for Normal Mode. The Sleep pin has internal 25µA (nominal) active pulldown current.

Absolute Maximum Ratings

Digital Supply Voltage D_{VDD} to DGND . . . . . +5.5V
Analog Supply Voltage A_{VDD} to AGND . . . . . +5.5V
Grounds, AGND TO DGND . . . . . -0.3V to +0.3V
Digital Input Voltages (D11-D0, CLK, SLEEP) . . . . . D_{VDD} + 0.3V
Reference Input Voltage Range . . . . . A_{VDD} + 0.3V
Analog Output Current (IOUTA/B, QOUTA/B) 24mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA}(^{O}C/W)
LQFP Package 70
Maximum Junction Temperature . . . . . 150^{O}C
Maximum Storage Temperature Range . . . . . -65^{O}C to 150^{O}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{O}C
(LQFP - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^{O}C to 85^{O}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

A_{VDD} = D_{VDD} = +5V (except where otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = 25^{O}C for All Typical Values

PARAMETER	TEST CONDITIONS	T_A = -40^{O}C TO 85^{O}C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	"Best Fit" Straight Line (Note 8)	-2.0	±0.75	+2.0	LSB
Differential Linearity Error, DNL	(Note 8)	-1.0	±0.5	+1.0	LSB
Offset Error, I_{OS}	(Note 8)	-0.025	-	+0.025	% FSR
Offset Drift Coefficient	(Note 8)	-	0.1	-	ppm FSR/^{O}C
Full Scale Gain Error, FSE	With External Reference (Notes 2, 8)	-10	±2	+10	% FSR
	With Internal Reference (Notes 2, 8)	-10	±1	+10	% FSR
Full Scale Gain Drift	With External Reference (Note 8)	-	±50	-	ppm FSR/^{O}C
	With Internal Reference (Note 8)	-	±100	-	ppm FSR/^{O}C
Full Scale Output Current, I_{FS}		2	-	20	mA
Crosstalk	f_{CLK} = 100MSPS, f_{OUT} = 10MHz	-	85	-	dB
	f_{CLK} = 100MSPS, f_{OUT} = 40MHz	-	64	-	dB
Gain Matching Between Channels (DC Measurement)	As a percentage of Full Scale Range	-5	-	+5	% FSR
	In dB Full Scale Range	-0.445	-	+0.420	dB FSR
Output Voltage Compliance Range	(Note 3, 8)	-0.3	-	1.25	V
DYNAMIC CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}	(Note 3)	130	-	-	MHz
Output Settling Time, (t_{SETT})	±0.05% (±2 LSB) (Note 8)	-	35	-	ns
Singlet Glitch Area (Peak Glitch)	R_L = 25Ω (Note 8)	-	5	-	pV•s
Output Rise Time	Full Scale Step	-	2.5	-	ns
Output Fall Time	Full Scale Step	-	2.5	-	ns
Output Capacitance		-	10	-	pF

Electrical Specifications $A_{VDD} = D_{VDD} = +5V$ (except where otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	$T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
Output Noise	IOUTFS = 20mA	-	50	-	pA/$\sqrt{Hz}$
	IOUTFS = 2mA	-	30	-	pA/$\sqrt{Hz}$
AC CHARACTERISTICS					
+5V Power Supply Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 100MSPS, f_{OUT} = 20.2MHz, 30MHz Span (Notes 4, 8)	-	77	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz, 8MHz Span (Notes 4, 8)	-	93	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, 8MHz Span (Notes 4, 8)	-	93	-	dBc
+5V Power Supply Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 100MSPS, f_{OUT} = 4.0MHz (Notes 4, 8)	-	-72	-	dB
	f_{CLK} = 50MSPS, f_{OUT} = 2.0MHz (Notes 4, 8)	-	-74	-	dB
	f_{CLK} = 25MSPS, f_{OUT} = 1.0MHz (Notes 4, 8)	-	-73	-	dB
+5V Power Supply Spurious Free Dynamic Range, SFDR to Nyquist ($f_{CLK}/2$)	f_{CLK} = 130MSPS, f_{OUT} = 40.4MHz (Notes 4, 8)	-	55	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 10.1MHz (Notes 4, 8)	-	66	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 5.02MHz, T = 25^oC (Notes 4, 8)	66	72	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 5.02MHz, T = Min to Max (Notes 4, 8)	66	-	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 40.4MHz (Notes 4, 8)	-	54	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 20.2MHz (Notes 4, 8)	-	62	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz, T = 25^oC (Notes 4, 8)	66	72	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz, T = Min to Max (Notes 4, 8)	66	-	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 2.51MHz (Notes 4, 8)	-	75	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz (Notes 4, 8)	-	64	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, T = 25^oC (Notes 4, 8)	66	72	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, T = Min to Max (Notes 4, 8)	66	-	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 2.51MHz (Notes 4, 8)	-	76	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz (Notes 4, 8)	-	78	-	dBc
	f_{CLK} = 25MSPS, f_{OUT} = 1.0MHz (Notes 4, 8)	-	77	-	dBc
+5V Power Supply Multitone Power Ratio	f_{CLK} = 20MSPS, f_{OUT} = 2.0MHz to 2.99MHz, 8 Tones at 110kHz Spacing (Notes 4, 8)	-	76	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 10MHz to 14.95MHz, 8 Tones at 530kHz Spacing (Notes 4, 8)	-	76	-	dBc
+3V Power Supply Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 100MSPS, f_{OUT} = 20.2MHz, 30MHz Span (Notes 4, 8)	-	73	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz, 8MHz Span (Notes 4, 8)	-	91	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, 8MHz Span (Notes 4, 8)	-	91	-	dBc
+3V Power Supply Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 100MSPS, f_{OUT} = 4.0MHz (Notes 4, 8)	-	-71	-	dB
	f_{CLK} = 50MSPS, f_{OUT} = 2.0MHz (Notes 4, 8)	-	-75	-	dB
	f_{CLK} = 25MSPS, f_{OUT} = 1.0MHz (Notes 4, 8)	-	-74	-	dB

Electrical Specifications $A_{VDD} = D_{VDD} = +5V$ (except where otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	$T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
+3V Power Supply Spurious Free Dynamic Range, SFDR to Nyquist ($f_{CLK}/2$)	f_{CLK} = 130MSPS, f_{OUT} = 40.4MHz (Notes 4, 8)	-	47	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 10.1MHz (Notes 4, 8)	-	66	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 5.02MHz (Notes 4, 8)	-	73	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 40.4MHz (Notes 4, 8)	-	48	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 20.2MHz (Notes 4, 8)	-	58	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz (Notes 4, 8)	-	72	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 2.51MHz (Notes 4, 8)	-	76	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz (Notes 4, 8)	-	53	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, T = 25^oC (Notes 4, 8)	68	73	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, T = Min to Max (Notes 4, 8)	66	-	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 2.51MHz (Notes 4, 8)	-	76	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz(Notes 4, 8)	-	76	-	dBc
	f_{CLK} = 25MSPS, f_{OUT} = 1.0MHz (Notes 4, 8)	-	76	-	dBc
+3V Power Supply Multitone Power Ratio	f_{CLK} = 20MSPS, f_{OUT} = 2.0MHz to 2.99MHz, 8 Tones at 110kHz Spacing (Notes 4, 8)	-	76	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 10MHz to 14.95MHz, 8 Tones at 530kHz Spacing (Notes 4, 8)	-	76	-	dBc
VOLTAGE REFERENCE					
Internal Reference Voltage, V_{FSADJ}	Pin 18 Voltage with Internal Reference	1.15	1.22	1.29	V
Internal Reference Voltage Drift		-	±10	-	ppm/^oC
Internal Reference Output Current Sink/Source Capability		-	±100	-	nA
Reference Input Impedance		-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Note 8)	-	1.4	-	MHz
DIGITAL INPUTS D11-D0, CLK					
Input Logic High Voltage with 5V Supply, V_{IH}	(Note 3)	3.5	5	-	V
Input Logic High Voltage with 3V Supply, V_{IH}	(Note 3)	2.1	3	-	V
Input Logic Low Voltage with 5V Supply, V_{IL}	(Note 3)	-	0	1.3	V
Input Logic Low Voltage with 3V Supply, V_{IL}	(Note 3)	-	0	0.9	V
Input Sleep Current, I_{IH}		-25	-	+25	µA
Input Logic Current, I_{IH}		-10	-	+10	µA
Input Logic Current, I_{IL}		-10	-	+10	µA
Digital Input Capacitance, C_{IN}		-	5	-	pF

Electrical Specifications $A_{VDD} = D_{VDD} = +5V$ (except where otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	$T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 4 (Note 3)	-	1.5	-	ns
Data Hold Time, t_{HLD}	See Figure 4 (Note 3)	-	1.2	-	ns
Propagation Delay Time, t_{PD}	See Figure 4	-	2.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 4 (Note 3)	4	-	-	ns
POWER SUPPLY CHARACTERISTICS					
AV_{DD} Power Supply	(Note 9)	2.7	5.0	5.5	V
DV_{DD} Power Supply	(Note 9)	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})	5V or 3V, IOUTFS = 20mA (Note 7)	-	44	50	mA
	5V or 3V, IOUTFS = 2mA	-	7	-	mA
Digital Supply Current (I_{DVDD})	5V (Note 5)	-	12	-	mA
	5V (Note 6)	-	17.6	-	mA
	5V (Note 7)	-	29	38	mA
	3V (Note 5)	-	4	-	mA
	3V (Note 6)	-	8.2	-	mA
	3V (Note 7)	-	9.6	12	mA
Supply Current (I_{AVDD}) Sleep Mode	5V or 3V, IOUTFS = Don't Care	-	2.7	-	mA
Power Dissipation	5V, IOUTFS = 20mA (Note 5)	-	280	-	mW
	5V, IOUTFS = 20mA (Note 6)	-	312	-	mW
	5V, IOUTFS = 20mA (Note 7)	-	365	440	mW
	5V, IOUTFS = 2mA (Note 6)	-	137	-	mW
	3V, IOUTFS = 20mA (Note 5)	-	144	-	mW
	3V, IOUTFS = 20mA (Note 6)	-	158		mW
	3V, IOUTFS = 20mA (Note 7)	-	161	177	mW
	3V, IOUTFS = 2mA (Note 6)	-	46	-	mW
Power Supply Rejection	Single Supply (Note 8)	-0.2	-	+0.2	% FSR/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. Spectral measurements made with differential transformer coupled output and no external filtering.
5. Measured with the clock at 60MSPS and the output frequency at 10MHz.
6. Measured with the clock at 100MSPS and the output frequency at 40MHz.
7. Measured with the clock at 130MSPS and the output frequency at 5MHz.
8. See "Definition of Specifications".
9. It is recommended that the output current be reduced to 12mA or less to maintain optimum performance for operation below 3V. DV_{DD} and AV_{DD} do not have to be equal.

Definition of Specifications

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Full Scale Gain Drift, is measured by setting the data inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per ^{O}C.

Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R_{SET}).

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Internal Reference Voltage Drift, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm per ^{O}C.

Offset Drift, is measured by setting the data inputs to all logic low (all 0's) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per degree ^{O}C.

Offset Error, is measured by setting the data inputs to all logic low (all 0's) and measuring the output voltage through a known resistance. Offset error is defined as the maximum *deviation* of the output current from a value of 0mA.

Output Settling Time, is the time required for the output voltage to settle to within a specified error band measured from the beginning of the output transition. The measurement is done by switching quarter scale. Termination impedance was 25Ω due to the parallel resistance of the 50Ω loading on the output and the oscilloscope's 50Ω input. This also aids the ability to resolve the specified error band without overdriving the oscilloscope.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed does not violate the compliance range.

Power Supply Rejection, is measured using a single power supply. The supply's nominal +5V is varied ±10% and the change in the DAC full scale output is noted.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1's. The frequency is increased until the amplitude of the output waveform is 0.707 (-3dB) of its original value.

Singlet Glitch Area, is the switching transient appearing on the output during a code transition. It is measured as the area under the overshoot portion of the curve and is expressed as a Volt-Time specification. This is tested using a single code transition across a major current source.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

Total Harmonic Distortion, THD, is the ratio of the RMS value of the fundamental output signal to the RMS sum of the first five harmonic components.

Detailed Description

The HI5828 is a dual 12-bit, current out, CMOS, digital to analog converter. Its maximum update rate is 130MSPS and can be powered by either single or dual power supplies in the recommended range of +3V to +5V. Operation with clock rates higher than 130MSPS is possible; please contact the factory for more information. It consumes 370mW of power when using a +5V supply with the data switching at 130MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter might have a substantially larger amount of current turning on and off at certain, worst-case transition points such as midscale and quarter scale transitions. By greatly reducing the amount of current switching at certain 'major' transitions, the overall glitch of the converter is dramatically reduced, improving settling time, transient problems, and accuracy.

Digital Inputs and Termination

The HI5828 digital inputs are guaranteed to CMOS levels. However, TTL compatibility can be achieved by lowering the supply voltage to 3V due to the digital threshold of the input buffer being approximately half of the supply voltage. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are long 50Ω lines, then 50Ω termination resistors should be placed as close to the converter inputs as possible connected to the digital ground plane (if separate grounds are used). These termination resistors are not likely needed as long as the digital waveform source is within a few inches of the DAC.

Ground Planes

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane. Consult Application Note AN9855.

Noise Reduction

To minimize power supply noise, 0.1µF capacitors should be placed as close as possible to the converter's power supply pins, A_{VDD} and D_{VDD}. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for DV_{DD} and to the analog ground for A_{VDD}. Additional filtering of the power supplies on the board is recommended.

Voltage Reference

The internal voltage reference of the device has a nominal value of + 1.2V with a ±10ppm/°C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1µF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (18) selects the reference. The internal reference can be selected if pin 18 is tied low (ground). If an external reference is desired, then pin 18 should be tied high (the analog supply voltage) and the external reference driven into REFIO, pin 17. The full scale output current of the converter is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range, though operation below 2mA is possible, with performance degradation.

V_{FSADJ} and V_{REFIO} will be equivalent except for a small offset voltage. If the internal reference is used, V_{FSADJ} will equal approximately 1.2V on the FSADJ pin (20). If an external reference is used, V_{FSADJ} will equal the external reference. The calculation for I_{OUT}(Full Scale) is:

$$I_{OUT}(\text{Full Scale}) = (V_{FSADJ}/R_{SET}) \text{ X } 32.$$

If the full scale output current is set to 20mA by using the internal voltage reference (1.2V) and a 1.91kΩ R_{SET} resistor, then the input coding to output current will resemble the following:

TABLE 1. INPUT CODING vs OUTPUT CURRENT

INPUT CODE (D11-D0)	I/QOUTA (mA)	I/QOUTB (mA)
11 11111 11111	20	0
10 00000 00000	10	10
00 00000 00000	0	20

Outputs

The 5 MSBs for each DAC on the HI5828 drive a thermometer decoder**,** which is a digital decoder that has an N-bit (5 bits for the HI5828) binary coded input word with 2^N-1 (31 for the HI5828) output bits, where the number of output bits that are active correlate directly to the input binary word. The HI5828 uses a thermometer decoder to significantly minimize the output glitch energy for each DAC. I/QOUTA and I/QOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -0.3V to 1.25V. R_{LOAD} (the impedance loading each current output) should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$$V_{OUT} = I_{OUT} \text{ X } R_{LOAD}.$$

These outputs can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. The SFDR measurements in this data sheet were performed with a 1:1 transformer on the output of the DAC (see Figure 1). With the center tap grounded, the output swing of pins 15/22 and 16/21 will be biased at zero volts. The loading as shown in Figure 1 will result in a 500mV signal at the output of the transformer if the full scale output current of the DAC is set to 20mA. $V_{OUT} = 2 \text{ x } I_{OUT} \text{ x } R_{EQ}$, where R_{EQ} is ~12.5Ω.

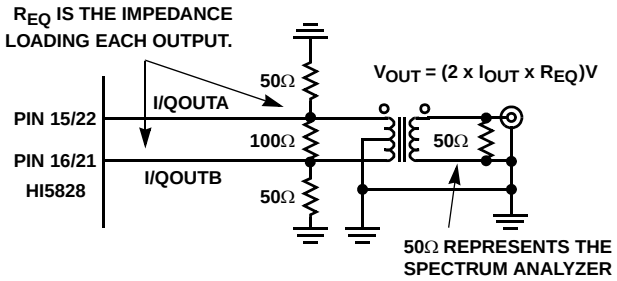


FIGURE 1.

Allowing the center tap to float will result in identical transformer output, however the output pins of the DAC will have positive DC offset. Since the DAC's output voltage compliance range is -0.3V to +1.25V, the center tap may need to be left floating or DC offset in order to increase the amount of signal swing available. The 50Ω load on the output of the transformer represents the spectrum analyzer's input impedance.

Timing Diagrams

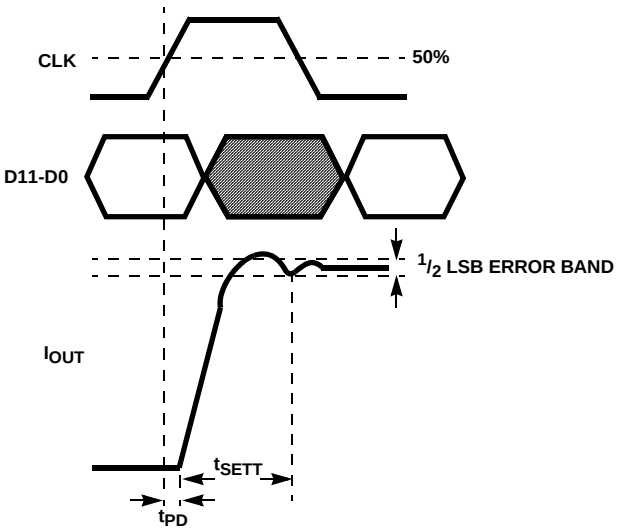


FIGURE 2. OUTPUT SETTLING TIME DIAGRAM

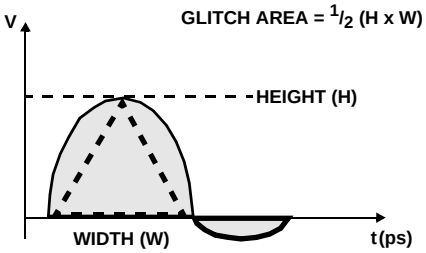


FIGURE 3. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

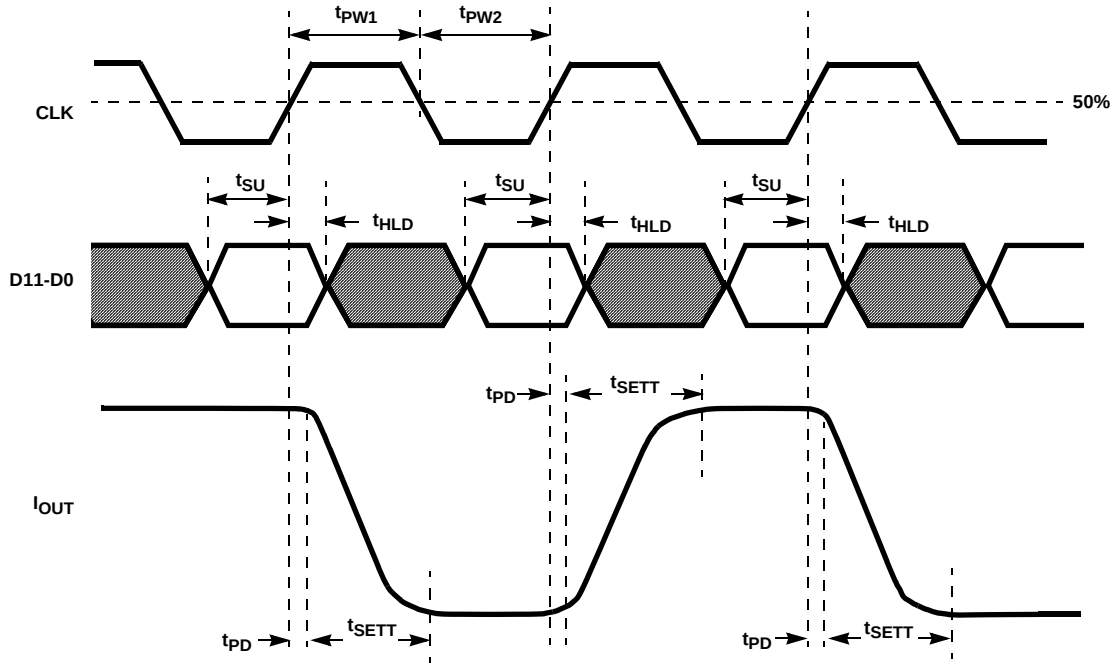
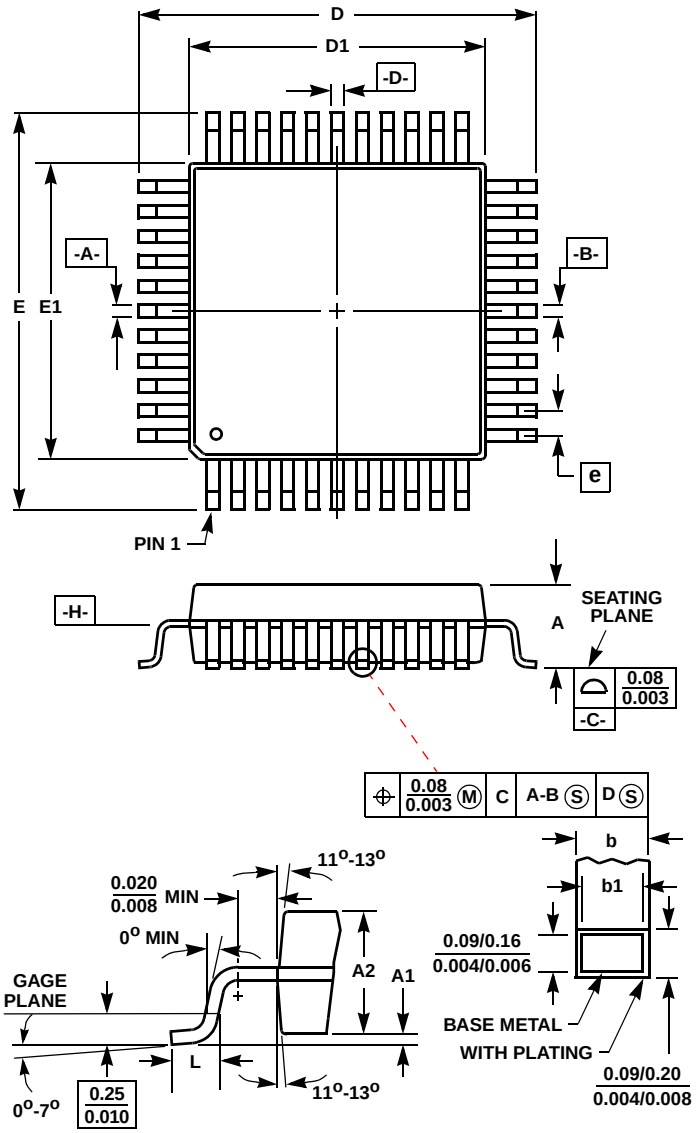


FIGURE 4. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Thin Plastic Quad Flatpack Packages (LQFP)



Q48.7x7A (JEDEC MS-026BBC ISSUE B)
48 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.350	0.358	8.90	9.10	3
D1	0.272	0.280	6.90	7.10	4, 5
E	0.350	0.358	8.90	9.10	3
E1	0.272	0.280	6.90	7.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	48		48		7
e	0.020 BSC		0.50 BSC		-

Rev. 2 1/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

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