

# CMOS Strobed Hex Inverter/Buffer

High-Voltage Types (20-Volt Rating)

■ CD4502B consists of six inverter/buffers with 3-state outputs. A logic "1" on the OUTPUT DISABLE input produces a high-impedance state in all six outputs. This feature permits common bussing of the outputs, thus simplifying system design. A Logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B"-series I<sub>OL</sub> standard.

The CD4502B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

## MAXIMUM RATINGS, Absolute-Maximum Values:

### DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)

Voltages referenced to V<sub>SS</sub> Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub> +0.5V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA

### POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C

STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C

### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

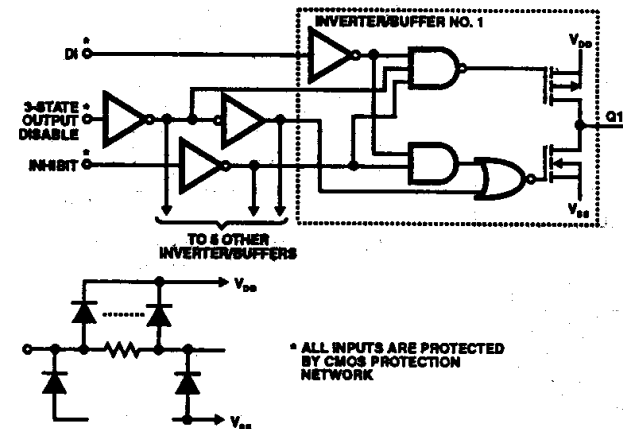
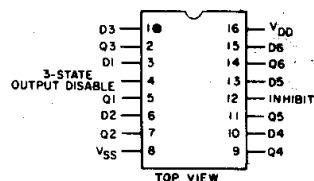


Fig.1 – Logic diagram of 1 of 6 identical inverter/buffers.



TERMINAL ASSIGNMENT

## Features:

- 2 TTL-load output drive capability
- 3-state outputs
- Common output-disable control
- Inhibit control
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Noise margin (full package-temperature range) =

1 V at V<sub>DD</sub> = 5 V  
2 V at V<sub>DD</sub> = 10 V  
2.5 V at V<sub>DD</sub> = 15 V

## Applications:

- 3-state hex inverter for interfacing IC's with data buses
- COS/MOS to TTL hex buffer

# CD4502B Types

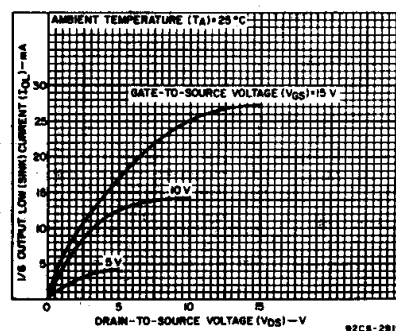
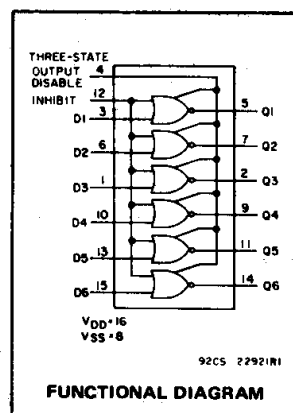


Fig.2 – Typical output low (sink) current characteristics.

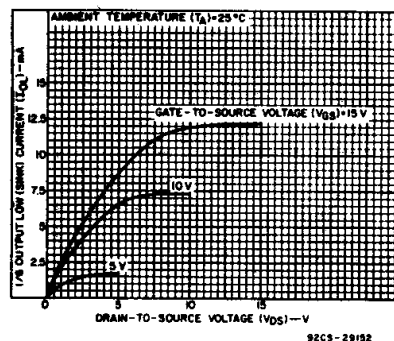


Fig.3 – Minimum output low (sink) current characteristics.

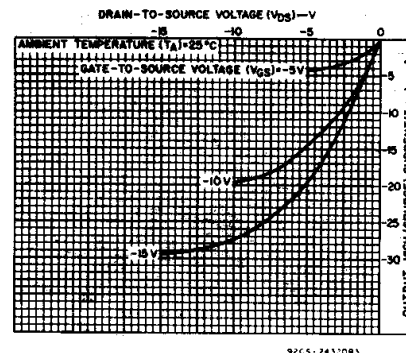


Fig.4 – Typical output high (source) current characteristics.

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## CD4502B Types

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC                                                    | LIMITS |      | UNITS |
|-------------------------------------------------------------------|--------|------|-------|
|                                                                   | Min.   | Max. |       |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | 3      | 18   | V     |

### STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC                                         | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|-------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) |                                       |       |       |       | +25   |                   |      |       |
|                                                             |                       |                        |                        | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |       |
| Quiescent Device<br>Current,<br>I <sub>DD</sub> Max.        | —                     | 0,5                    | 5                      | 1                                     | 1     | 30    | 30    | —     | 0.02              | 1    | μA    |
|                                                             | —                     | 0,10                   | 10                     | 2                                     | 2     | 60    | 60    | —     | 0.02              | 2    |       |
|                                                             | —                     | 0,15                   | 15                     | 4                                     | 4     | 120   | 120   | —     | 0.02              | 4    |       |
|                                                             | —                     | 0,20                   | 20                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0,5                    | 5                      | 3.84                                  | 3.66  | 2.52  | 2.16  | 3.06  | 6                 | —    | mA    |
|                                                             | 0.5                   | 0,10                   | 10                     | 9.6                                   | 9     | 6.6   | 5.4   | 7.8   | 15.6              | —    |       |
|                                                             | 1.5                   | 0,15                   | 15                     | 25.2                                  | 24    | 16.8  | 14.4  | 20.4  | 40.8              | —    |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 4.6                   | 0,5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |
|                                                             | 2.5                   | 0,5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|                                                             | 9.5                   | 0,10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|                                                             | 13.5                  | 0,15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
| Output Voltage:<br>Low-Level,<br>V <sub>OL</sub> Max.       | —                     | 0,5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|                                                             | —                     | 0,10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|                                                             | —                     | 0,15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output Voltage:<br>High-Level,<br>V <sub>OH</sub> Min.      | —                     | 0,5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|                                                             | —                     | 0,10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|                                                             | —                     | 0,15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low<br>Voltage,<br>V <sub>IL</sub> Max.               | 0.5, 4.5              | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|                                                             | 1, 9                  | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|                                                             | 15, 13.5              | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High<br>Voltage,<br>V <sub>IH</sub> Min.              | 4.5                   | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|                                                             | 9                     | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|                                                             | 13.5                  | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                       |                       | 0,18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |
| 3-State Output<br>Leakage Current<br>I <sub>OUT</sub> Max.  | 0,18                  | 0,18                   | 18                     | ±0.4                                  | ±0.4  | ±12   | ±12   | —     | ±10 <sup>-4</sup> | ±0.4 | μA    |

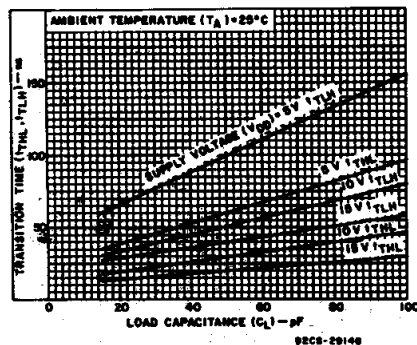


Fig. 8 - Typical transition time as a function of load capacitance.

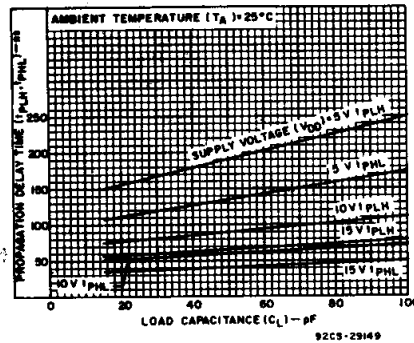


Fig. 9 - Typical propagation delay time as a function of load capacitance.

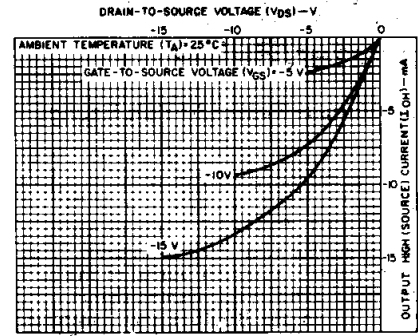


Fig. 5 - Minimum output high (source) current characteristics.

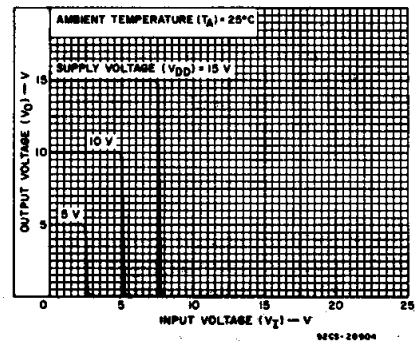


Fig. 6 - Typical voltage transfer characteristics.

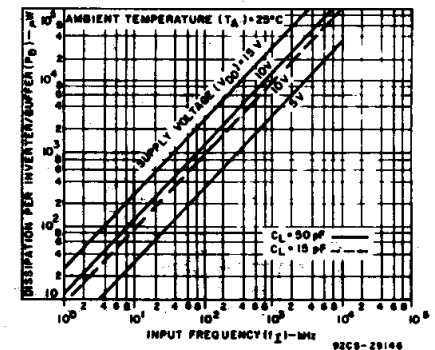


Fig. 7 - Typical power dissipation as a function of input frequency.

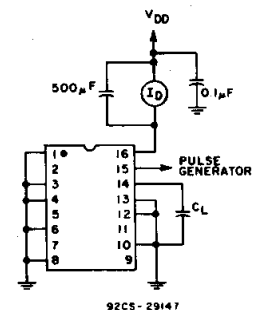


Fig. 10 - Power-dissipation test circuit.

## CD4502B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20 \text{ ns}$ ,  
 $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ K}\Omega$  Unless otherwise specified.

| CHARACTERISTIC                                                                                  | TEST CONDITIONS | LIMITS     |     |     | UNITS |    |
|-------------------------------------------------------------------------------------------------|-----------------|------------|-----|-----|-------|----|
|                                                                                                 |                 | VDD<br>(V) | TYP | MAX |       |    |
| Data or Inhibit Delay Times:<br>High to Low, t <sub>PHL</sub>                                   |                 | 5          | 135 | 270 | ns    |    |
|                                                                                                 |                 | 10         | 60  | 120 |       |    |
|                                                                                                 |                 | 15         | 40  | 80  |       |    |
| Low to High, t <sub>PLH</sub>                                                                   |                 | 5          | 190 | 380 |       |    |
|                                                                                                 |                 | 10         | 90  | 180 |       |    |
|                                                                                                 |                 | 15         | 65  | 130 |       |    |
| Disable Delay Times: R <sub>L</sub> =1 KΩ<br>Output High to High<br>Impedance, t <sub>PHZ</sub> | See Fig. 14     | 5          | 60  | 120 | ns    |    |
|                                                                                                 |                 | 10         | 40  | 80  |       |    |
|                                                                                                 |                 | 15         | 30  | 60  |       |    |
| High-Impedance to Output<br>High, t <sub>PZH</sub>                                              |                 | 5          | 110 | 220 |       |    |
|                                                                                                 |                 | 10         | 50  | 100 |       |    |
|                                                                                                 |                 | 15         | 40  | 80  |       |    |
| Output Low to High<br>Impedance, t <sub>PLZ</sub>                                               |                 | 5          | 125 | 250 |       |    |
|                                                                                                 |                 | 10         | 65  | 130 |       |    |
|                                                                                                 |                 | 15         | 55  | 110 |       |    |
| High Impedance to Output<br>Low, t <sub>PZL</sub>                                               |                 | 5          | 125 | 250 |       |    |
|                                                                                                 |                 | 10         | 55  | 110 |       |    |
|                                                                                                 |                 | 15         | 40  | 80  |       |    |
| Transition Times:<br>Low to High, t <sub>TLH</sub>                                              |                 |            | 5   | 100 | 200   | ns |
|                                                                                                 |                 |            | 10  | 50  | 100   |    |
|                                                                                                 |                 |            | 15  | 40  | 80    |    |
| High to Low, t <sub>THL</sub>                                                                   |                 | 5          | 60  | 120 |       |    |
|                                                                                                 |                 | 10         | 30  | 60  |       |    |
|                                                                                                 |                 | 15         | 20  | 40  |       |    |
| Input Capacitance, C <sub>IN</sub>                                                              | Any Input       | 5          | 7.5 | pF  |       |    |
| Output Capacitance, C <sub>OUT</sub>                                                            |                 | 7-8        | 15  | pF  |       |    |

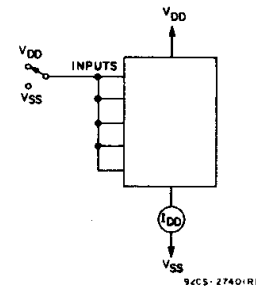


Fig. 11 - Quiescent-device-current test circuit.

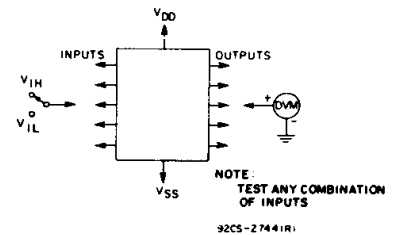


Fig. 12 - Input-voltage test circuit.

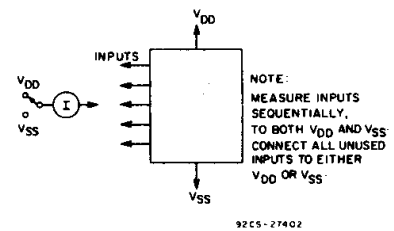


Fig. 13 - Input leakage current test circuit.

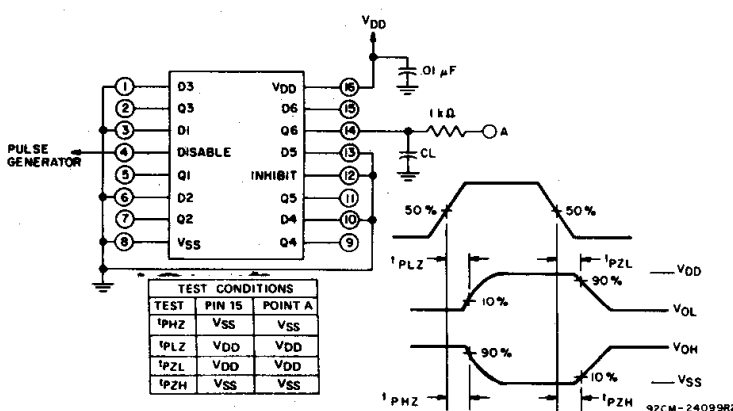
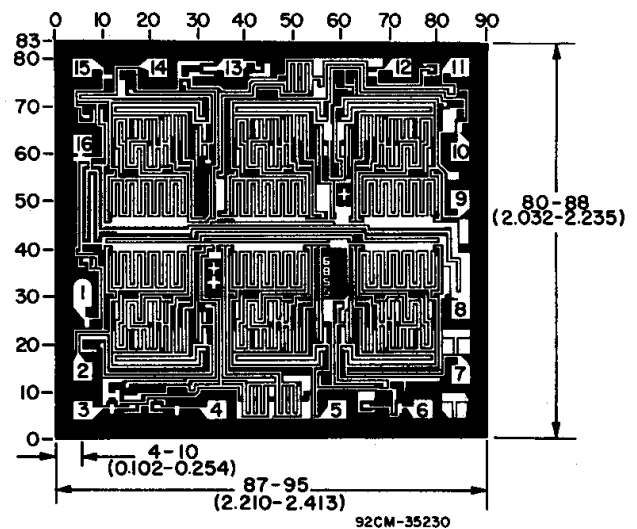


Fig. 14 - Disable delay times test circuit and waveforms.



Dimensions and Pad Layout for CD4502BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 7702002EA        | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 7702002EA<br>CD4502BF3A | <a href="#">Samples</a> |
| CD4502BE         | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD4502BE                | <a href="#">Samples</a> |
| CD4502BEE4       | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD4502BE                | <a href="#">Samples</a> |
| CD4502BF3A       | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 7702002EA<br>CD4502BF3A | <a href="#">Samples</a> |
| CD4502BM         | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4502BM                | <a href="#">Samples</a> |
| CD4502BM96       | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4502BM                | <a href="#">Samples</a> |
| CD4502BME4       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4502BM                | <a href="#">Samples</a> |
| CD4502BNSR       | ACTIVE        | SO           | NS                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4502B                 | <a href="#">Samples</a> |
| CD4502BPW        | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CM502B                  | <a href="#">Samples</a> |
| CD4502BPWR       | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CM502B                  | <a href="#">Samples</a> |
| JM38510/17403BEA | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | JM38510/<br>17403BEA    | <a href="#">Samples</a> |
| M38510/17403BEA  | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | JM38510/<br>17403BEA    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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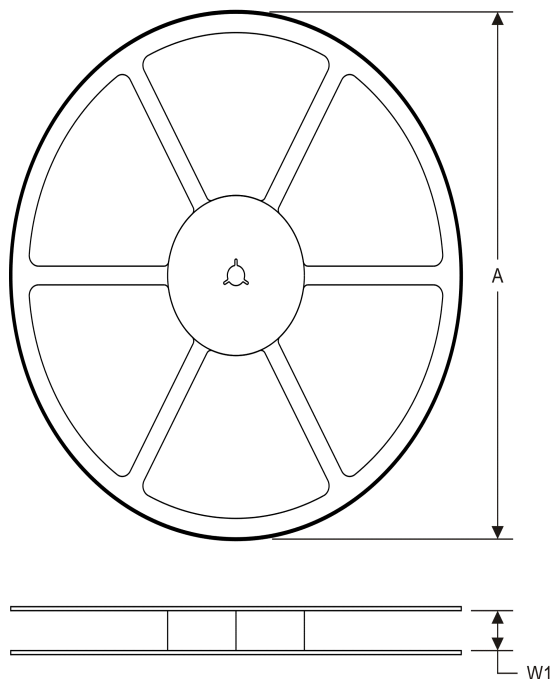
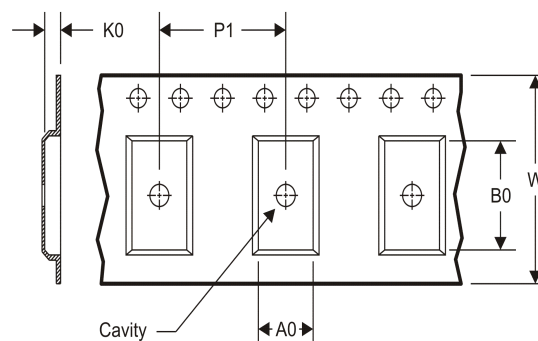
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**OTHER QUALIFIED VERSIONS OF CD4502B, CD4502B-MIL :**

- Catalog: [CD4502B](#)
- Military: [CD4502B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


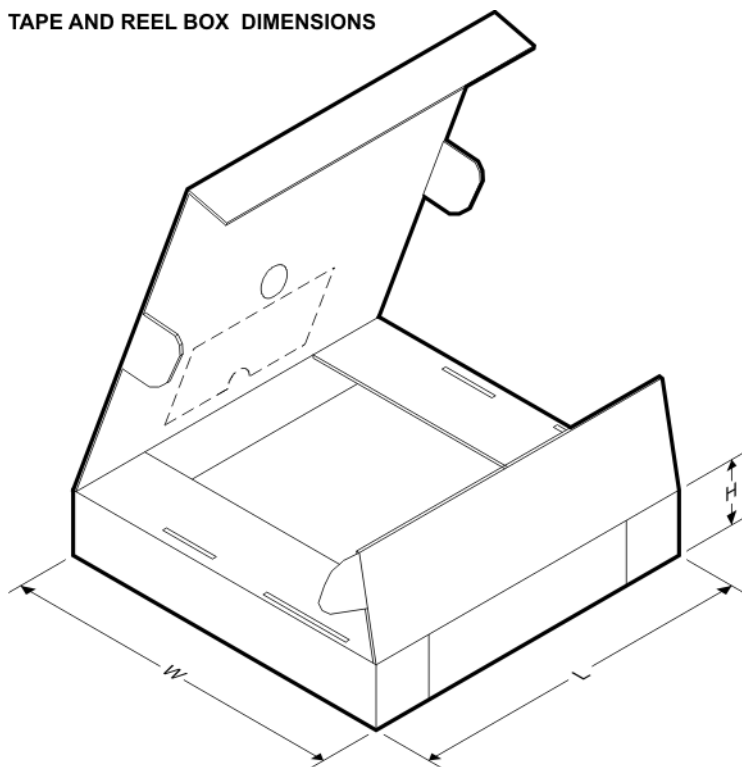
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4502BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4502BNSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4502BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



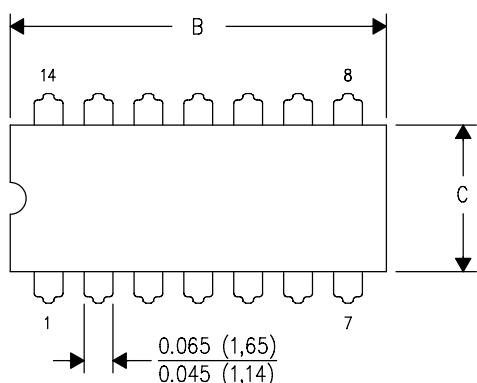
\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4502BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4502BNSR | SO           | NS              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| CD4502BPWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |

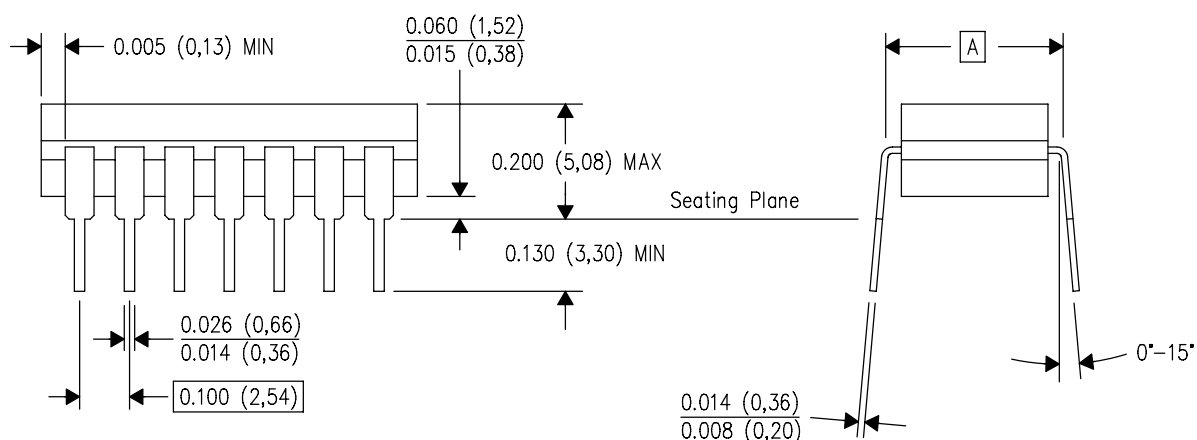
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

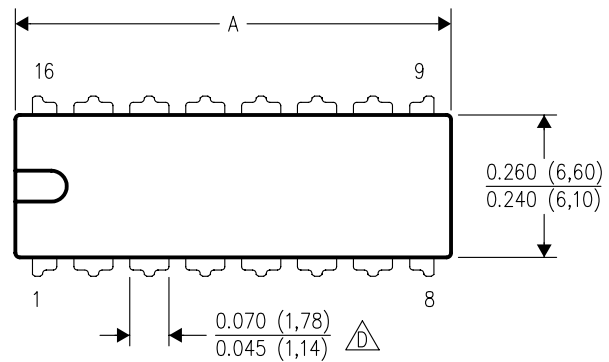
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



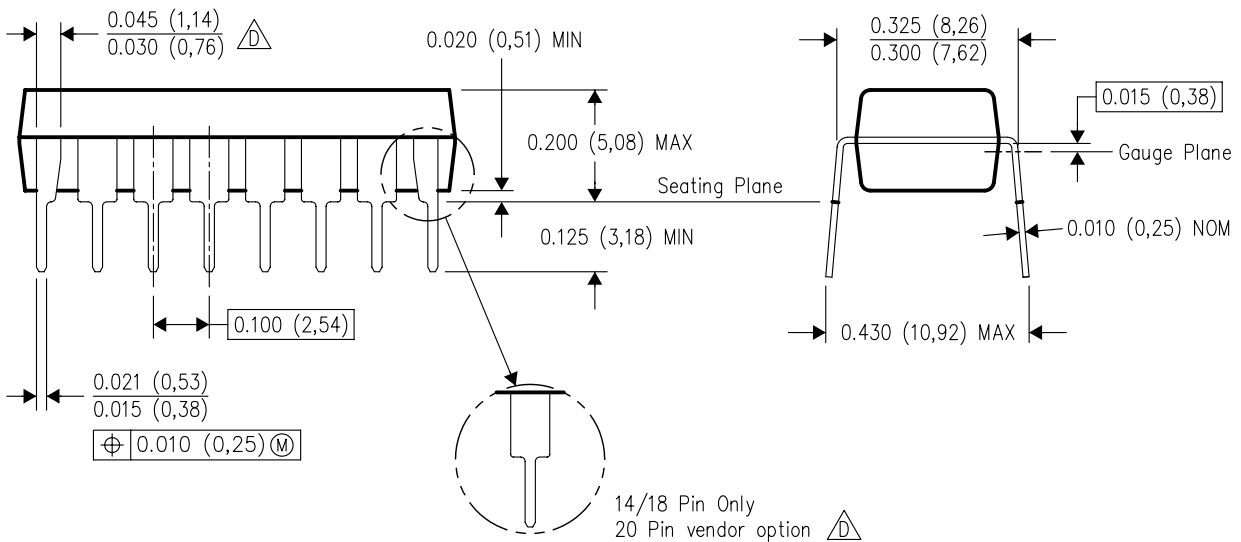
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



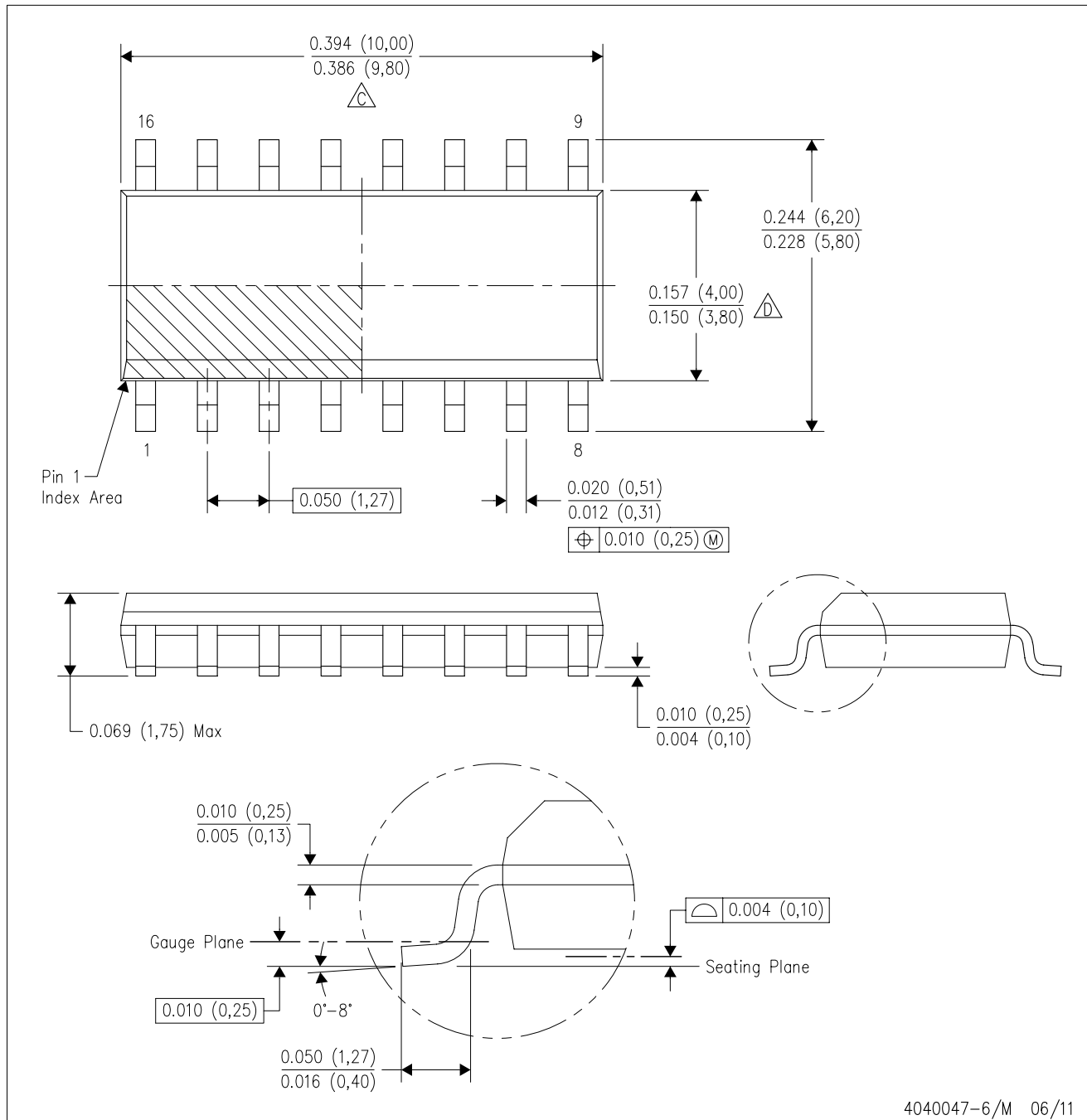
14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

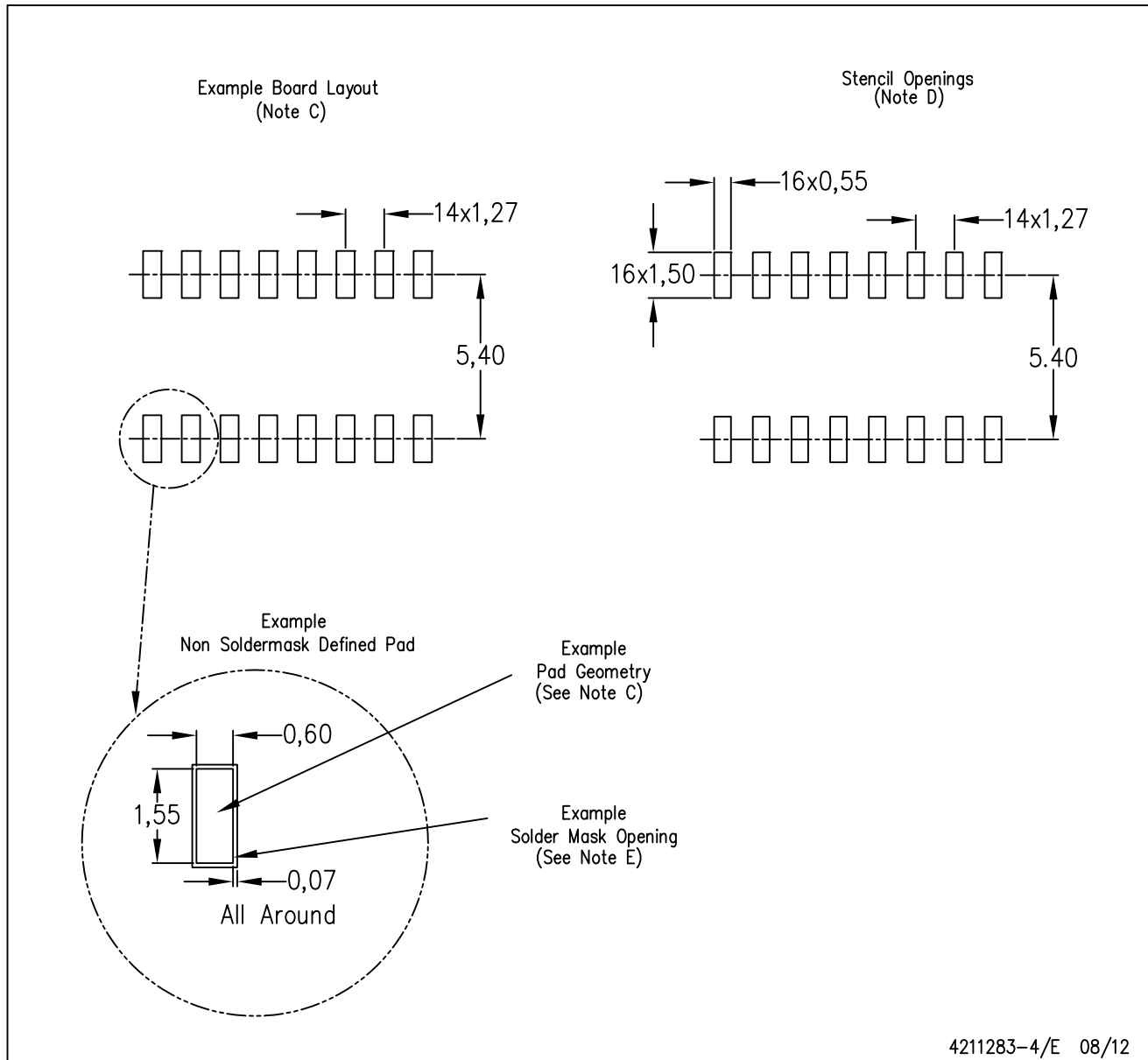
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

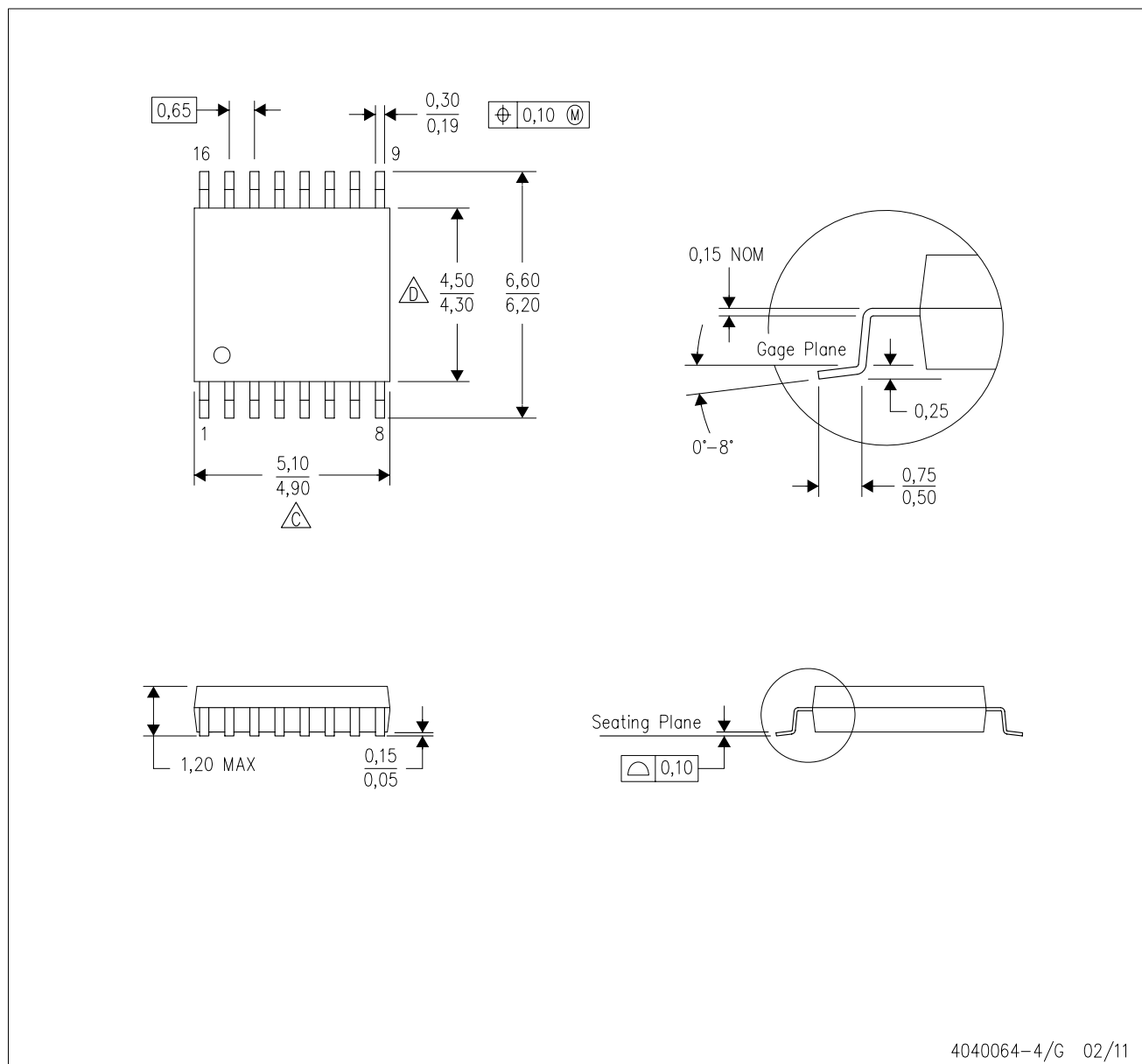
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

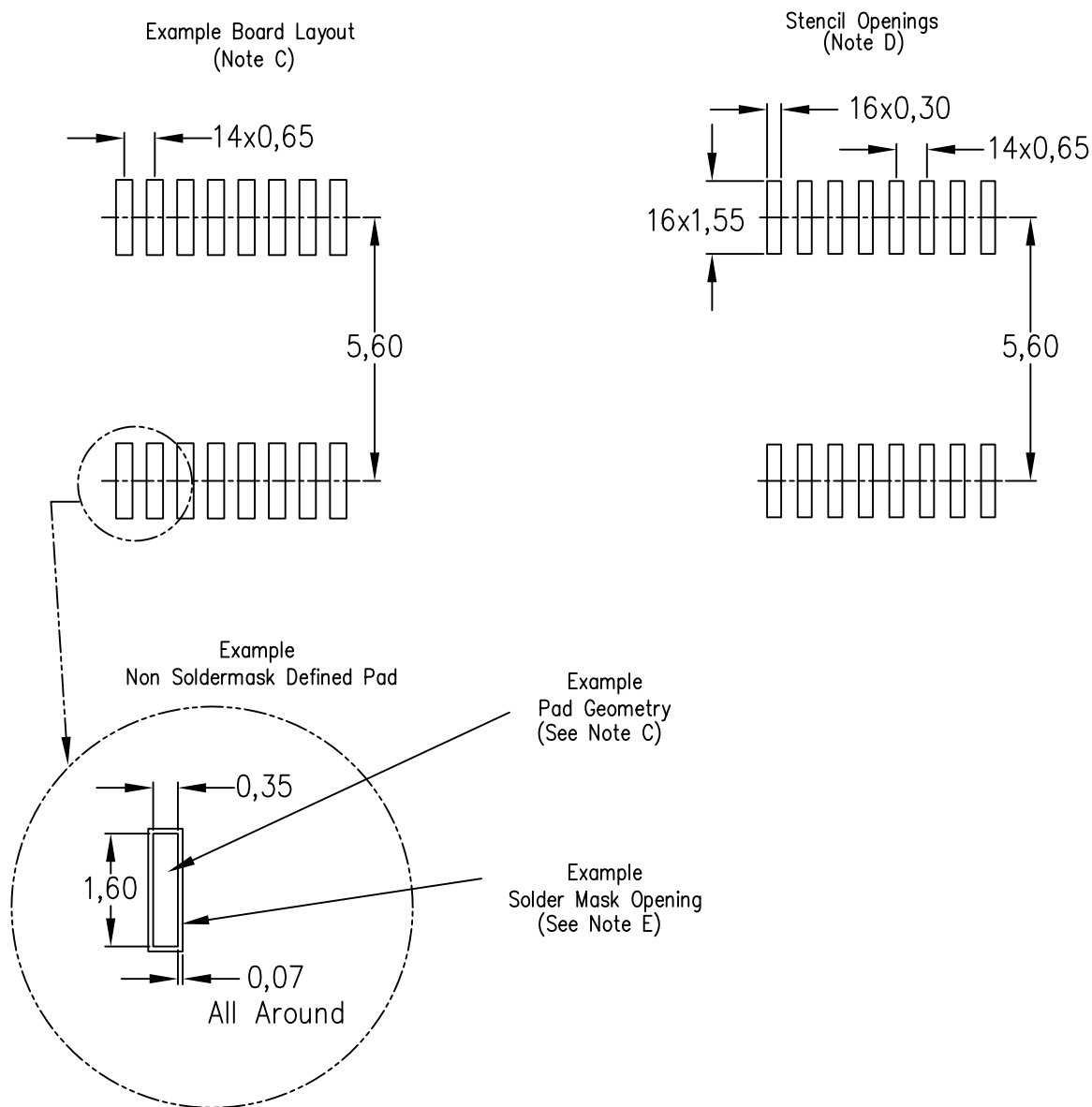
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - $\Delta$  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - $\Delta$  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

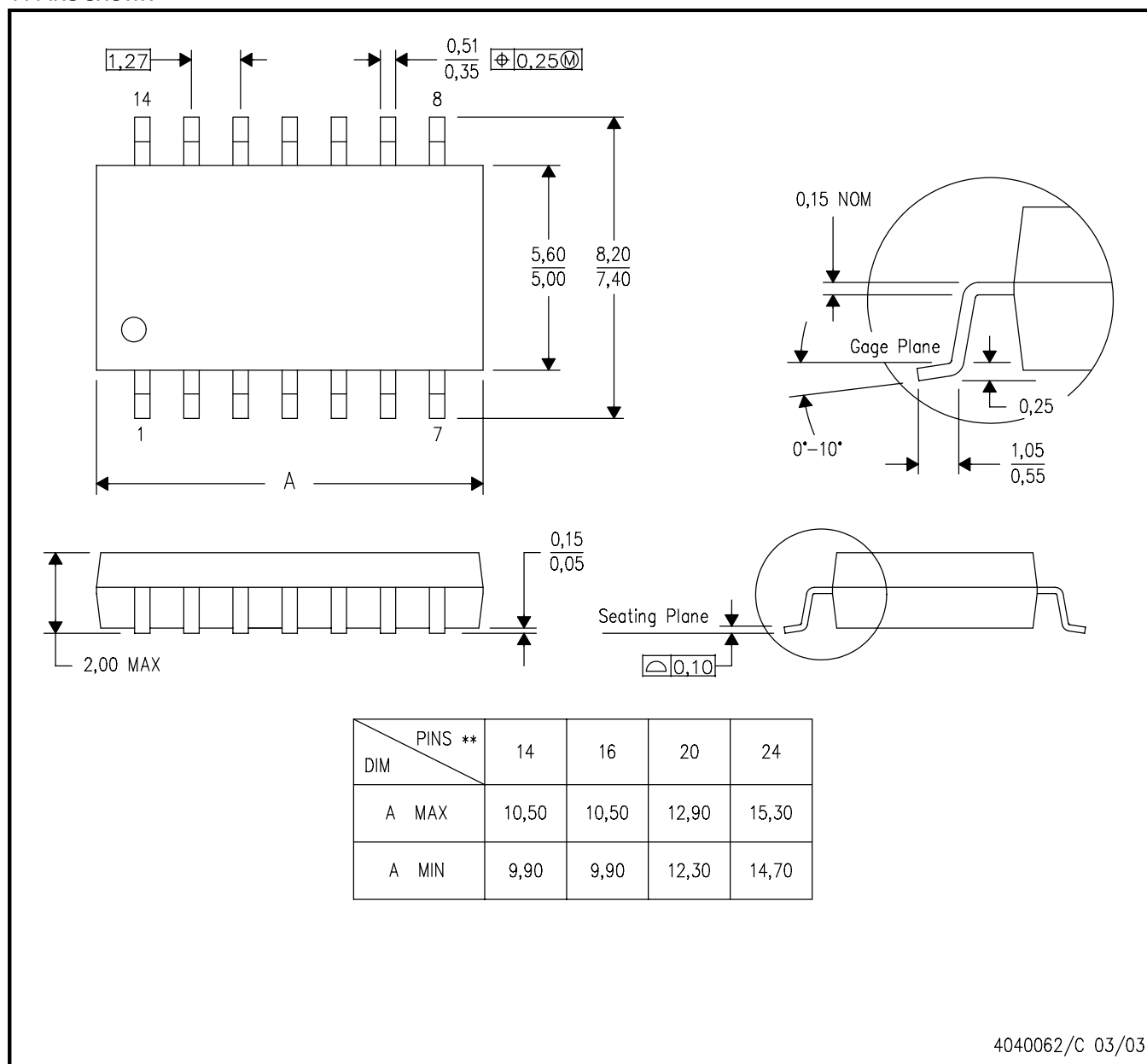
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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|                               |                                                                                          |
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| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
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| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
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