File Number **2169**

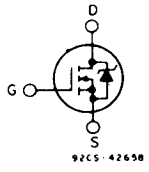
IRF644, IRF645, IRF646, IRF647

Avalanche Energy Rated N-Channel Power MOSFETs

N-CHANNEL ENHANCEMENT MODE

14A, and 13A, 275V, 250V
r_{DS} (on) = 0.28Ω, 0.34Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275V, 250V DC rated - 120V AC line system operation*



TERMINAL DIAGRAM

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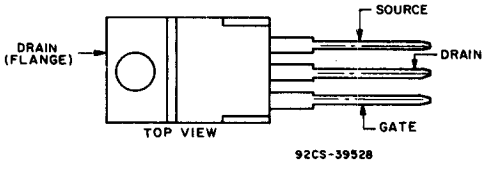
The IRF644, IRF645, IRF646, and IRF647 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

All types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

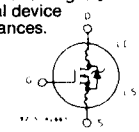
Absolute Maximum Ratings

Parameter		IRF644	IRF645	IRF646	IRF647	Units
V_{DS}	Drain - Source Voltage ①	250	250	275	275	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	250	250	275	275	V
I_D @ T_C = 25°C	Continuous Drain Current	14	13	14	13	A
I_D @ T_C = 100°C	Continuous Drain Current	8.8	8.0	8.8	8.0	A
I_{DM}	Pulsed Drain Current ③	56	52	56	52	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125				W
	Linear Derating Factor	1.0				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	550				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRF646 IRF647	275	—	—	V	V_{GS} = 0V
	IRF644 IRF645	250	—	—	V	I_D = 250μA
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = 20V
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$ On-State Drain Current ②	IRF644 IRF646	14	—	—	A	$V_{DS} > I_{D(on)}$ X $R_{DS(on)max.}$, V_{GS} = 10V
	IRF645 IRF647	13	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF644 IRF646	—	0.20	0.28	Ω	V_{GS} = 10V, I_D = 10A
	IRF645 IRF647	—	0.24	0.34	Ω	
g_{fs} Forward Transconductance ②	ALL	6.7	10	—	S(Ω)	$V_{DS} > I_{D(on)}$ X $R_{DS(on)max.}$, I_D = 10A
C_{iss} Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss} Output Capacitance	ALL	—	320	—	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	69	—	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	16	24	ns	V_{DD} = 90V, I_D = 10A, Z_D = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	—	67	100	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	53	80	ns	
t_f Fall Time	ALL	—	49	74	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	39	59	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	6.6	9.9	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	20	30	nC	
L_D Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

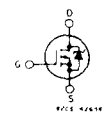


Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS} Case-to-Sink	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRF644 IRF646	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF645 IRF647	—	—	13	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRF644 IRF646	—	—	56	A	
	IRF645 IRF647	—	—	52	A	
V_{SD} Diode Forward Voltage ②	ALL	—	—	1.8	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
t_{rr} Reverse Recovery Time	ALL	150	300	640	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR} Reverse Recovered Charge	ALL	1.6	3.4	7.2	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_j = 25°C, L = 4.5MH, R_{gs} = 25Ω, I_{peak} = 14 A. See figures 14, 15.

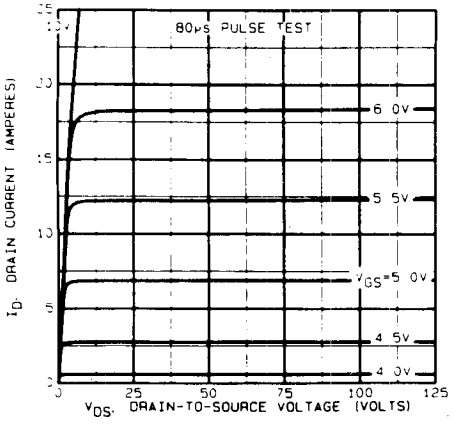


Fig. 1 — Typical Output Characteristics

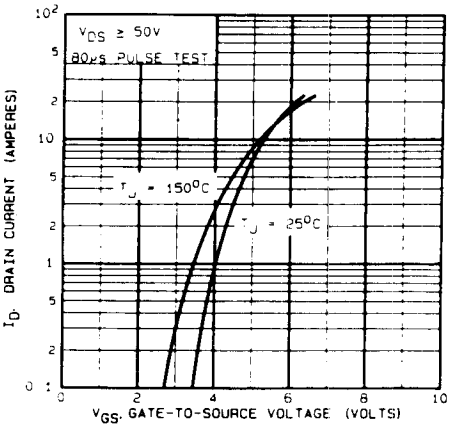


Fig. 2 — Typical Transfer Characteristics

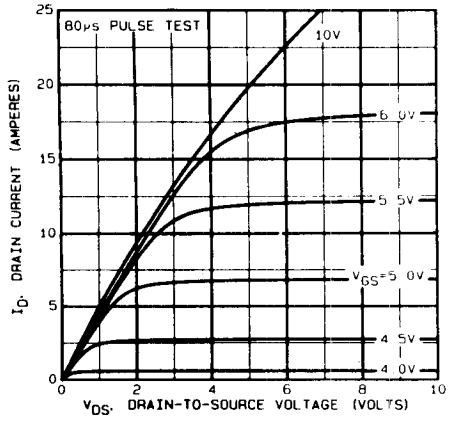


Fig. 3 — Typical Saturation Characteristics

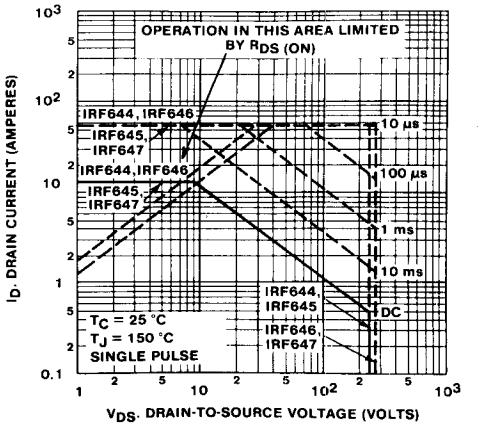


Fig. 4 — Maximum Safe Operating Area

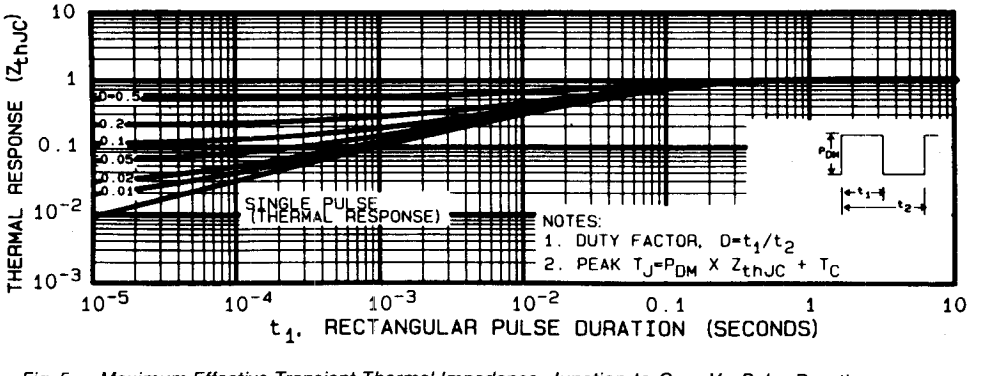


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

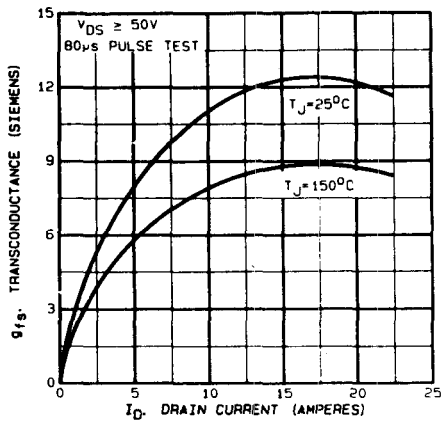


Fig. 6 — Typical Transconductance Vs. Drain Current

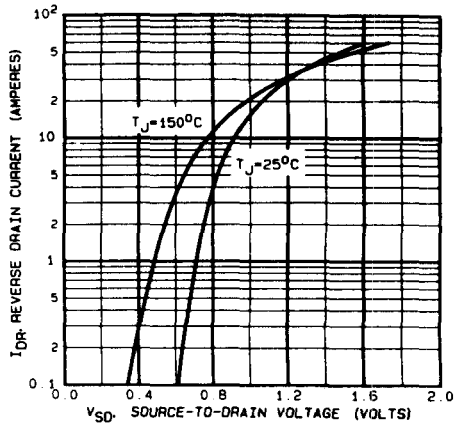


Fig. 7 — Typical Source-Drain Diode Forward Voltage

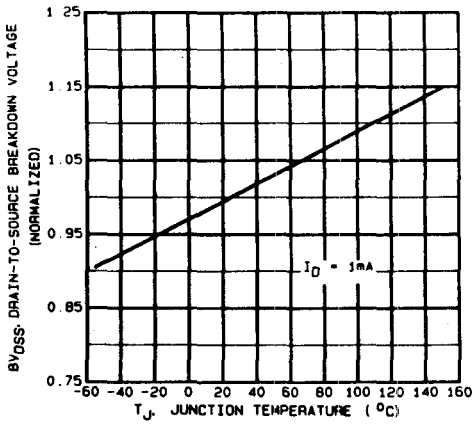


Fig. 8 — Breakdown Voltage Vs. Temperature

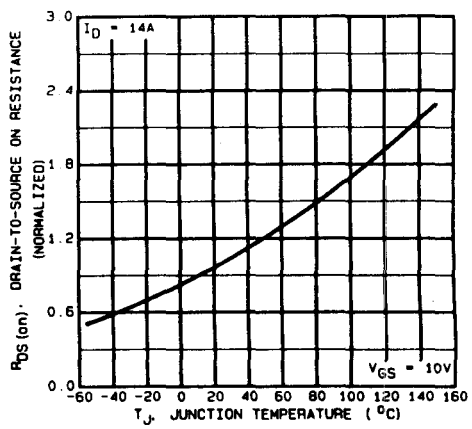


Fig. 9 — Normalized On-Resistance Vs. Temperature

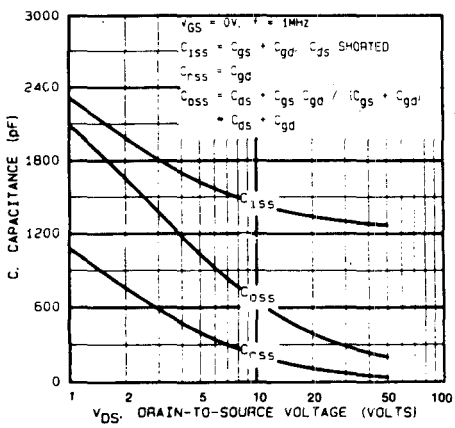


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

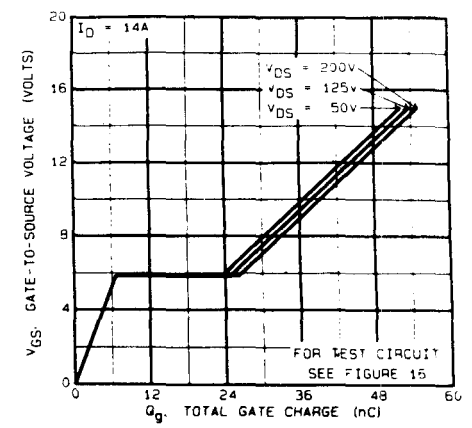


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

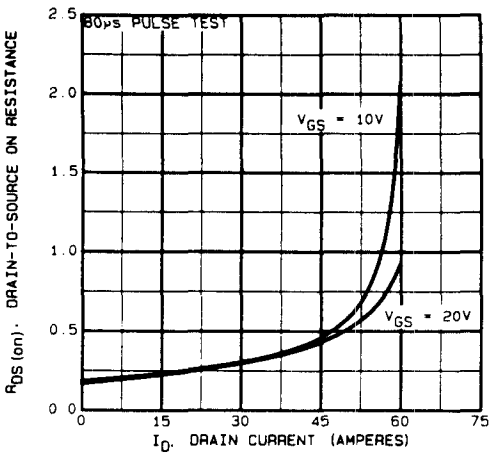


Fig. 12 — Typical On-Resistance Vs. Drain Current

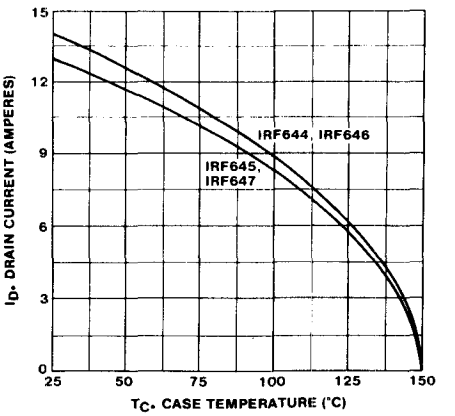


Fig. 13 — Maximum Drain Current Vs. Case Temperature

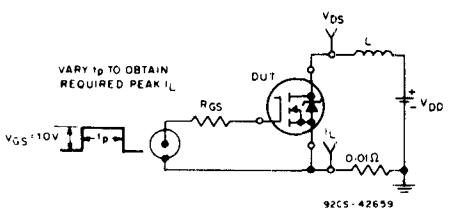


Fig. 14 — Unclamped Energy Test Circuit

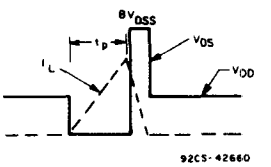


Fig. 15 — Unclamped Energy Waveforms

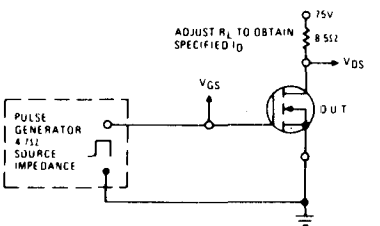


Fig. 16 — Switching Time Test Circuit

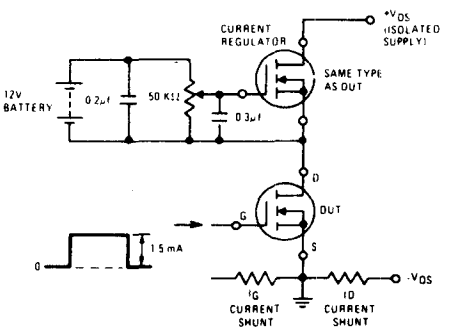


Fig. 17 — Gate Charge Test Circuit