DS2411
Silicon Serial Number with V_{CC} Input

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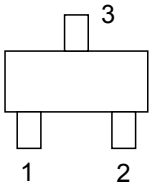
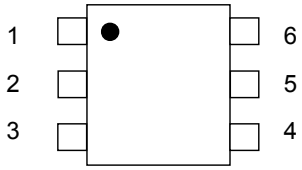
FEATURES

- Unique, Factory-Lasered and Tested 64-Bit Registration Number (8-Bit Family Code Plus 48-Bit Serial Number Plus 8-Bit CRC Tester); Guaranteed No Two Parts Alike
- Standby Current <1µA
- Built-In Multidrop Controller Enables Multiple DS2411s to Reside on a Common 1-Wire® Network
- Multidrop Compatible with Other 1-Wire Products
- 8-Bit Family Code Identifies Device as DS2411 to the 1-Wire Master
- Low-Cost TSOC, SOT23-3, and Flip-Chip Surface-Mount Packages
- Directly Connects to a Single-Port Pin of a Microprocessor and Communicates at up to 15.4kbps
- Overdrive Mode Boosts Communication Speed to 125kbps
- Operating Range: 1.5V to 5.25V, -40°C to +85°C

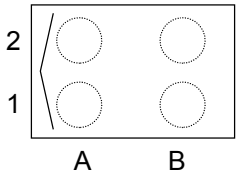
PIN CONFIGURATION



SOT23-3, Top View



TSOC, Top View



Flip Chip, Top View
(Bumps Not Visible)

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
DS2411R/ T&R	-40°C to +85°C	SOT23-3, Tape-and-Reel
DS2411P	-40°C to +85°C	TSOC
DS2411P/ T&R	-40°C to +85°C	TSOC, Tape-and-Reel
DS2411X	-40°C to +85°C	Flip Chip, Tape-and-Reel

PIN DESCRIPTION

NAME	PIN		
	SOT23	TSOC	FLIP CHIP
I/O	1	2	A1
V_{CC}	2	6	B2
GND	3	1	B1
N.C.	—	3	A2
N.C.	—	4	—
N.C.	—	5	—

DESCRIPTION

The DS2411 silicon serial number is a low-cost, electronic registration number with external power supply. It provides an absolutely unique identity that can be determined with a minimal electronic interface (typically, a single port pin of a microcontroller). The DS2411's registration number is a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit family code (01h). Data is transferred serially through the Dallas Semiconductor's 1-Wire protocol. The external power supply is required, extending the operating voltage range of the device below typical 1-Wire devices.

ABSOLUTE MAXIMUM RATINGS*

I/O Voltage to GND	-0.5V to +6V
V_{CC} Voltage to GND	-0.5V to +6V
I/O, V_{CC} Current	±20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A Specification

* *This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

ELECTRICAL CHARACTERISTICS (V_{CC} = 1.5V to 5.25V; T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Temperature	T_A	(Note 1)	-40	+85	°C
Supply Voltage	V_{CC}	(Note 1)	1.5	5.25	V
1-Wire Pullup		$V_{CC} = V_{PUP}$ (Note 1)	1.5	5.25	V
I/O PIN GENERAL DATA					
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)	0.3	2.2	kΩ
Power-Up Delay	t_{PWRP}	V_{CC} stable to first 1-Wire command (Notes 1, 3)	1200		µs
Input Capacitance	C_{IO}	(Note 3)		100	pF
Input Load Current	I_L	$0V \le V(I/O) \le V_{CC}$	-1	+1	µA
Standby Supply Current	I_{CCS}	$V(I/O) \le V_{IL}$, or $V(I/O) \ge V_{IH}$		1	µA
Active Supply Current	I_{CCA}			100	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 3, 4, 5)	0.4	3.2	V
Input Low Voltage	V_{IL}	(Note 1)		0.30	V
Input High Voltage	V_{IH}	(Note 1)	V_{CC} - 0.3		V
Low-to-High Switching Threshold	V_{TH}	(Notes 3, 4, 6)	0.75	3.4	V
Switching Hysteresis	V_{HY}	(Notes 3, 7)	0.18		V
Output Low Voltage at 4mA	V_{OL}	(Note 8)		0.4	V
Rising Edge Holdoff	t_{REH}	Standard speed (Note 9)	1.25	5	µs
		Overdrive speed (Note 9)	0.5	2	
Recovery Time	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ (Note 1)	5		µs
		Overdrive speed, R_{PUP} = 2.2kΩ (Note 1)	2		
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ (Note 1)	5		
Timeslot Duration	t_{SLOT}	Standard speed	65		µs
		Overdrive $V_{CC} \ge 2.2V$	8		
		Overdrive $V_{CC} \ge 1.5V$	10		

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
I/O PIN, 1-Wire RESET, PRESENCE DETECT CYCLE					
Reset Low Time	t_{RSTL}	Standard speed	480	640	µs
		Overdrive speed	60	80	
Presence-Detect High Time	t_{PDH}	Standard speed	15	60	µs
		Overdrive $V_{CC} \geq 2.2V$	2	6	
		Overdrive $V_{CC} \geq 1.5V$	2	8.5	
Presence-Detect Low Time	t_{PDL}	Standard speed	60	240	µs
		Overdrive $V_{CC} \geq 2.2V$	8	24	
		Overdrive $V_{CC} \geq 1.5V$	8	30	
Presence-Detect Fall Time	t_{FPD}	Standard speed (Note 10)	0.4	8	µs
		Overdrive speed (Note 10)	0.05	1	
Presence-Detect Sample Time	t_{MSP}	Standard speed (Note 1)	60	75	µs
		Overdrive $V_{CC} \geq 2.2V$ (Note 1)	6	10	
		Overdrive $V_{CC} \geq 1.5V$ (Note 1)	8.5	10	
I/O PIN, 1-Wire WRITE					
Write-0 Low Time	t_{W0L}	Standard speed (Notes 1, 13)	60	120	µs
		Overdrive $V_{CC} \geq 2.2V$ (Notes 1, 13)	6	16	
		Overdrive $V_{CC} \geq 1.5V$ (Notes 1, 13)	8	16	
Write-1 Low Time	t_{W1L}	Standard speed (Notes 1, 11, 13)	5	15 - ε	µs
		Overdrive speed (Notes 1, 11, 13)	1	2 - ε	
I/O PIN, 1-Wire READ					
Read Low Time	t_{RL}	Standard speed (Notes 1, 11)	5	15 - ε	µs
		Overdrive speed (Notes 1, 11)	1	2 - ε	
Read Sample Time	t_{MSR}	Standard speed (Notes 1, 12)	$t_{RL} + \delta$	15	µs
		Overdrive speed (Notes 1, 12)	$t_{RL} + \delta$	2	

Note 1: System requirement.

Note 2: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required. Minimum allowable pullup resistance is slightly greater than the value necessary to produce the absolute maximum current (20mA) during 1-Wire low times at V_{PUP} = 5.25V assuming V_{OL} = 0V.

Note 3: Not production tested.

Note 4: V_{TL} and V_{TH} are functions of V_{CC} and temperature.

Note 5: Voltage below which during a falling edge on I/O, a logic '0' is detected.

Note 6: Voltage above which during a rising edge on I/O, a logic '1' is detected.

Note 7: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O has to drop by V_{HY} to be detected as logic '0'.

Note 8: The I-V characteristic is linear for voltages less than 1V.

Note 9: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the previous edge.

Note 10: Interval during the negative edge on I/O at the beginning of a presence-detect pulse between the time at which the voltage is 90% of V_{PUP} and the time at which the voltage is 10% of V_{PUP}.

Note 11: ε represents the time required for the pullup circuitry to pull the voltage on I/O up V_{IL} to V_{TH}.

Note 12: δ represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input-high threshold of the bus master.

Note 13: Interval begins when the voltage drops below V_{TL} during a negative edge on I/O and ends when the voltage rises above V_{TH} during a positive edge on I/O.

OPERATION

The DS2411's registration number is accessed through a single data line. The 48-bit serial number, 8-bit family code, and 8-bit CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are bus-master-generated falling edges on the I/O pin. All data is read and written least significant bit first. The device requires a delay between V_{CC} power-up and initial 1-Wire communication, t_{PWRP} (1200µs). During this time the device may issue presence-detect pulses.

1-Wire BUS SYSTEM

The 1-Wire bus has a single bus master and one or more slaves. In all instances, the DS2411 is a slave device. The bus master is typically either a microcontroller or a Dallas Semiconductor bridge chip such as the DS2480, DS2490, or DS1481. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing).

Hardware Configuration

The 1-Wire bus has a single data line, I/O. It is important that each device on the bus be able to drive I/O at the appropriate time. To facilitate this, each device has an open-drain or three-state output. The DS2411 has an open-drain output with an internal circuit equivalent to that shown in Figure 3. The bus master can have the same equivalent circuit. If a bidirectional pin is not available on the master, separate output and input pins can be connected together. The bus requires a pullup resistor at the master end of the bus, as shown in Figure 4. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 15.4kbps in standard speed and 125kbps in overdrive.

The idle state for the 1-Wire bus is high. If a transaction needs to be suspended for any reason, I/O must remain high if the transaction is to be resumed. If the bus is pulled low, slave devices on the bus will interpret the low as either a timeslot, or a reset depending on the duration.

Figure 1. DS2411 REGISTRATION NUMBER

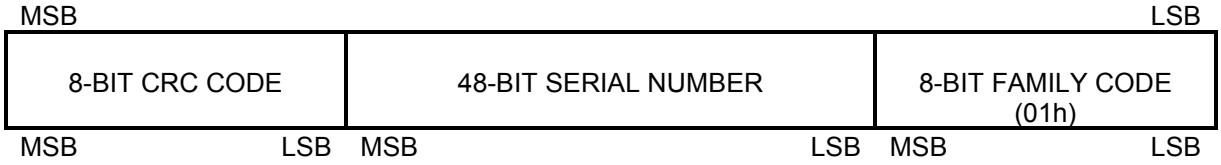


Figure 2. 1-WIRE CRC GENERATOR

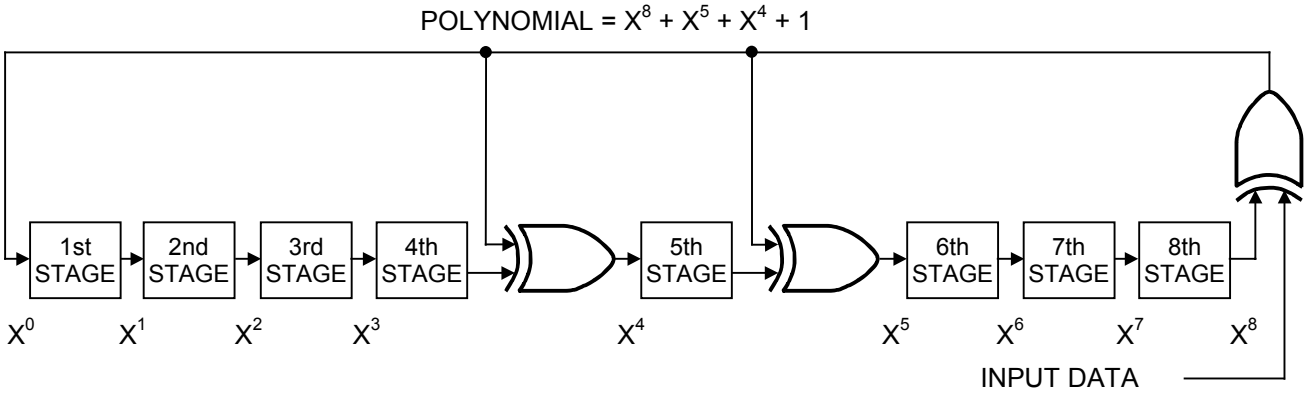


Figure 3. DS2411 EQUIVALENT CIRCUIT

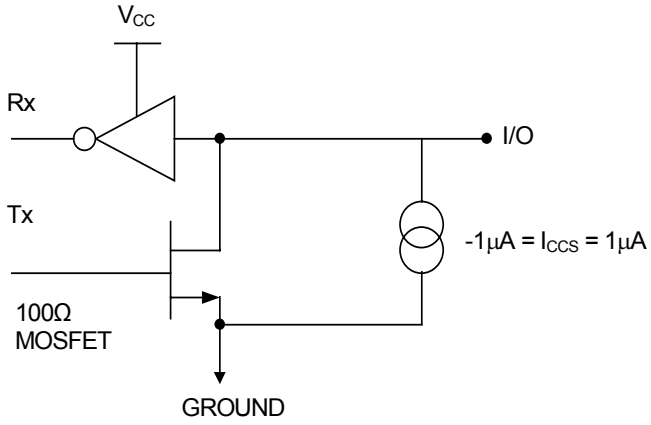
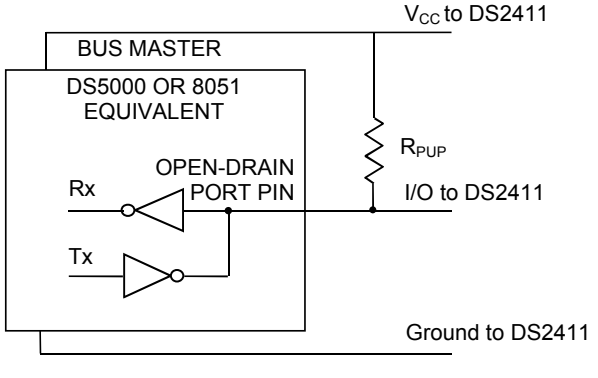


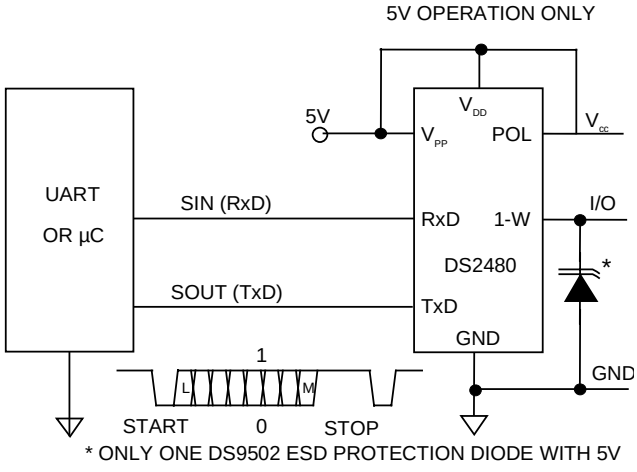
Figure 4. BUS MASTER CIRCUIT

a) Open Drain



R_{PUP} must be between 0.3 kΩ and 2.2 kΩ. The optimal value depends on the 1-Wire communication speed and the bus load characteristics.

b) DS2480B Serial Bridge



TRANSACTION SEQUENCE

The communication sequence for accessing the DS2411 through the 1-Wire bus is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2411 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the three ROM function commands. All ROM function command codes are 1 byte long. A list of these commands follows (see the flowchart in Figure 5).

Read ROM [33h]

This command allows the bus master to read the DS2411's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command should only be used if there is a single slave device on the bus. If more than one slave is present on the bus, a data collision results when all slaves try to transmit at the same time (open drain produces a wired-AND result), and the resulting registration number read by the master will be invalid.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the romcode tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to App Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Overdrive Skip ROM [3Ch]

This command causes all overdrive-capable slave devices on the 1-Wire network to enter overdrive speed (OD = 1). All communication following this command has to occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to regular speed (OD = 0).

To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed has to be issued followed by a read ROM or search ROM command sequence. Overdrive speeds up the time for the search process.

1-Wire SIGNALING

The DS2411 requires a strict protocol to ensure data integrity. The protocol consists of four types of signaling on the I/O pin: initialization sequence with reset pulse and presence pulse, write 0, write 1, and read data. All high-to-low transitions except the presence pulse are initiated by the bus master. The DS2411 can communicate at two different speeds: standard and overdrive. If not explicitly placed into overdrive speed, the DS2411 communicates at standard speed.

The initialization sequence required to begin any communication with the DS2411 is shown in Figure 6. A reset pulse followed by a presence pulse indicates that the DS2411 is ready to send or receive. The bus master transmits (Tx) a reset pulse by driving I/O low for t_{RSTL} (minimum 480µs at regular speed, 60µs at overdrive speed). The bus master then releases I/O and goes into receive mode (Rx). I/O is pulled high by the 2.2kΩ pullup resistor. After detecting a high level on I/O, the DS2411 waits for t_{PDH} (15µs to 60µs at standard speed, 2µs to 8.5µs at overdrive speed) and then transmits the presence pulse by driving I/O low for t_{PDL} (60µs to 240µs at standard speed, 8µs to 30µs at overdrive speed). A reset pulse of 480µs or longer exits overdrive speed and returns to standard speed. If the DS2411 is in overdrive speed and the reset pulse is no longer than 80µs, it is guaranteed to remain in overdrive speed.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 7. All time slots are initiated by the master driving the I/O pin low. The falling edge on I/O synchronizes the DS2411 to the master by triggering a delay circuit in the DS2411. During write time slots, the delay circuit determines when the DS2411 samples the I/O pin. For a read data time slot, if a "0" is to be transmitted by the DS2411, the delay circuit determines how long the DS2411 drives the I/O pin low, such that it stays low even after the master releases it. If the data bit is a 1, the DS2411 does not drive the I/O pin low, thus allowing I/O to return high after the master releases it.

CRC GENERATION

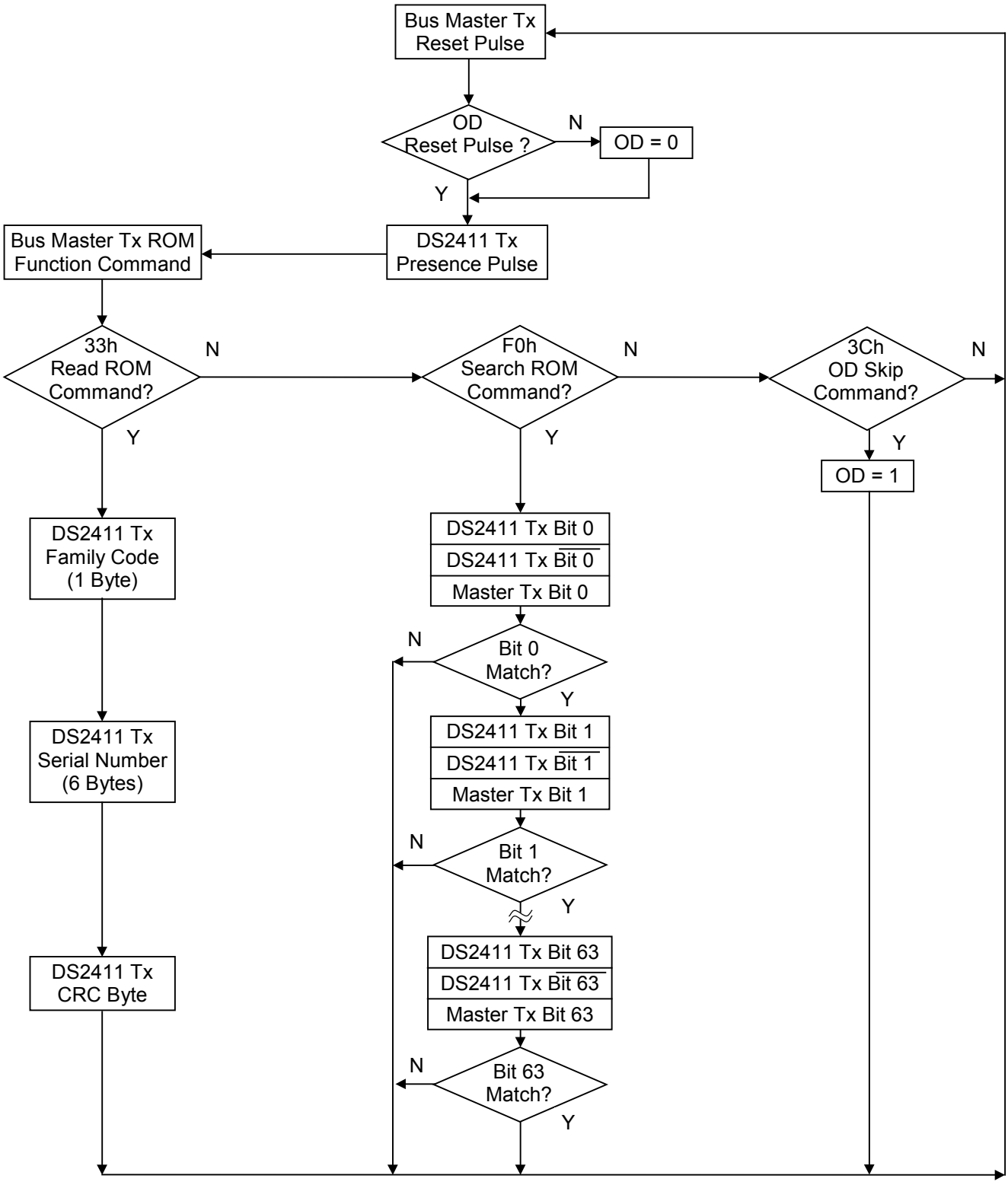
To validate the registration number transmitted from the DS2411, the bus master can generate a CRC value from the 8-bit family code and unique 48-bit serial number as it is received. If the CRC matches the last 8 bits of the registration number, the transmission is error free.

The equivalent polynomial function of this CRC is: $CRC = x^8 + x^5 + x^4 + 1$.

CUSTOM DS2411

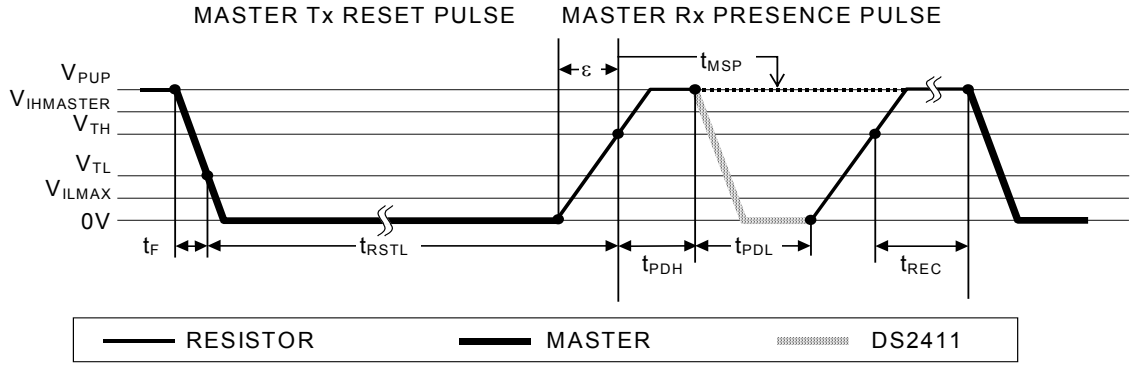
Customization of a portion of the unique 48-bit serial number by the customer is available. Dallas Semiconductor will register and assign a specific customer ID in the 12 most significant bits of the 48-bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non-selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your Maxim/Dallas Semiconductor sales representative for more information.

Figure 5. ROM FUNCTIONS FLOW CHART



INITIALIZATION PROCEDURE

Figure 6. Reset and Presence Pulse



READ/WRITE TIMING DIAGRAM

Figure 7a. Write-One Time Slot

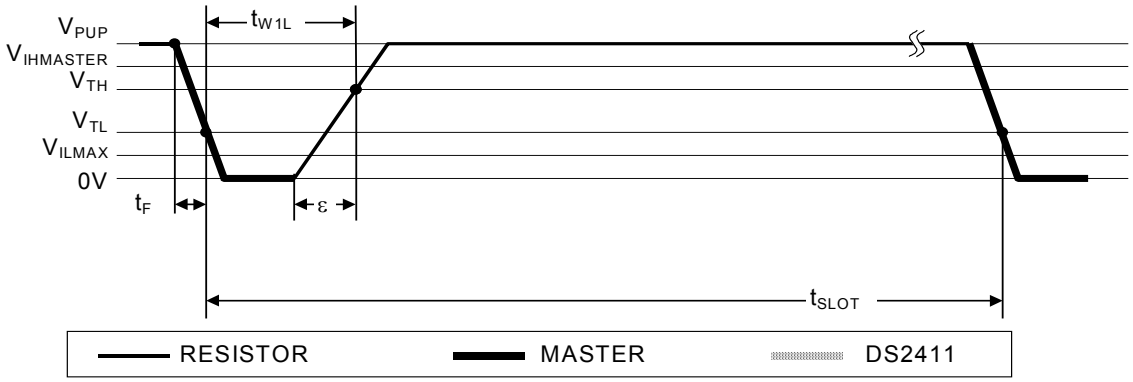


Figure 7b. Write-Zero Time Slot

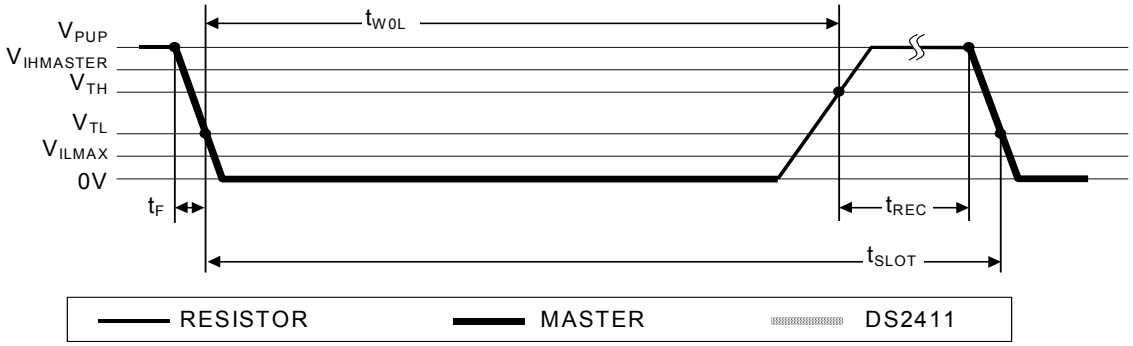


Figure 7c. Read-data Time Slot