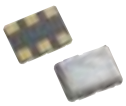
CRYSTAL OSCILLATORS
LVPECL/LVDS 3.3V

SURFACE MOUNT
RF Models



5 x 7 mm Surface Mount
0º to 70ºC or -40º to +85ºC
750 KHz to 800 MHz

FEATURES
- High speed – Low jitter LVPECL or LVDS output with tristate
- Small SMD package – 5 x 7mm
- Stability options: 100, 50, 25 or 20 ppm
- Commercial or industrial temperature range
- Rugged, hermetic package for automated assembly

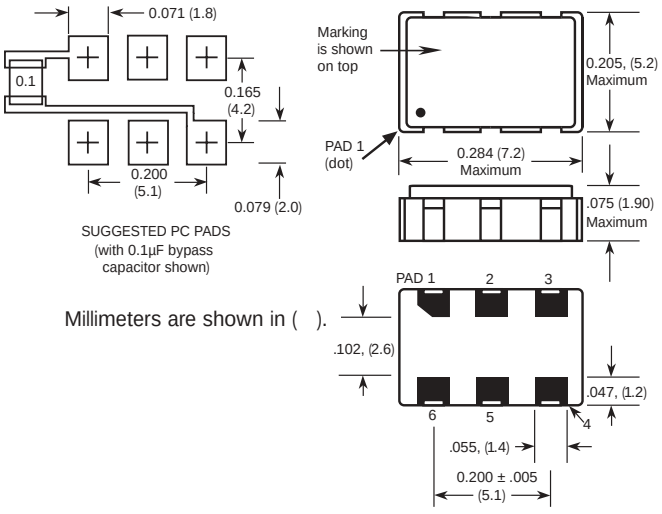
TYPICAL APPLICATIONS
- Telecom/networking systems that require low jitter clocks
  - DSL
  - Gigabit ethernet
  - Fibre Channel
  - Optical networking

Description

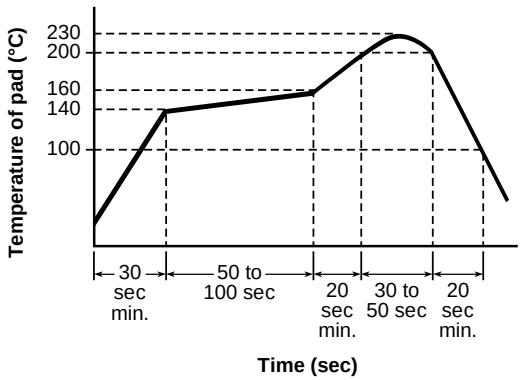
MF Electronics RF surface mount oscillators provide waveforms for clocking LVPECL and LVDS circuits. The new 5 x 7mm footprint package provides the performance of larger oscillators with a new level of board space reduction achieved. ASIC technology is used to accomplish size reduction and enhance performance and reliability. Low jitter output signals are generated. The wide range of frequencies offered, many stability options, and industrial temperature range availability, make this model the solution for many applications. A tristate function is included to allow for easy automated testing of assemblies. Tape and reel packaging is standard.

CONNECTIONS

PIN 1	Tristate
PIN 2	N/C
PIN 3	Ground
PIN 4	Output 1: Q
PIN 5	Output 2: $\overline{Q}$
PIN 6	$+V_{DD}$



Outline Drawing



Recommended Reflow Soldering Profile

MF ELECTRONICS

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5 x 7 mm Surface Mount
0º to 70º or -40º to +85ºC
750 KHz to 800 MHz

ELECTRICAL SPECIFICATIONS

Frequency Range 750 KHz to 800 MHz

Frequency Stability
Includes calibration at 25°C, operating temperature, change of input voltage, change of load, shock and vibration. 100, 50, 25 or 20 ppm

	MIN	TYP	MAX	UNITS
Input Voltage, V_{DD}	3.15	3.3	3.45	volts
Jitter				
Period jitter RMS				
19.44MHz		5		ps
77.76MHz		8		ps
155.52MHz		9		ps
622.08MHz		10		ps
Integrated jitter RMS				
12 KHz to 20 MHz @ 155.52MHz		3	5	ps
Symmetry at (V_{DD}-1.3)V_{DC} (PECL)	40	50	60	percent
at (1.25 V_{DC}) (LVDS)	40	50	60	percent
Aging				
First year		3		ppm
After first year		1		ppm/yr

Tristate
Input Requirements for Pin 1.:
"1": On – Pin 1 may float or 2.8V min
"0": Tristate – Pin 1 requires 0.4V max

Typical Phase Noise (dBc/Hz)	***10Hz***	***100Hz***	***1KHz***	***10KHz***	***100KHz***
Oscillator Frequency					
19.44MHz	-60	-90	-112	-140	-140
106.25MHz	-60	-90	-112	-127	-125
155.52MHz	-60	-90	-112	-125	-123
622.08MHz	-60	-90	-109	-110	-109

ENVIRONMENTAL SPECIFICATIONS

Temperature

Operating	Commercial: 0º to 70°C, Industrial: -40º to +85ºC
Storage	-55º to +125°C

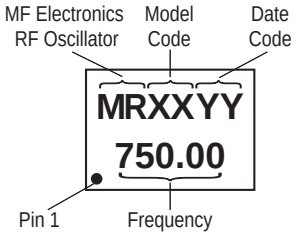
Shock – 1000 Gs, 0.35 ms, 1/2 sine wave, 3 shocks in each plane
Vibration – 10-2000 Hz of .06" d.a. or 20 Gs, whichever is less
Humidity – Resistant to 85° R.H. at 85°C

MECHANICAL SPECIFICATIONS

Leak – MIL STD 883, Method 1014, condition A1
Case – Ceramic with hermetic resistance-welded metal lid
Pads – Solderable gold over nickel
Marking – Epoxy ink or laser engraved
Resistance to Solvents – MIL STD 202, Method 215

MARKING SPECIFICATION

The format for the marking is:



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PECL OUTPUT MODELS
ELECTRICAL SPECIFICATIONS

	MIN	TYP	MAX	UNITS
RL = 50 Ω to (V_{DD} – 2V) (see figure)				
Output High Voltage, V_{OH}		V_{DD} – 1.025		V
Output Low Voltage, V_{OL}			V_{DD} – 1.620	V
Input Current, PECL				
0.75 – 24 MHz			25	mA
24 – 160 MHz			65	mA
160 – 800 MHz			100	mA
Switching Characteristics				
Clock Rise Time, tr @20/80%		0.3	0.35	ns
Clock Fall Time, tf @80/20%		0.3	0.35	ns

LVDS OUTPUT MODELS
ELECTRICAL SPECIFICATIONS

	MIN	TYP	MAX	UNITS
RL = 100 Ω (see figure)				
Output Differential Voltage, V_{OD}	247	355	454	mV
Output High Voltage, V_{OH}		1.4	1.6	V
Output Low Voltage, V_{OL}	0.9	1.1		V
Offset Voltage, V_{OS}	1.125	1.2	1.375	V
Input Current, LVDS				
0.75 – 24 MHz			25	mA
24 – 96 MHz			45	mA
96 – 800 MHz			80	mA
Switching Characteristics				
Differential Clock Rise Time, tr		0.3	0.4	ns
Differential Clock Fall Time, tf		0.3	0.4	ns

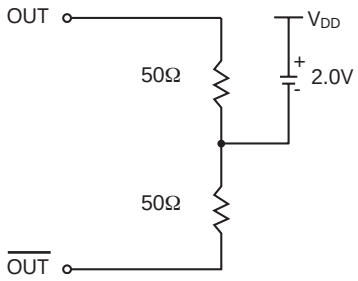

Fig 1.
PECL Levels Test Circuit

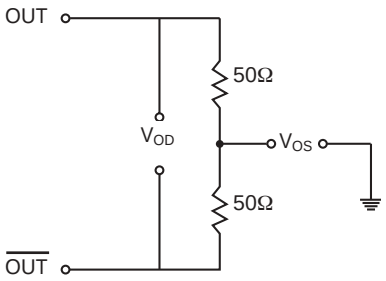

Fig 2.
LVDS Test Load

HOW TO ORDER

For Part Number, insert option codes after model type, and add frequency, for example:

RF A A T A 125 M

- Frequency Stability: A = ±100 ppm; B = ±50 ppm; C = ±25 ppm; D = ±20 ppm
- Temperature Range of Operation: A = 0 to 70ºC; B = -40 to +85ºC
- Tristate: T = Tristate; N = No Tristate
- Output Logic: A = 45/55% LVDS; B = 40/60% LVDS; C = 45/55% PECL; D = 40/60% PECL
- Frequency
- M = MHz; K = KHz

SS#	Rev.
RF	A