Customer-Programmable Linear Hall-Effect Sensor Optimized for Use in Current Sensing Applications

Not for New Design

These parts are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.

Date of status change: July 2, 2018

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the ACS73369.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Customer-Programmable Linear Hall-Effect Sensor Optimized for Use in Current Sensing Applications

FEATURES AND BENEFITS

- Customer-programmable offset and sensitivity
- Sensitivity and QVO temperature coefficients programmed at Allegro for improved accuracy
- Output value decreases with south magnetic field and increases with north magnetic field.
- 3-pin SIP package for easy integration with magnetic concentrator
- Low noise, moderate bandwidth analog output
- High-speed chopping scheme minimizes QVO drift over temperature
- Temperature-stable quiescent voltage output and sensitivity
- Precise recoverability after temperature cycling
- Output voltage clamps provide short-circuit diagnostic capabilities
- Undervoltage lockout (UVLO)
- Wide ambient temperature range: –40°C to 85°C
- Immune to mechanical stress

PACKAGE:

3-pin SIP
(suffix UA)

Not to scale

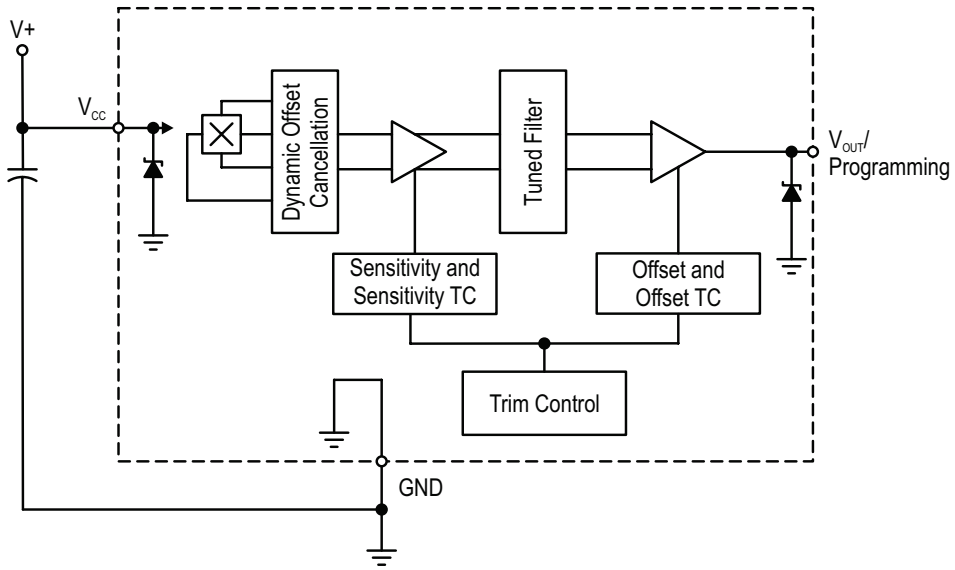
DESCRIPTION

The Allegro™ A1369 is a customer-programmable, high accuracy linear Hall-effect-based current sensor IC. It is packaged in a thin 3-pin SIP to allow for easy integration with a magnetic core to create a highly accurate current sensing module. The programmable nature of the A1369 enables it to account for manufacturing tolerances in the final current sensing module assembly.

This temperature-stable device is available in a through-hole single in-line package (TO-92). The accuracy of the device is enhanced via programmability on the output pin for end-of-line optimization without the added complexity and cost of a fully programmable device. The device features One-Time-Programming (OTP), using nonvolatile memory, to optimize device sensitivity and the quiescent output voltage (QVO) (output with no magnetic field) for a given application or circuit. The A1369 also allow for optimized performance over temperature through programming the temperature coefficient for both Sensitivity and QVO at Allegro end-of-line test.

These ratiometric Hall-effect sensor ICs provide a voltage output that is proportional to the applied magnetic field. The quiescent voltage output is user-adjustable around 50% of the supply voltage, and the output sensitivity is programmable within a range of –8.5 mV/G to –12.5 mV/G for the A1369-10 and –22 mV/G to –26 mV/G for the A1369-24.

The features of this linear device makes it ideal for use in industrial applications requiring high accuracy and are guaranteed over a wide temperature range, –40°C to 85°C.



Functional Block Diagram

SELECTION GUIDE*

Part Number	Sensitivity Range (mV/G)
A1369EUA-10-T	–8.5 to –12.5
A1369EUA-24-T	–22 to –26

*Contact Allegro™ for additional packing options.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		15	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	V_{OUT} to GND	2	mA
Output Sink Current	$I_{OUT(SINK)}$	V_{CC} to V_{OUT}	10	mA
Operating Ambient Temperature	T_A		–40 to 85	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package UA, on 1-layer PCB with copper limited to solder pads	165	°C/W

*Additional thermal information available on the Allegro website.

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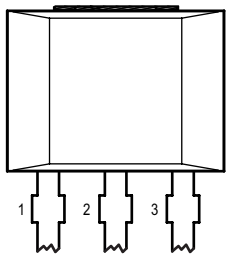
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package UA, 3-Pin SIP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCC	Input power supply; tie to GND with bypass capacitor
2	GND	Ground
3	VOUT	Output Signal; also used for programming

ELECTRICAL CHARACTERISTICS: Valid over T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Undervoltage Threshold [1]	V_{UVLOHI}	T_A = 25°C (device power on)	–	–	3	V
	$V_{UVLOLOW}$	T_A = 25°C (device power on)	2.5	–	–	V
Supply Current	I_{CC}	No load on V_{OUT}	–	9	12	mA
Power-On Time [2]	t_{PO}	T_A = 25°C, $C_{L(PROBE)}$ = 10 pF	–	60	–	µs
Delay to Clamp [3]	t_{CLP}	T_A = 25°C, C_L = 10 nF	–	30	–	µs
Supply Zener Clamp Voltage	V_Z	T_A = 25°C, I_{CC} = 24.5 mA	6	7.3	–	V
Internal Bandwidth	BW_i	Small signal –3 dB	–	7	–	kHz
Chopping Frequency [4]	f_C	T_A = 25°C	–	400	–	kHz
OUTPUT CHARACTERISTICS						
Output Referred Noise [5]	V_N	T_A = 25°C, Sens = 10.5 mV/G, C_L = 1 nF	–	10	–	$mV_{(p-p)}$
		T_A = 25°C, Sens = 24 mV/G, C_L = 1 nF	–	24	–	$mV_{(p-p)}$
Input Referred Noise Density	V_{NRMS}	T_A = 25°C, No load out V_{OUT}, f <<BW_i	–	1.5	–	mG/√Hz
DC Output Resistance	R_{OUT}		–	<1	–	Ω
Output Load Resistance	R_L	V_{OUT} to GND	4.7	–	–	kΩ
Output Load Capacitance	C_L	V_{OUT} to GND	–	–	1	nF
Output Voltage Clamp [6]	$V_{CLP(HIGH)}$	T_A = 25°C, B = +X G; R_L = 10 kΩ (V_{OUT} to GND)	4.55	–	–	V
	$V_{CLP(LOW)}$	T_A = 25°C, B = –X G; R_L = 10 kΩ (V_{OUT} to GND)	–	–	0.45	V
INITIAL QVO and SENSITIVITY						
Pre-Programming Quiescent Voltage Output	$V_{OUT(Q)init}$	B = 0 G, T_A = 25°C	–	2.5	–	V
Pre-Programming Sensitivity	$Sens_{init}$	A1369-10, T_A = 25°C	–	–10	–	mV/G
		A1369-24, T_A = 25°C	–	–24	–	mV/G
Target Sensitivity Temperature Coefficient	TC_{Sens}	T_A = 85°C, calculated relative to 25°C	–	0	–	%/°C
Target Quiescent Voltage Output Drift	$\Delta V_{OUT(Q)}$	T_A = 85°C, calculated relative to 25°C	–	0	–	%/°C

Continued on the next page…

[1] On power-up, the output of the A1369 will be held low until V_{CC} exceeds V_{UVLOHI}. Once powered, the output will remain valid until V_{CC} drops below V_{UVLOLO}, when the output will be pulled low.
[2] See Characteristic Definitions.
[3] See Characteristic Definitions.
[4] f_C varies up to approximately ±20% over the full operating ambient temperature range and process.
[5] Value is derived as 6 sigma value from the spectral noise density.
[6] $V_{CLP(LOW)}$ and $V_{CLP(HIGH)}$ will scale with V_{CC} due to ratiometry.

ELECTRICAL CHARACTERISTICS (continued): Valid over T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CUSTOMER QUIESCENT VOLTAGE OUTPUT PROGRAMMING						
Guaranteed Quiescent Voltage Output Range [7]	$V_{OUT(Q)}$	T_A = 25°C	2.45	–	2.55	V
Quiescent Voltage Output Programming Bits			–	5	–	bits
Average Quiescent Voltage Output Step Size [8][9]	$Step_{VOUT(Q)}$	T_A = 25°C	4.75	7.5	10.5	mV
Quiescent Voltage Output Programming Resolution [10]	$Err_{PGVOUT(Q)}$	T_A = 25°C	–	$Step_{VOUT(Q)}$ × ±0.5		
CUSTOMER SENSITIVITY PROGRAMMING						
Sensitivity Programming Bits			–	7	–	bits
Guaranteed Fine Step Sensitivity Range [11]	Sens	A1369-10, T_A = 25°C	–8.5	–	–12.5	mV/G
		A1369-24, T_A = 25°C	–22	–	–26	mV/G
Average Sensitivity Step Size [8][9]	$Step_{Sens}$	A1369-10, T_A = 25°C	–72	–102	–133	µV/G
		A1369-24, T_A = 25°C	–163	–233	–303	µV/G
Sensitivity Programming Resolution [10]	$Err_{PROGSENS}$	T_A = 25°C	–	$Step_{Sens}$ × ±0.5	–	µV/G
CUSTOMER CLAMP DISABLE PROGRAMMING						
Clamp Disable Bit			–	1	–	bit
Output Voltage [12]	$V_{SAT,HIGH}$	B = –X G; R_L = 4.7 kΩ (V_{OUT} to GND)	4.75	–	–	V
	$V_{SAT,LOW}$	B = + X G; R_L = 4.7 kΩ (V_{OUT} to GND)	–	–	0.25	V
CUSTOMER LOCK						
Overall Programming Lock Bit	LOCK		–	1	–	bit
ERROR COMPONENTS [13]						

Continued on the next page…

[7] $V_{OUT(Q)(max)}$ is the value available with all programming fuses blown (maximum programming code set). $V_{OUT(Q)}$ is the total range from $V_{OUT(Q)init}$ up to and including $V_{OUT(Q)(max)}$. See Characteristic Definitions.
[8] Step size is larger than required to account for manufacturing spread. See Characteristics Definitions.
[9] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be twice the maximum specified value of $StepV_{OUT(Q)}$ or $Step_{SENS}$.
[10] Fine programming value accuracy. See Characteristic Definitions.
[11] $Sens_{(max)}$ is the value available with all programming fuses blown (maximum programming code set). Sens range is the total range from $Sens_{init}$ up to and including $Sens_{(max)}$. See Characteristic Definitions.
[12] $V_{SAT,HIGH}$ and $V_{VSAT,LOW}$ will scale with the supply voltage due to the Ratiometry of the part.

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ELECTRICAL CHARACTERISTICS (continued): Valid over T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Linearity Sensitivity Error	Lin_{ERR}	A1369-10	–	±1.0	–	%
		A1369-24	–	±1.5	–	%
Symmetry Sensitivity Error	Sym_{ERR}	A1369-10	–	±1.5	–	%
		A1369-24	–	±1.7	–	%
Ratiometry Quiescent Voltage Output Error[14]	$Rat_{VOUT(Q)}$	A1369-10, over guaranteed supply voltage (relative to V_{CC} = 5 V)	–	±0.5	–	%
		A1369-24, over guaranteed supply voltage (relative to V_{CC} = 5 V)	–	±0.5	–	%
Ratiometry Sensitivity Error	Rat_{SENS}	A1369-10, over guaranteed supply voltage (relative to V_{CC} = 5 V)	–	±1.0	–	%
		A1369-24, over guaranteed supply voltage (relative to V_{CC} = 5 V)	–	±1.0	–	%
Ratiometry Clamp Error	$Rat_{VOUTVLP}$	A1369-10, over guaranteed supply voltage (relative to V_{CC} = 5 V), T_A = 25°C	–	±0.5	–	%
		A1369-24, over guaranteed supply voltage (relative to V_{CC} = 5 V), T_A = 25°C	–	±0.5	–	%
ADDITIONAL CHARACTERISTICS[15]						
Guaranteed Quiescent Voltage Output Drift Through Temperature Range	$\Delta V_{OUT(Q)}$	A1369-10, T_A = 85°C	−20	–	+20	mV
		A1369-24, T_A = 85°C	−30	–	+30	mV
		A1369-10, T_A = -40°C	–	±40	–	mV
		A1369-24, T_A = -40°C	–	±50	–	mV
Sensitivity Drift Through Temperature Range	$\Delta Sens_{TC}$	A1369-10, measured at 85°C, calculated relative to 25°C	–	±1.6	–	%
		A1369-24, measured at 85°C, calculated relative to 25°C		±1.8		%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C; after temperature cycling	–	±2	–	%

[13] Typical error is based on ±3 σ value of sample distribution.
[14] Percent change from actual value at V_{CC} = 5 V for a given temperature.
[15] Typical error is based on ±3 σ value around mean value of sample distribution.

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CHARACTERISTIC DEFINITIONS

Power-On Time. When the supply is ramped to its operating voltage, the device output requires a finite time to react to an input magnetic field. Power-on time is defined as the time it takes for the output voltage begin responding to an applied magnetic field after the power supply has reached its minimum specified operating voltage, V_{CC}(min).

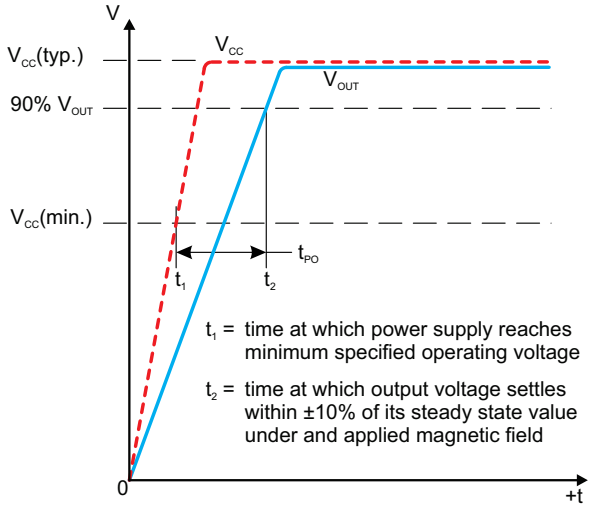

Figure 1: Power-On Time

Delay to Clamp. A large magnetic input step may cause the clamp to overshoot its steady-state value. The delay to clamp is defined as the time it takes for the output voltage to settle within 1% of its steady-state value after initially passing through its steady-state voltage.

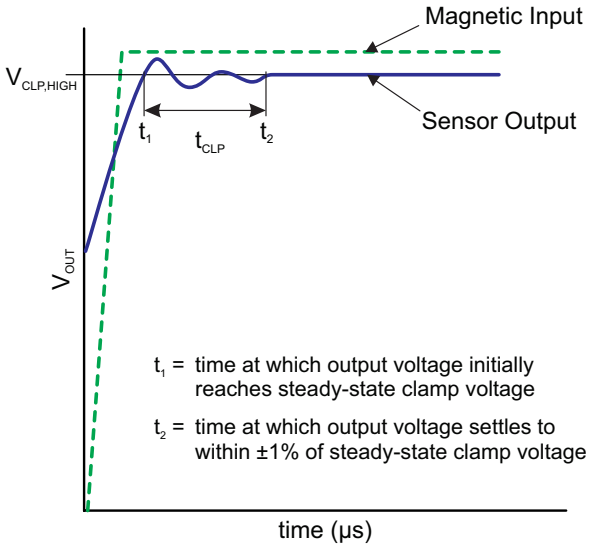

Figure 2: Delay to Clamp

Guaranteed Quiescent Voltage Output Range. The quiescent voltage output can be programmed around 2.5 V within the guaranteed quiescent voltage range limits, $V_{OUT(Q)(max)}$ and $V_{OUT(Q)(min)}$. The available guaranteed programming range falls within the distribution of initial $V_{OUT(Q)}$ and the maximum code $V_{OUT(Q)}$.

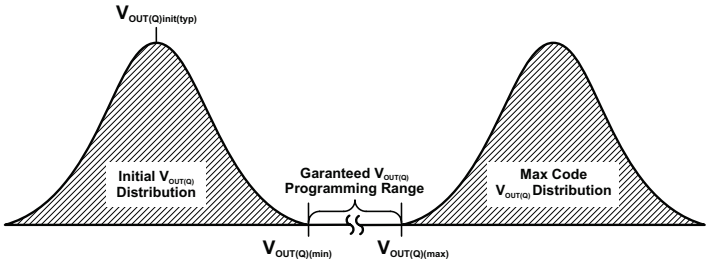

Figure 3: QVO Range

Average Quiescent Voltage Output Step Size. The average quiescent voltage output step size for a single device is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)}(2^N - 1) - V_{OUT(Q)init}}{2^N - 1}$$

where N is the number of available programming bits in the trim range. $2^N - 1$ is the value of the maximum programming code in the range.

Quiescent Voltage Output Programming Resolution. The programming resolution for any device is half of its programming step size. Therefore the typical programming resolution will be:

$$0.5 \times Step_{VOUT(Q)(typ)}$$

Quiescent Voltage Output Drift Through Temperature Range. Due to internal component tolerances and thermal considerations the quiescent voltage output, $\Delta V_{OUT(Q)}$, may drift from its nominal value over the operating ambient temperature, T_A. For purposes of specification, the Quiescent Voltage Output Drift Through Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q,\,TA)} - V_{OUT(Q,\,25°C)}$$

Sensitivity. The presence of a south pole magnetic field perpendicular to the branded surface of the package face increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north pole will decrease the output voltage from

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its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device and is defined as:

$$Sens = \frac{V_{OUT(B+)} - V_{OUT(B-)}}{B^+ - B^-}$$

where B+ and B- are two magnetic fields with opposite polarities.

Guaranteed Sensitivity Range. The magnetic sensitivity can be programmed around its nominal value within the sensitivity range limits, $Sens_{(max)}$ and $Sens_{(min)}$. Refer to the section on guaranteed quiescent voltage output range for a conceptual explanation.

Average Sensitivity Step Size. Refer to the section on average quiescent voltage output step size for a conceptual explanation.

Sensitivity Programming Resolution. Refer to the section on quiescent voltage output programming resolution for a conceptual explanation.

Sensitivity Temperature Coefficient. The device sensitivity changes over temperature with respect to its sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 85°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{SENS} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\%\right)\left(\frac{1}{T2 - T1}\right)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 85°C.

The ideal value of sensitivity over temperature, $Sens_{IDEAL(TA)}$, is defined as:

$$Sens_{IDEAL(TA)} = Sens_{T1} \times (100\% + TC_{SENS}(T_A - T1))$$

Guaranteed Sensitivity Temperature Coefficient Range. The magnetic sensitivity temperature coefficient can be programmed within its limits of $TC_{Sens(max)}$ and $TC_{Sens(min)}$. Refer to the section on guaranteed quiescent voltage output range for a conceptual explanation.

Average Sensitivity Temperature Coefficient Step Size. Refer to the section on average quiescent voltage output step size for a conceptual explanation.

Sensitivity Temperature Coefficient Programming Resolution. Refer to the section on quiescent voltage output programming resolution for a conceptual explanation.

Sensitivity Drift Through Temperature Range. Second-order sensitivity temperature coefficient effects cause the magnetic sensitivity to drift from its ideal value over the operating ambient temperature, T_A. For purposes of specification, the sensitivity drift through temperature range, $\Delta Sens_{TC}$, is defined:

$$\Delta Sens_{TC} - \frac{Sens_{TA} - Sens_{IDEAL(TA)}}{Sens_{IDEAL(TA)}} \times 100\%$$

Sensitivity Drift Due to Package Hysteresis. Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during or after temperature cycling. This change in sensitivity follows a hysteresis curve. For purposes of specification, the sensitivity drift due to package hysteresis, $\Delta Sens_{PKG}$, is defined:

$$\Delta Sens_{PKG} = \left(\frac{Sens_{(25°C, 2)} - Sens_{(25°C, 1)}}{Sens_{(25°C, 1)}}\right) \times 100\%$$

where $Sens_{(25°C ,1)}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C ,2)}$ is the value of sensitivity at T_A = 25°C after temperature cycling T_A up to 85°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error. The A1369 is designed to provide linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally the sensitivity of a device is the same for both fields for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERR+}) and negative (Lin_{ERR-}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERR+} = \left(1 - \frac{Sens_{B++}}{Sens_{B+}}\right) \times 100\%$$

$$Lin_{ERR-} = \left(1 - \frac{Sens_{B--}}{Sens_{B-}}\right) \times 100\%$$

$$Lin_{ERR} = max(|Lin_{ERR+}|, |Lin_{ERR-}|)$$

where

$$Sens_{Bx} = \left(\frac{|V_{OUTBx} - V_{OUT(Q)}|}{D_x}\right)$$

and B++, B+, B--, and B- are positive and negative magnetic fields with respect to the quiescent voltage output such that |B++| > |B+| and |B--| > |B-|.

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The output voltage clamps, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, limit the operating magnetic range of the applied field in which the device provides a linear output. The maximum positive and negative applied magnetic fields in the operating range can be calculated:

$$|B_{MAX(+)}| - \frac{V_{CLP,HIGH} - V_{OUT(Q)}}{Sens}$$

$$|B_{MAX(-)}| - \frac{V_{OUT(Q)} - V_{CLP,LOW}}{Sens}$$

Symmetry Sensitivity Error. The magnetic sensitivity of a device is constant for any two applied magnetic fields of equal magnitude and opposite polarities.

Symmetry error, SymERR (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{(B+)}}{Sens_{(B-)}}\right) \times 100\%$$

where

$$Sens_{Bx} = \left(\frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x}\right)$$

and B+, B- are positive and negative magnetic fields such that |B+| = |B-|.

Ratiometry Error. The A1369 provides a ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, magnetic sensitivity, Sens, and clamp voltage, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, are proportional to the supply voltage, V_{CC}. When the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in quiescent voltage output, $Rat_{VOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUTO(VCC)} / V_{OUTO(5\ V)}}{V_{CC}/5\ V}\right) \times 100\%$$

The ratiometric error in magnetic sensitivity, Rat_{Sens} (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5\ V)}}{V_{CC}/5\ V}\right) \times 100\%$$

The ratiometric error in the clamp voltages, $Rat_{VOUTCLP}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{VOUTCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5\ V)}}{V_{CC}/5\ V}\right) \times 100\%$$

where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Undervoltage Lockout. The A1369 features an undervoltage lockout feature that ensures that the device will output a valid signal when V_{CC} is above certain threshold V_{UVLOHI}, and remains valid until V_{CC} falls below a lower threshold, $V_{UVLOLOW}$. The undervoltage lockout feature provides a hysteresis of operation to eliminate indeterminate output states.

The output of the A1369 is held low (GND) until V_{CC} exceeds V_{UVLOHI}. Once V_{CC} exceeds V_{UVLOHI}, the device powers up, and the output will provide a ratiometric output voltage proportional to the input magnetic signal, and V_{CC}. If V_{CC} should drop back down below $V_{UVLOLOW}$ for more than t_{uvlo} after the device is powered up, the output will be pulled low.

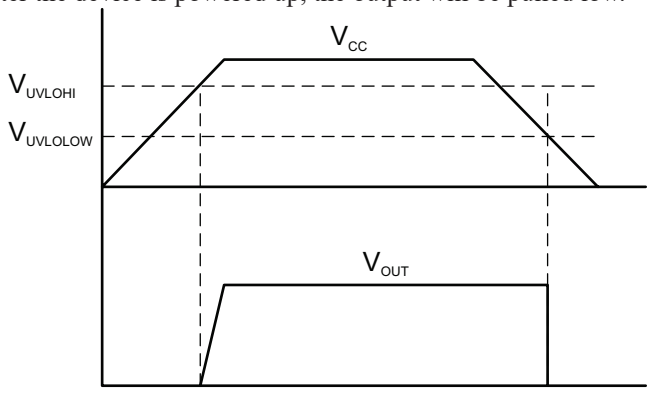

Figure 4: UVLO Operation

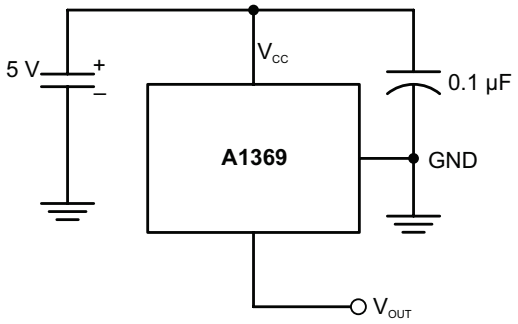

Figure 5: Typical Application Circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small-signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic-field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic-field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal- and stress-related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

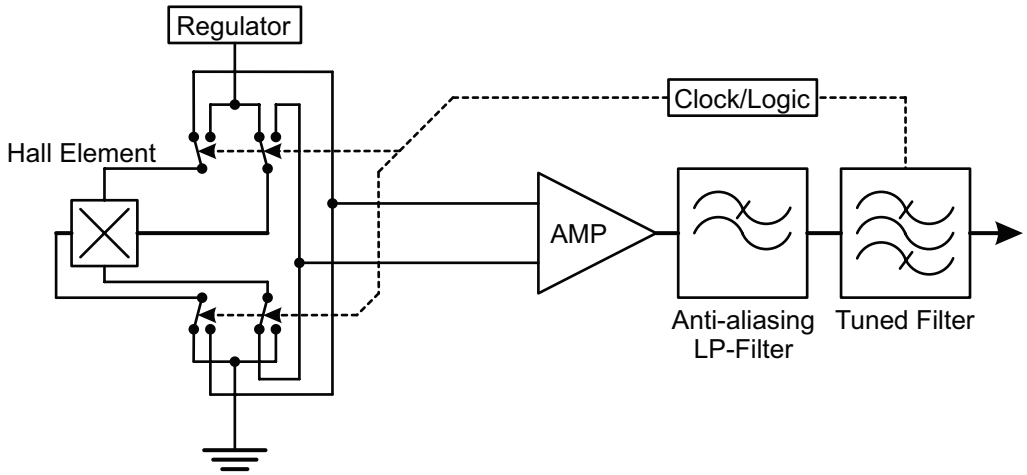

Figure 6: Concept of Chopper Stabilization Technique

PROGRAMMING GUIDELINES

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VOUT pin of the device. A unique combination of different voltage-level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as high (V_{PH}), mid (V_{PM}), and low (V_{PL}).

The A1369 features a Try mode, Blow mode, and Read mode:

- In Try mode, the value of multiple programmable parameters may be set and measured simultaneously. The parameter values are stored temporarily, and reset after cycling the supply voltage.
- In Blow mode, the value of a single programmable parameter may be permanently set by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially. This mode is used for blowing the device-level fuse, which permanently blocks the further programming of all parameters. Device locking is also accomplished in this mode.
- In Read mode, the current state of the programming fuses can be read back for verification of programmed value.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor Evaluation Kit—contact your local sales rep listed on the Allegro website (www.allegromicro.com) for details.

Definition of Terms

Register. The section of the programming logic that controls the choice of programmable modes and parameters.

Bit Field. The internal fuses unique to each register, represented as a binary number. Incrementing the bit field of a particular register causes its programmable parameter to change based on the internal programming logic.

Key. A series of mid-level voltage pulses used to select a register, with a value expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as key 1 or bit 0.

Code. The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

Addressing. Incrementing the bit field code of a selected register by serially applying a pulse train through the VOUT pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing. Applying a high-voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

Blow Pulse. A high-voltage pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply. Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Table 1: Programming Pulse Requirements

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
PROGRAMMING PROTOCOL (T_A = 25°C)						
Programming Voltage[16]	V_{PL}		4.5	–	5.5	V
	V_{PM}		12.5	13	13.5	V
	V_{PH}		18	18.5	19	V
Programming Current[17]	I_P	C_{BLOW} = 0.1 µF	200	–	–	mA
Pulse Width	t_{LOW}[18]		20	–	–	µs
	t_{ACTIVE}[19]		20	–	–	µs
	t_{BLOW}[20]		90	100	–	µs
Pulse Rise Time	t[21]		5	–	100	µs
Pulse Fall Time	t[22]		5	–	100	µs
Blow Pulse Slew Rate	SR_{BLOW}		0.375	–	–	V/µs

[16] Programming voltages are measured at the VOUT pin of the package.
[17] Minimum supply current available during programming to ensure proper fuse blowing.
[18] Duration of V_{PL} time between bits.
[19] V_{PL} and V_{PH} durations required during register selection and bit field addressing sequences.
[20] Pulse duration required to permanently blow a fuse.
[21] Rise time required for programming voltage transitions from V_{PL} to V_{PM} or V_{PL} to V_{PH}.
[22] Fall time required for programming voltage transitions from V_{PM} to V_{PL} or V_{PH} to V_{PL}.

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PROGRAMMING PROCEDURES

Mode/Parameter Selection

Each programmable mode/parameter can be accessed through a specific register. To select a register, a sequence of voltage pulses consisting of a V_{PH} pulse, a series of V_{PM} pulses, and a V_{PH} pulse (with no V_{CC} supply interruptions) must be applied serially to the VOUT pin. The number of V_{PM} pulses is called the key, and uniquely identifies each register. The pulse train used for selection of the first register, key 1, is shown in Figure 7.

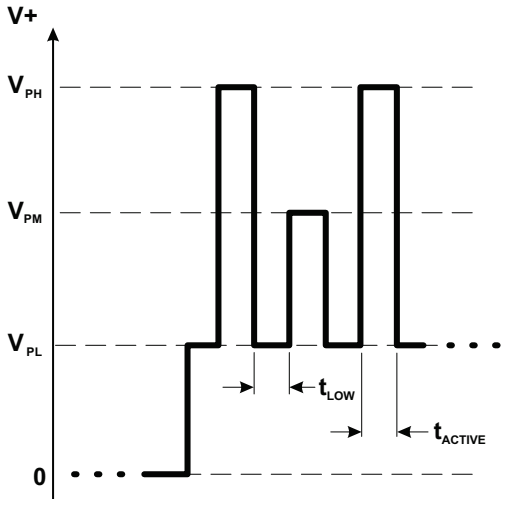

Figure 7: Parameter Selection Pulse Train

The A1369 has three registers that select among the three programmable modes:

- Register 1:
  - □ BLOW/LOCK
- Register 2:
  - □ TRY
- Register 3:
  - □ READ

And three registers that select among the seven programmable parameters:

- Register 1:
  - □ Sensitivity (SENS)
- Register 2:
  - □ Quiescent Voltage Output (QVO)
- Register 3:
  - □ Temperature Compensation at Factory
  - □ Accessible only in READ MODE
- Register 4:
  - □ Margin Low
  - □ Margin Comparator
  - □ Margin High
  - □ Overall Lock Bit
  - □ (LOCK)

Try Mode Bit Field Addressing

In Try mode, after a programmable parameter has been selected, a V_{PH} pulse transitions the programming logic into the bit field addressing state. A series of V_{PM} pulses to the VOUT pin of the device, as shown in Figure 8, increments the bit field of the selected parameter.

When addressing the bit field in Try mode, the number of V_{PM} pulses is represented by a decimal number called a code. Addressing activates the corresponding fuse locations in the given bit field by incrementing the binary value of an internal DAC. The value of the bit field (and code) increments by one with the falling edge of each V_{PM} pulse, up to the maximum possible code (see the Programming Logic table). As the value of the bit field code increases, the value of the programmable parameter changes. Measurements can be taken after each pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have unblown fuses to their initial states.

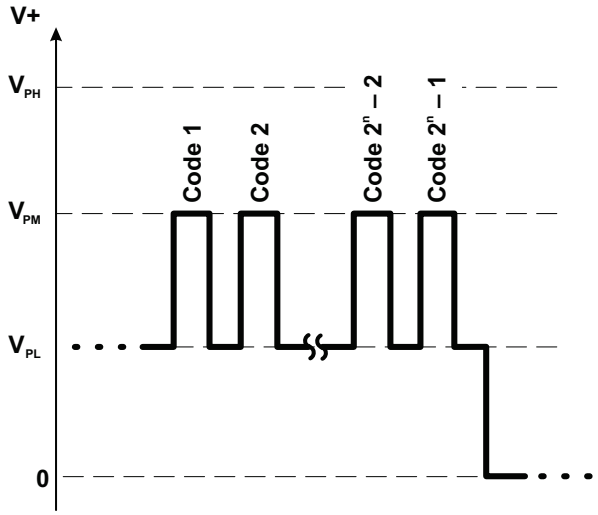

Figure 8: Try Mode Bit Field Addressing Pulse Train

Fuse Blowing

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by applying a V_{PH} pulse, called a blow pulse, of sufficient duration at the V_{PH} level to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. The A1369 has built in circuitry that will only allow one fuse to be blown at a time. During blow mode, the bit field can be considered a "one-shot" shift register. Table 2 illustrates how to relate the number of V_{PM} pulses to the binary and decimal value for Blow mode bit field addressing. It should be noted that the simple relationship between the number of V_{PM} pulses and the desired code is:

$$2^n = Code$$

where n is the number of V_{PM} pulses, and the bit field has an initial state of decimal code 1 (binary 000000001).

To correctly blow the desired fuses, the code representing the desired parameter value must be translated to a binary number. For example, as shown in Figure 9, decimal code 5 is equivalent to the binary number 101. Therefore, bit 2 must be addressed and blown, the device power supply cycled, and then bit 0 must be addressed and blown. An appropriate sequence for the blowing code 4 is shown in Figure 10. The order of blowing bits, however, is not important. Blowing bit 0 first and then bit 2 is acceptable.

Note:

After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

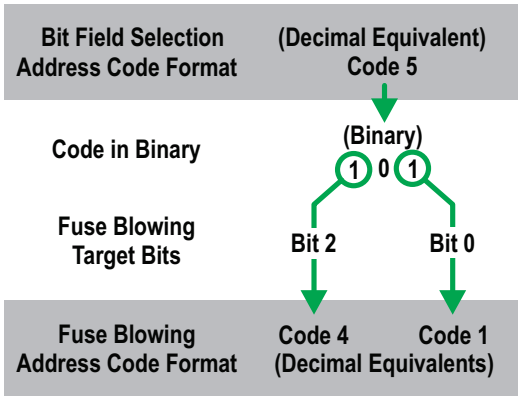

Figure 9: Example of Code 5 Broken into its Binary Components, which are Code 4 and Code 1

Table 2: Blow Mode Bit Field Addressing

# of V_{PM} Pulse (decimal)	Binary Register	Equivalent Code (2^n)
0	000000001	1
1	000000010	2
2	000000100	4
3	000001000	8
4	000010000	16
5	000100000	32
6	001000000	64
7	010000000	128
8	100000000	256

Locking the Device

After the desired code for each parameter is programmed, the device can be locked to prevent further programming of any parameters.

Additional Guidelines

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VOUT pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The C_{BLOW} blowing capacitor must be replaced in the final application with the load capacitor, C_L, for proper operation.
- The application capacitance, C_L, should be used when measuring the output duty cycle during programming. The blowing capacitor, C_{BLOW}, should be removed during measurement and should only be applied when blowing fuses.
- The power supply used for programming must be capable of delivering at least 18 V and 175 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.

The following programming order is required:

- Sens
- QVO
- LOCK (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

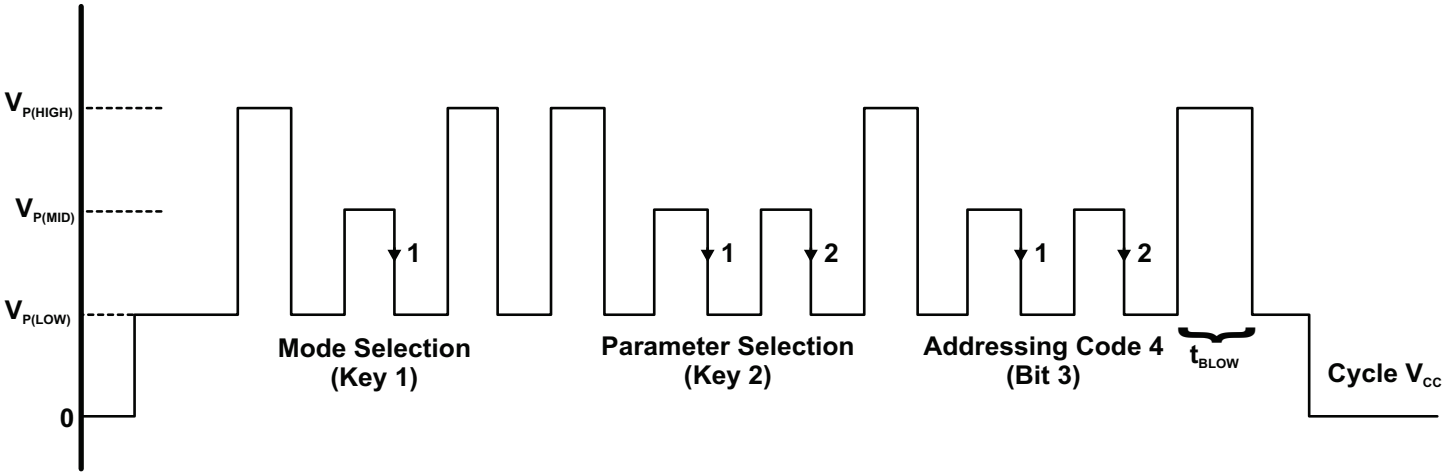

Figure 10: Example of Blow Mode Programming Pulses Applied to the VOUT Pin.

In this example, Sensitivity (Parameter Key 1) is addressed to blow bit 3.

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PROGRAMMING MODES

Try Mode

Try mode allows multiple programmable parameters to be tested simultaneously without permanently setting any values. In this mode, each high pulse will indefinitely loop the programming logic through the mode, register, and bit field states. There must be no interruptions in the V_{CC} supply.

After powering the V_{CC} supply, select mode key 1, the desired parameter register, and address its bit field. When addressing the bit field, each V_{PM} pulse increments the value of the parameter register up to the maximum possible code (see Programming Logic section). The addressed parameter value will be stored in the device even after the programming drive voltage is removed from the VOUT pin, allowing its value to be measured. To test an additional programmable parameter in conjunction with the original, enter an additional V_{PH} pulse on the VOUT pin to re-enter the parameter selection field. Select a different parameter register, and address its bit field without any supply interruptions. Both parameter values will be stored and can be measured after removing the programming drive voltage. Multiple programming combinations can be tested to achieve optimal application accuracy. See Figure 11 for an example of the Try mode pulse train.

Registers can be addressed and re-addressed an indefinite number of times in any order. Once the desired code is found for each register, cycle the supply and blow the bit field using Blow mode. Note that for accurate time measurements the blow capacitor, C_{BLOW}, should be removed during output voltage measurement.

Blow Mode

After the required value of the programmable parameter is found using Hold/Try mode, the corresponding code should be blown to make its value permanent. To do this, select the required parameter register, and address and blow each required bit separately (as described in the Fuse Blowing section). The supply must be cycled between blowing each bit of a given code. After a bit is blown, cycling the supply will not reset its value.

Read Mode

The state of the internal fuses can be read at any time in Read mode. Read mode is available before, and after locking the device. Read mode allows the programmer to verify that the intended bits were blown.

After powering the V_{CC} supply, select mode key 3, the desired parameter register, and address its bit field. Upon completing the selection of mode key 3, I_{CC} will increase by 250 µA to indicate the device is in Read Fuse mode. On the falling edge of the V_{PH} pulse that terminates the register selection, I_{CC} will increase by another 250 µA (total of 500 µA above normal I_{CC}) to indicate a fuse is blown, or decrease by 250 µA (total of 0 µA above nominal I_{CC}) to indicate an unblown fuse. On each consecutive falling edge of V_{PM} pulses the A1369 will modify I_{CC} to indicate the state of each fuse (500 µA above I_{CC} for a blown fuse, and 0 µA above I_{CC} for an unblown fuse).

The Read mode indicates the fuse values of the selected register in a serial fashion where one bit is read at a time. The LSB (B0) is selected on the falling edge of the V_{PH} pulse that terminates the key parameter selection, and begins the addressing code. The successive V_{PM} pulses select the succeeding bits in this order: B1, B2, B3, B4, B5, B6, B7, B8. See Figure 12 for an example pulse train.

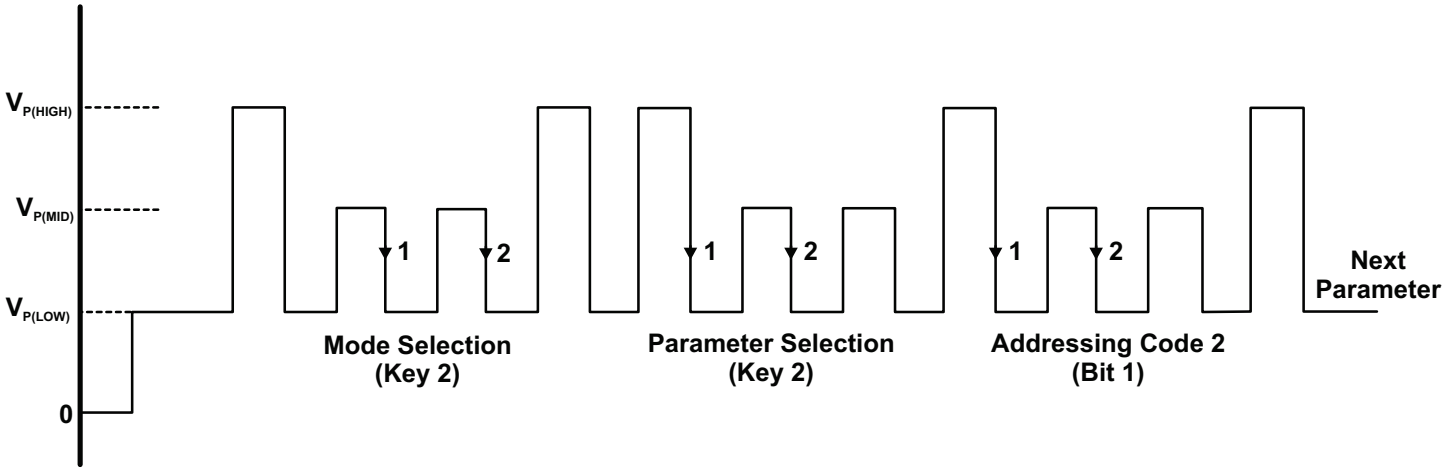

Figure 11: Example of Try Mode Programming Pulses Applied to the VOUT Pin.

In this example, Sensitivity (Parameter Key 1) is addressed to code 3 and QVO (Parameter Key 2) is addressed to code 2.

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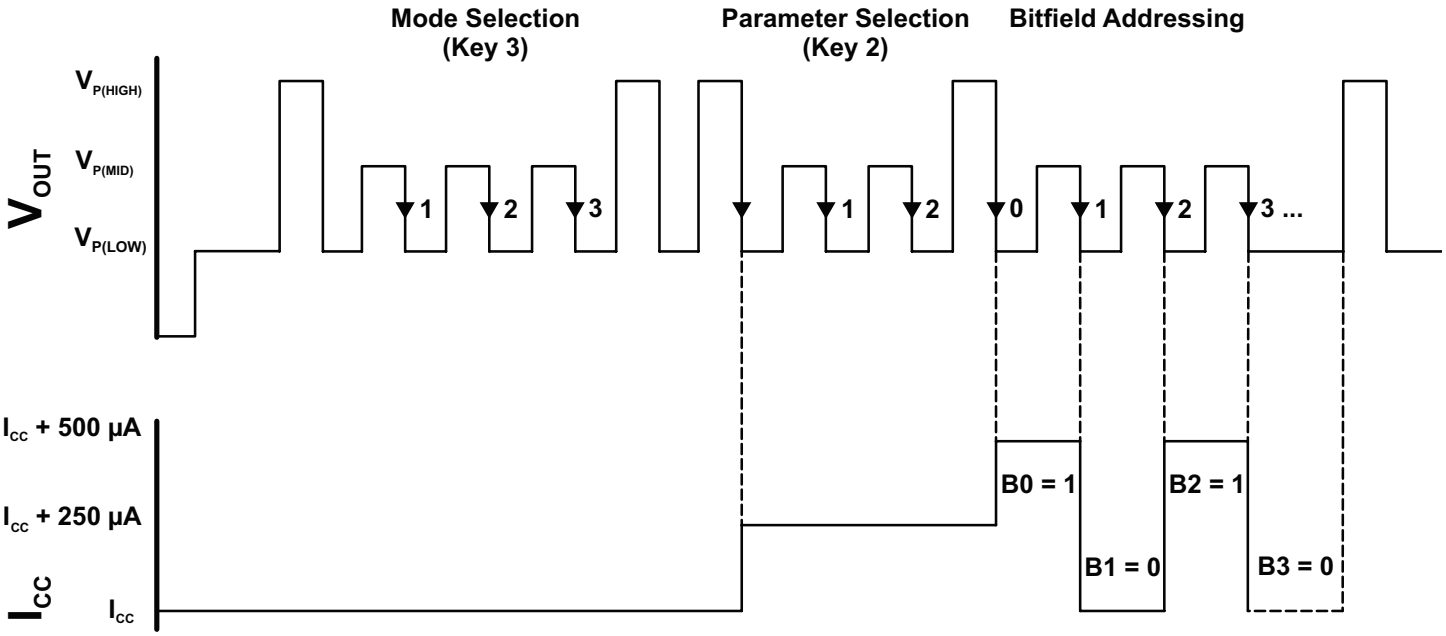

Figure 12: Example of Read Mode Programming Pulses Applied to the VOUT Pin and Device Response in I_{CC}.

PROGRAMMING STATE MACHINE

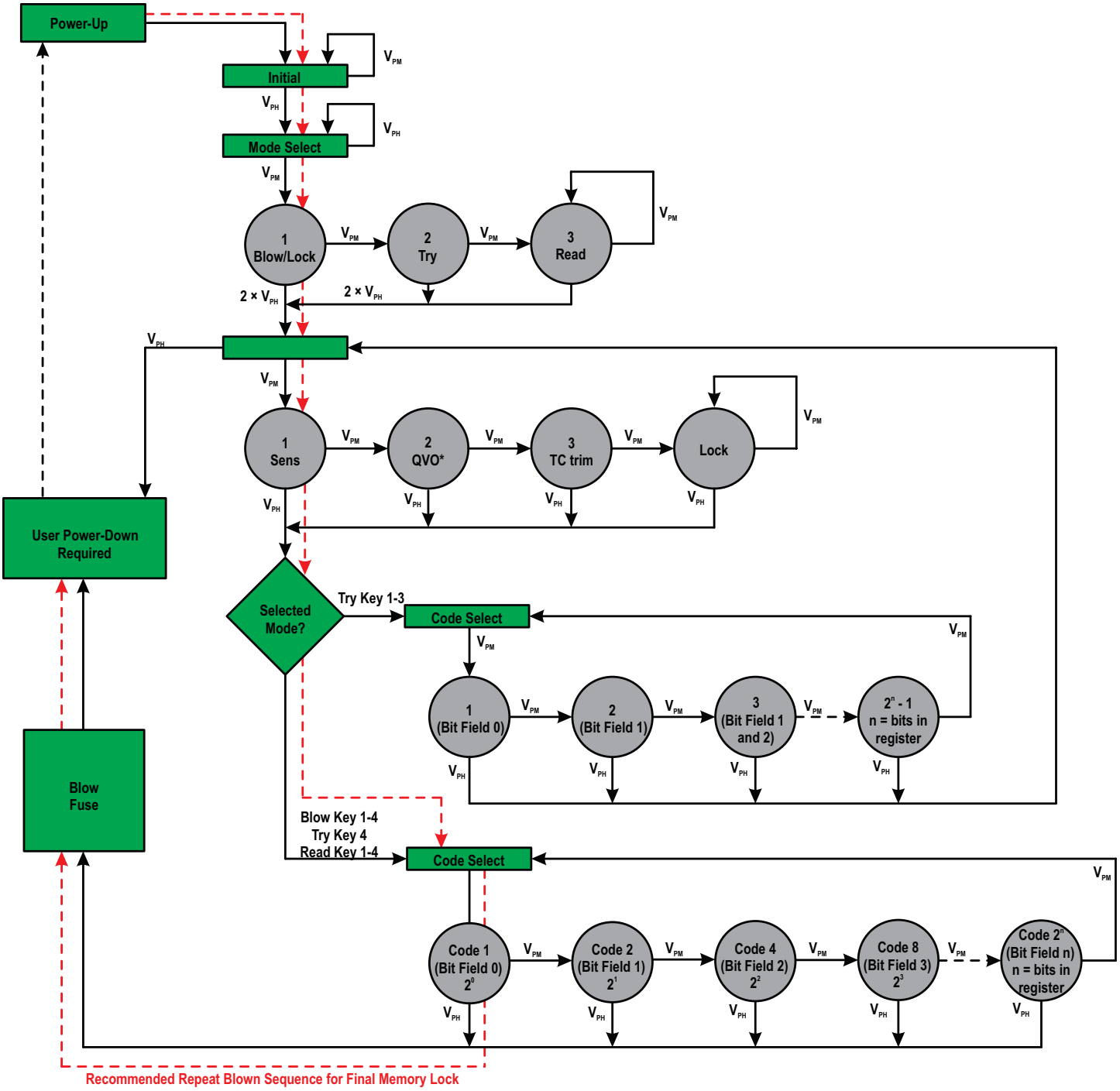

Figure 13: Programming State Machine

* QVO parameter needs to be programmed last; otherwise, next high pulse will lead to unwanted output polarity change.

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Initial State

After system power-up, the programming logic is reset to a known state. This is referred to as the Initial state. All the bit field locations that have intact fuses are set to logic 0. While in the Initial state, any V_{PM} pulses on the VOUT pin are ignored. To enter the Mode Selection state, apply a single V_{PH} pulse on VOUT pin.

Mode Selection State

This state allows the selection of the mode register containing the parameter to be programmed. To select a mode register, increment through the keys by sending V_{PM} pulses on the VOUT pin. Register keys select among the following programmable modes:

- 1 pulses –Blow/Lock
- 2 pulses – Try
- 3 pulses – Read

To enter the Parameter Selection state, apply 2 V_{PH} pulses on VOUT pin.

Parameter Selection State

This state allows the selection of the parameter register containing the bit fields to be programmed.

Applying a V_{PM} pulse to the VOUT pin will increment through the parameter registers.

- 1 pulse – Sensitivity
- 2 pulses – QVO, Polarity
- 3 pulses – Factory use only
- 4 pulses – Margin Low, Margin comp, margin high, Lock All

To enter the Bit Field Addressing state, send one V_{PH} pulse on the VOUT pin.

Bit Field Addressing State

This state allows the selection of the individual bit fields to be programmed in the selected parameter register (see Programming Logic table). Applying V_{PM} pulses to the VOUT pin increments the bitfield.

In Try mode, to re-enter the Parameter Selection state send one V_{PH} pulse on the VOUT pin. The previously addressed parameter will retain its value as long as V_{CC} is not cycled.

In Blow/Lock mode, to leave the Bit Field Addressing state requires either cycling device power or blowing the fuses for the selected code. Note that merely addressing the bit field does not permanently set the value of the selected programming parameter; fuses must be blown to do so. In Blow mode, only one bit is active at a time.

Fuse Blowing State

To blow an addressed bit field, apply a V_{PH} pulse on the VOUT pin. Power to the device should then be cycled before additional programming is attempted.

Note:
Each bit representing a decimal code must be blown individually (see the Fuse Blowing section).

Final memory lock will be executed in two steps:

1. Blowing the “Lock All” bit
2. Repeating the programming blow sequence for any bit of choice. This sequence will not blow that bit; rather, it will blow the final memory fuse.

Table 3: Programming Logic [23]

Programmable Mode (Register Key)	Bitfield Address		Description
	Binary Format [MSB → LSB]	Decimal Equivalent Code	
Blow/Lock (1)	01	1	Blow
			Lock
Try (2)	10	2	Try
Read (3)	11	3	Read

Registry Selection Key	Binary Bitfield Address [MSB → LSB]	Decimal Equivalent Code	Description
Sensitivity (1)	0000000	0	Initial value; Sens = $Sens_{PRE}$
	0111111	63	Maximum Sensitivity
	1111111	127	Minimum Sensitivity value in range
QVO, Clamp Disable (2)	0000000	0	Initial value
	0001111	15	Maximum QVO
	0010000	16	Minimum QVO
	0100000	32	Disable Output Clamp
Reserved (3)	0000000	0	For factory use only. Programming:Sens coarse, Sensitivity TC and QVO TC
Fuse Margin Lock (4)	000000001	1	Margin 10k
	000000010	2	Margin comparator
	000000100	4	Margin 150k
	100000000	256	Lock Device

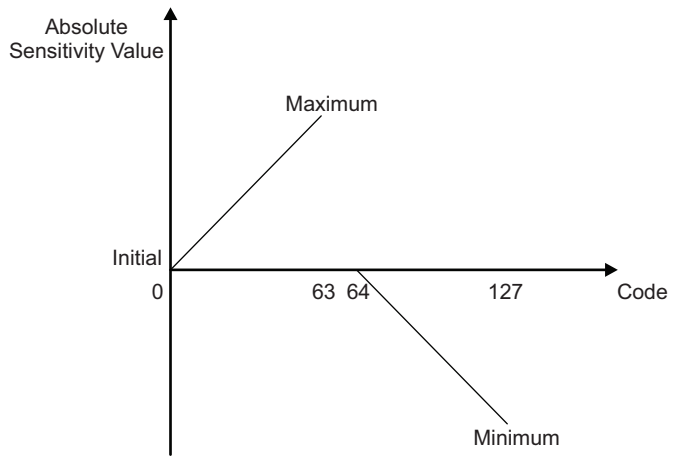

Figure 14: Sensitivity (1) Register

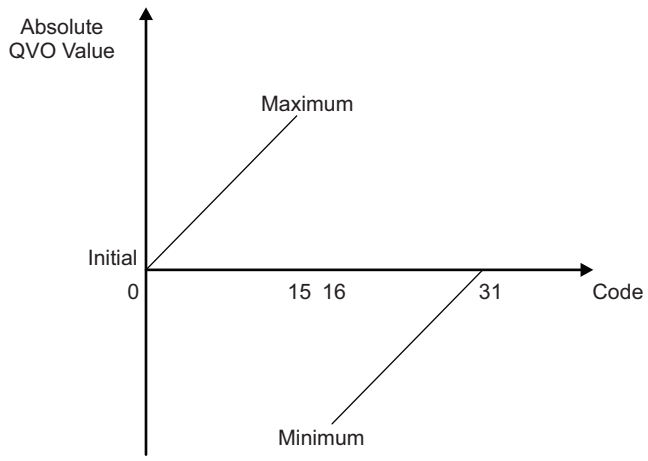

Figure 15: QVO (2) Register

[23] Programming is accomplished through the VOUT pin.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-9065)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

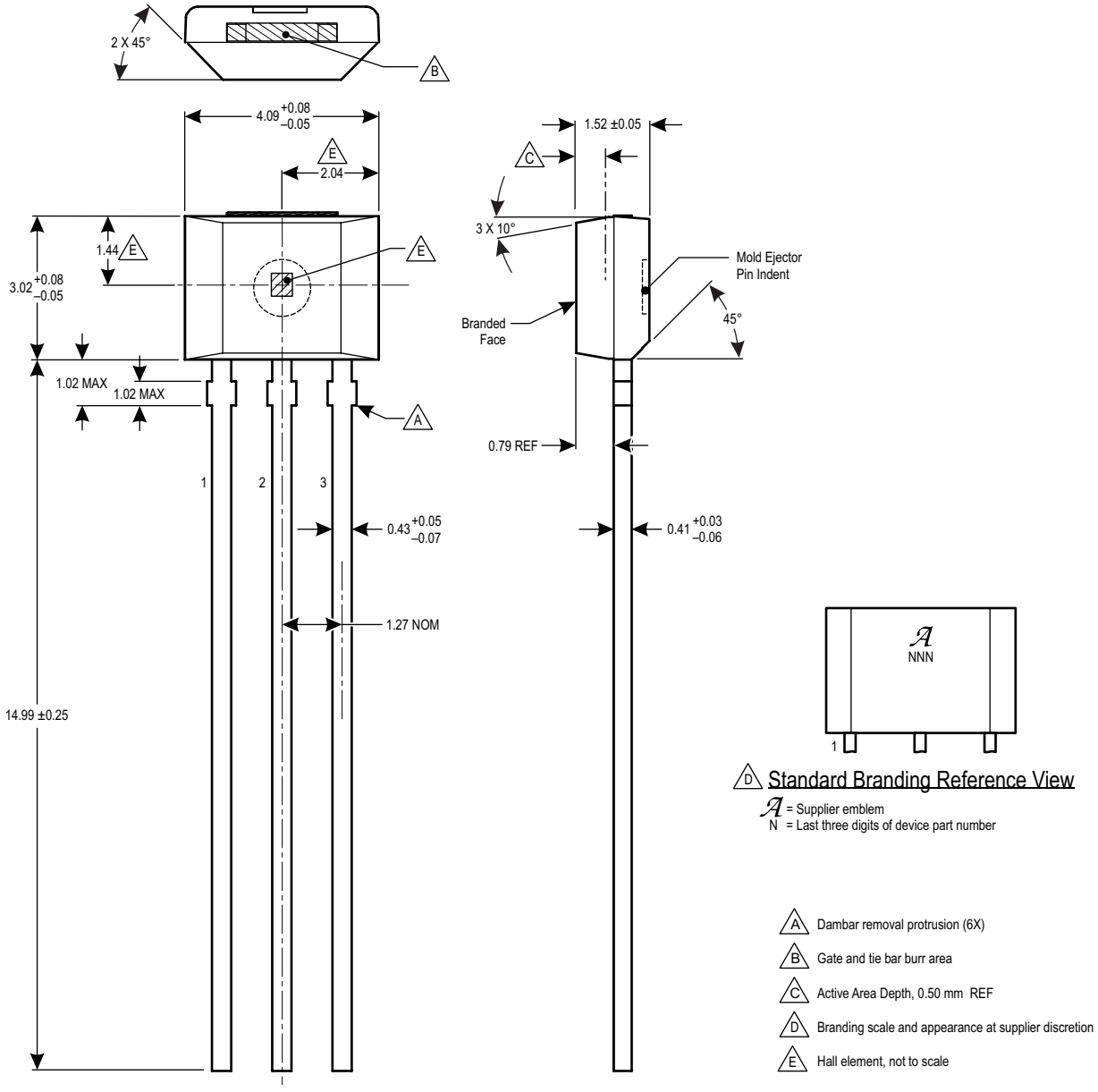

Figure 16: Package UA, 3-Pin SIP

Revision History

Number	Date	Description
–	November 18, 2014	Initial release.
1	April 8, 2015	Updated Programming Logic table; added Figures 14 and 15.
2	April 13, 2016	Corrected Absolute Maximum Characteristics table (page 3), Addressing section (page 11), and Table 1 (page 12); other miscellaneous editorial updates.
3	November 17, 2016	Updated Description (page 1), Selection Guide (page 2), and Figure 12 (page 17).
4	January 26, 2018	Removed duplicate default Sensitivity from electrical characteristic tables (page 5).
5	July 2, 2018	Updated product status to “Not for New Design”

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