



BUK9E1R9-40E

N-channel 40 V, 1.9 mΩ logic level MOSFET in I²PAK

5 June 2013

Product data sheet

1. General description

Logic level N-channel MOSFET in a I²PAK package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Power Steering
- Fan Control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2		-	-	349	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	1.6	1.93	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; Fig. 13 ; Fig. 14		-	40.9	-	nC

[1] Continuous current is limited by package.

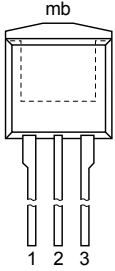


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 I2PAK (SOT226)	 mbb076
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9E1R9-40E	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9E1R9-40E	BUK9E1R9-40E

8. Limiting values

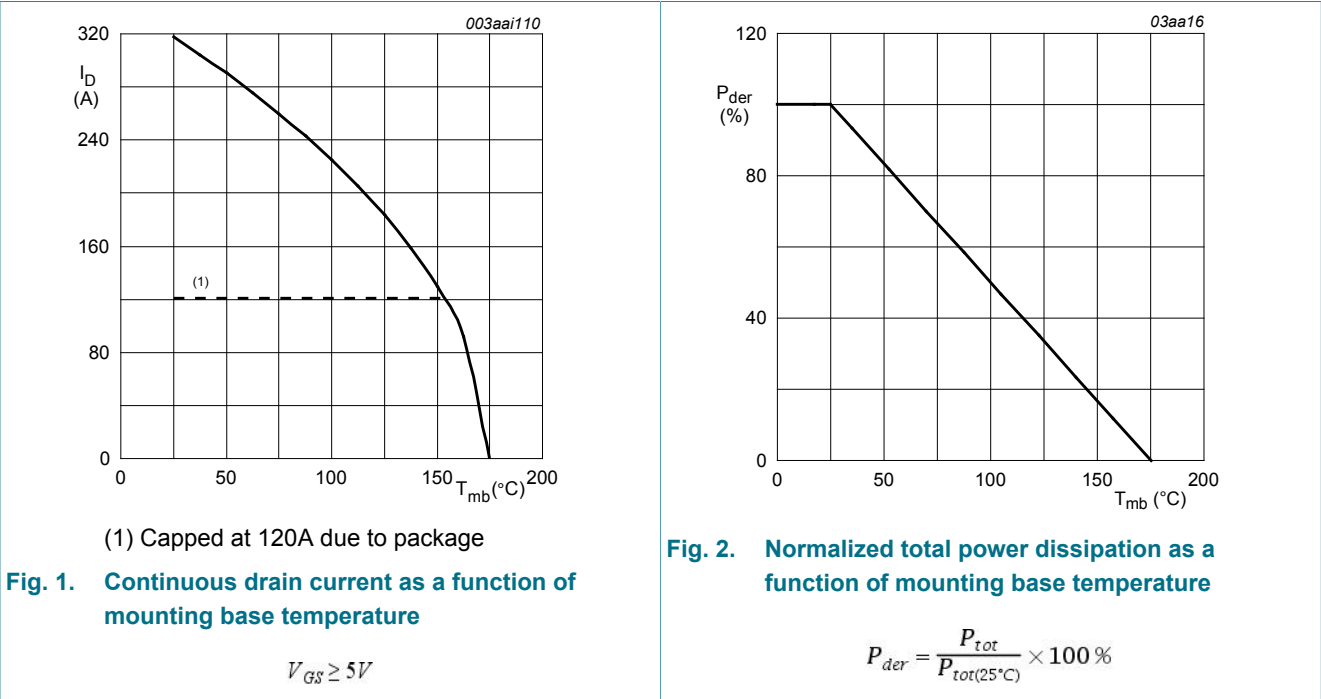
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; Pulsed	[1][2]	-15	15	V
		$T_j \leq 175\text{ °C}$; DC		-10	10	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[3]	-	120	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[3]	-	120	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4		-	1228	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2		-	349	W

Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[3]	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1228	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 120 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 3	[4][5]	-	1008	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}
- [3] Continuous current is limited by package.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



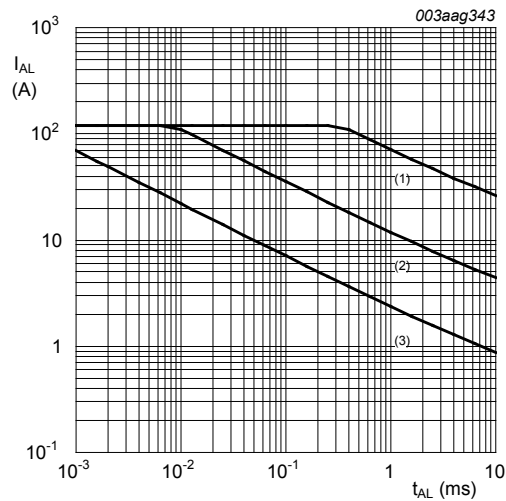


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25^{\circ}C$; (2) $T_{j\ (init)} = 150^{\circ}C$; (3) Repetitive Avalanche

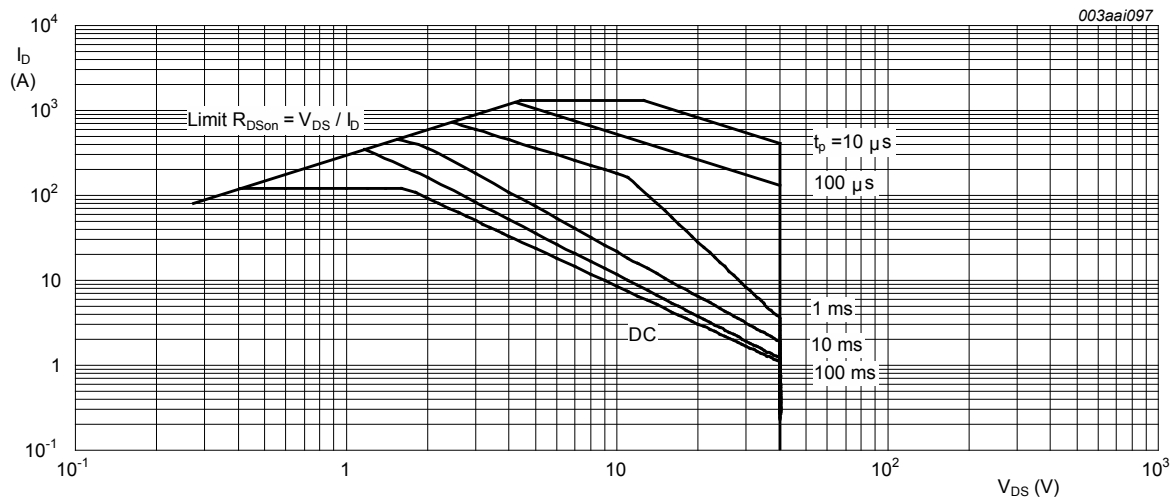


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.43	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	65	-	K/W

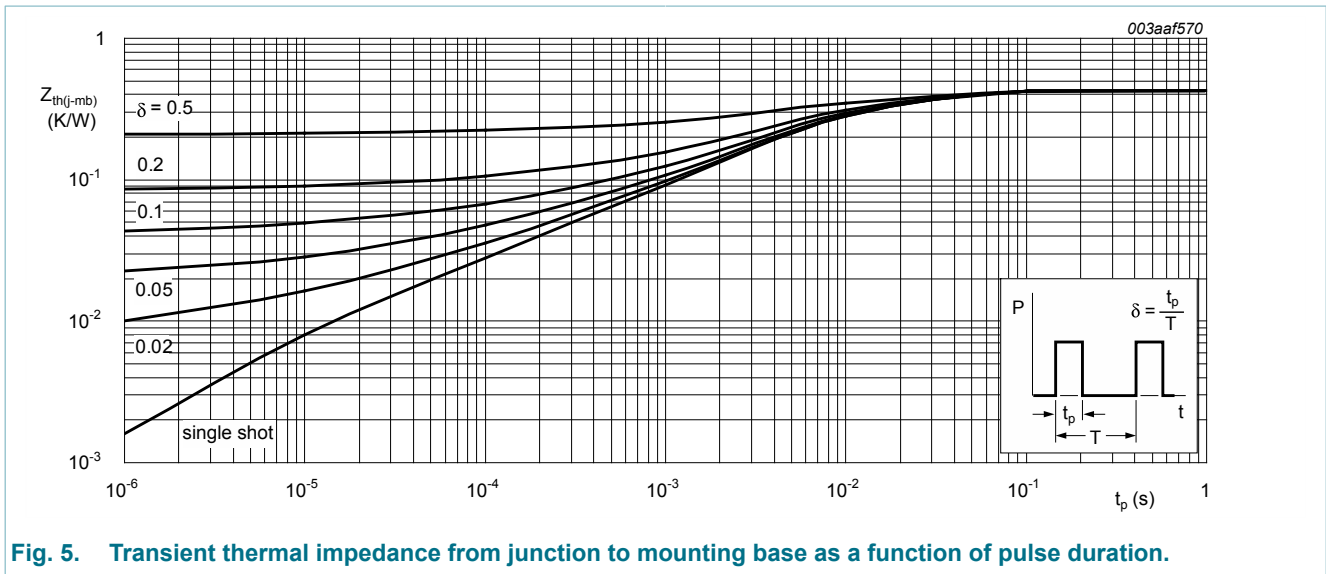


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		40	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ }^\circ\text{C}$		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55\text{ }^\circ\text{C}$; Fig. 9		-	-	2.45	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 175\text{ }^\circ\text{C}$; Fig. 9		0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	0.13	1	μA
		$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ }^\circ\text{C}$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11		-	1.6	1.93	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11		-	1.4	1.7	m Ω
		$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175\text{ }^\circ\text{C}$; Fig. 12 ; Fig. 11		-	-	3.7	m Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 5\text{ V}$; Fig. 13 ; Fig. 14		-	120	-	nC
Q_{GS}	gate-source charge			-	26.9	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GD}	gate-drain charge			-	40.9	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^{\circ}\text{C};$ Fig. 15		-	12300	16400	pF
C_{oss}	output capacitance			-	1530	1840	pF
C_{rss}	reverse transfer capacitance			-	740	1020	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega; V_{GS} = 5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$		-	95	-	ns
t_r	rise time			-	118	-	ns
$t_{d(off)}$	turn-off delay time			-	195	-	ns
t_f	fall time			-	119	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
		from drain lead 6mm from package to centre of die		-	4.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C};$ Fig. 16		-	0.77	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 25\text{ V}$		-	57	-	ns
Q_r	recovered charge			-	97	-	nC

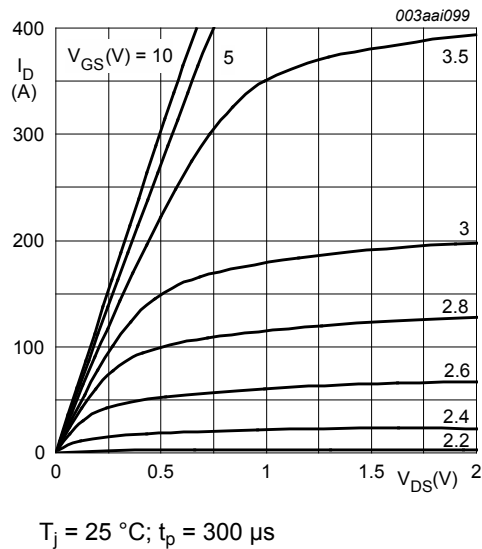


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

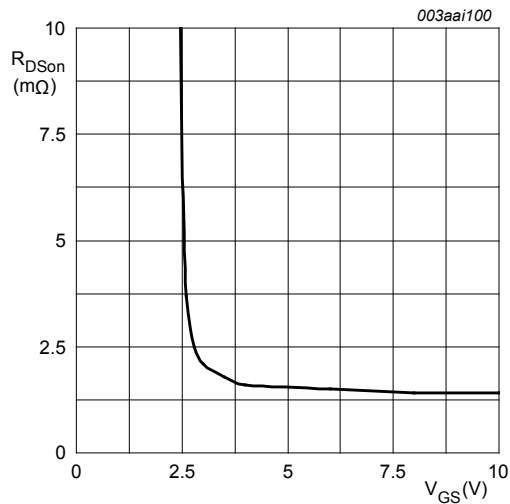


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

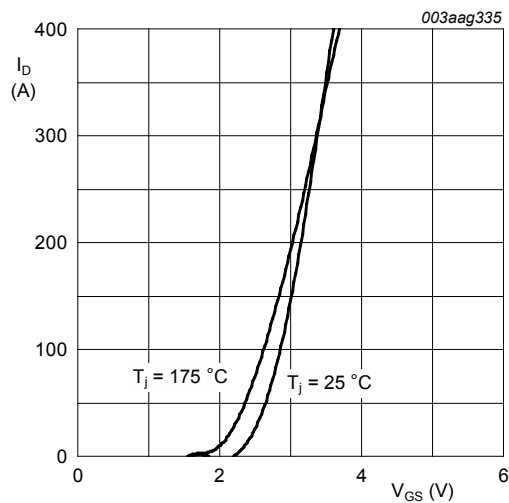


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 12\text{ V}$

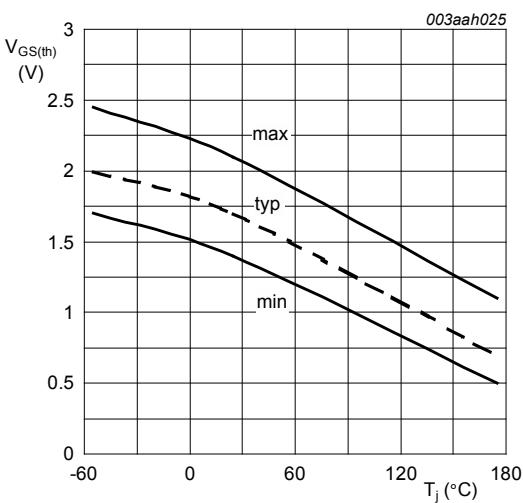


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

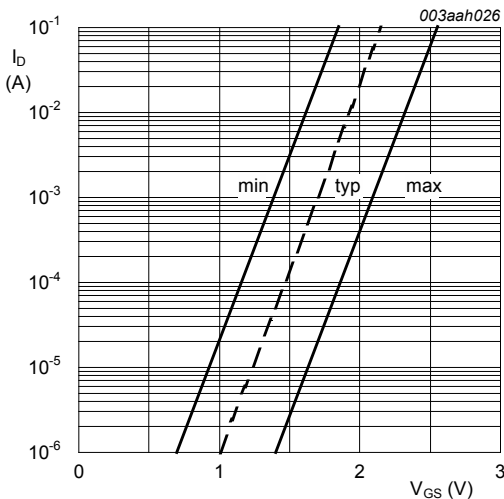


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

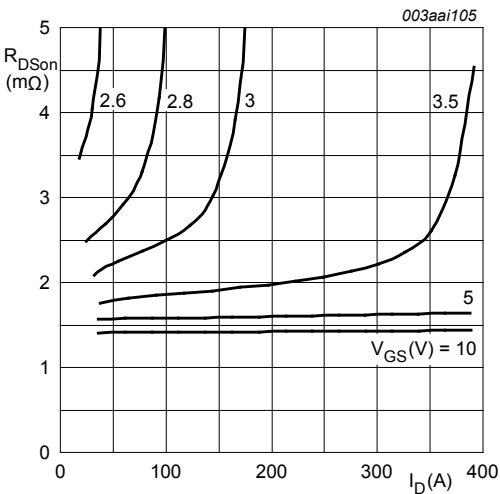


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$

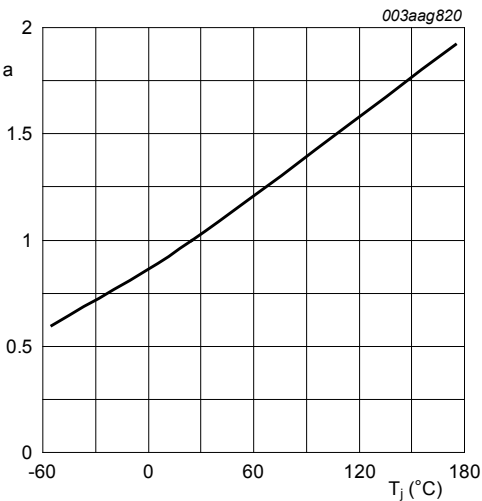


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^{\circ}\text{C})}}$$

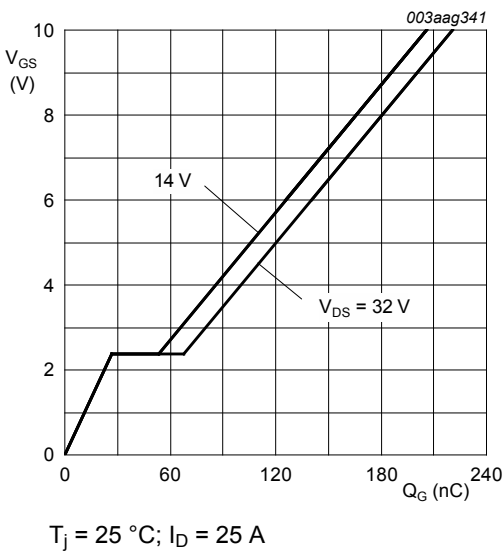


Fig. 14. Gate-source voltage as a function of gate charge; typical values

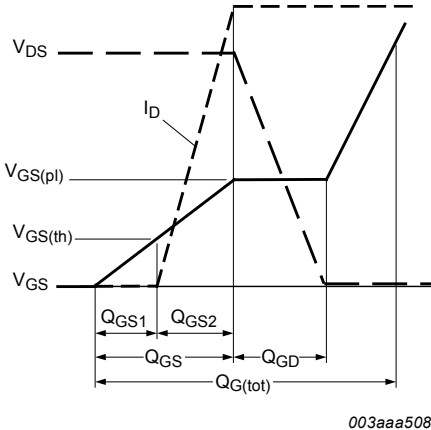


Fig. 13. Gate charge waveform definitions

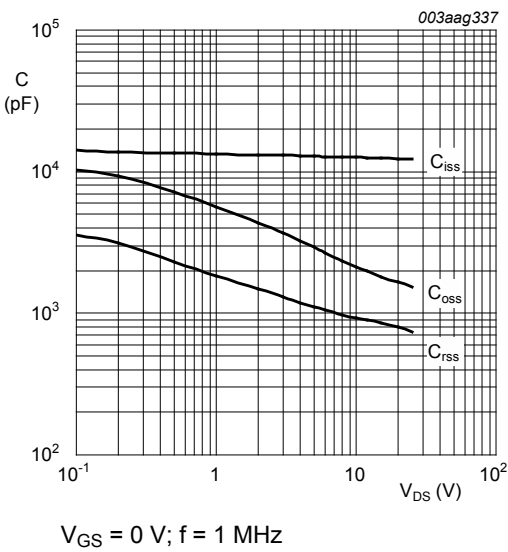
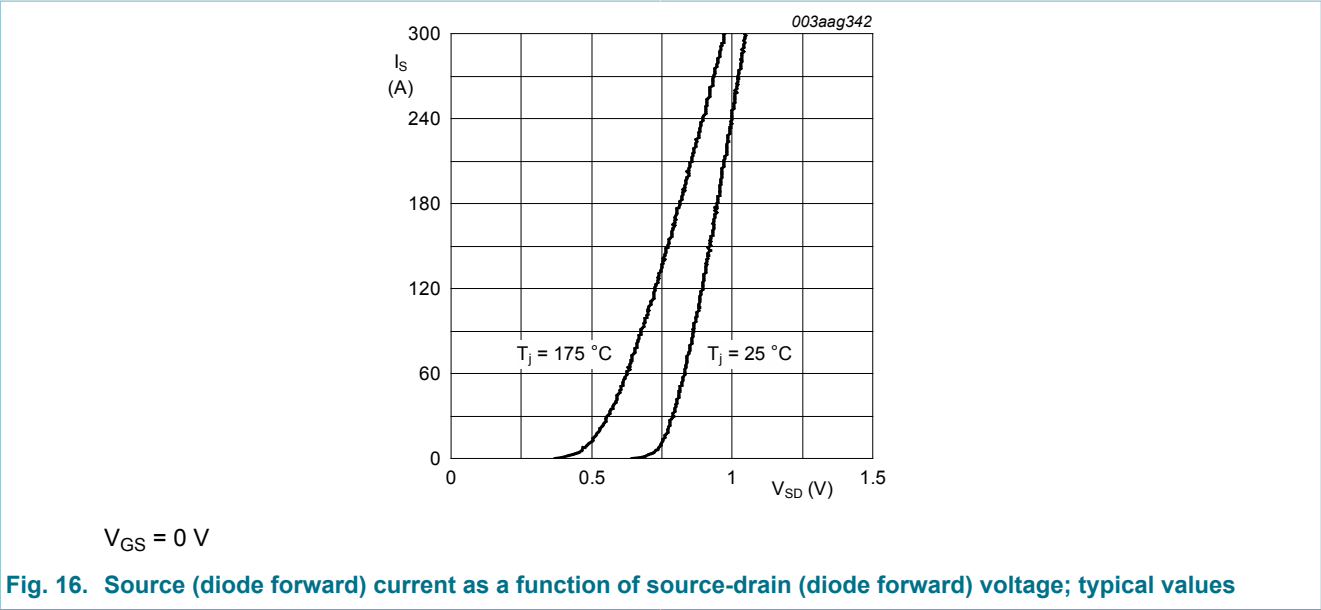


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



11. Package outline

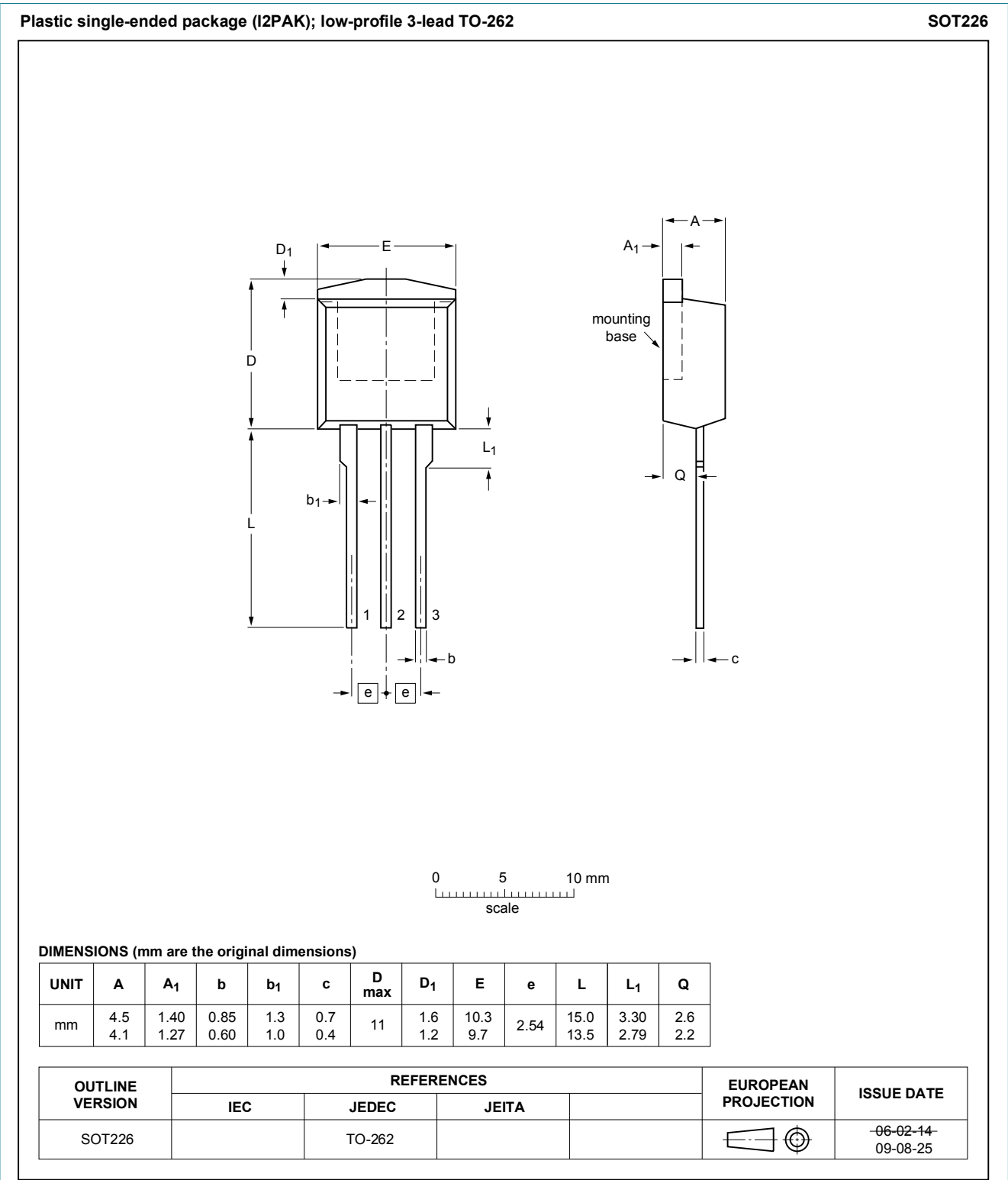


Fig. 17. Package outline I²PAK (SOT226)

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Document status [1][2]	Product status [3]	Definition
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Date of release: 5 June 2013