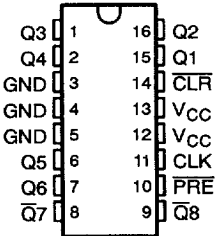


- Replaces SN74AS303
- Maximum Output Skew Between Same Phase Outputs of 1 ns
- Maximum Pulse Skew of 1 ns
- TTL-Compatible Inputs and Outputs
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include Plastic Small-Outline Package (D) and Standard Plastic 300-mil DIPs (N)

D OR N PACKAGE
(TOP VIEW)



description

The CDC303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. Preset (PRE) and clear (CLR) inputs are provided to set the Q and \bar{Q} outputs high or low independent of the clock (CLK) input.

The CDC303 has output and pulse-skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

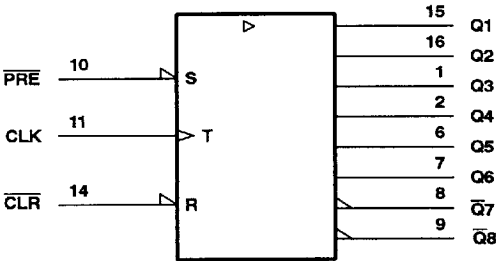
The CDC303 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
CLR	PRE	CLK	Q1–Q6	$\bar{Q}7$ – $\bar{Q}8$
L	H	X	L	H
H	L	X	H	L
L	L	X	L†	L†
H	H	↑	\bar{Q}_0	Q ₀
H	H	L	Q ₀	\bar{Q}_0

† This configuration will not persist when PRE or CLR returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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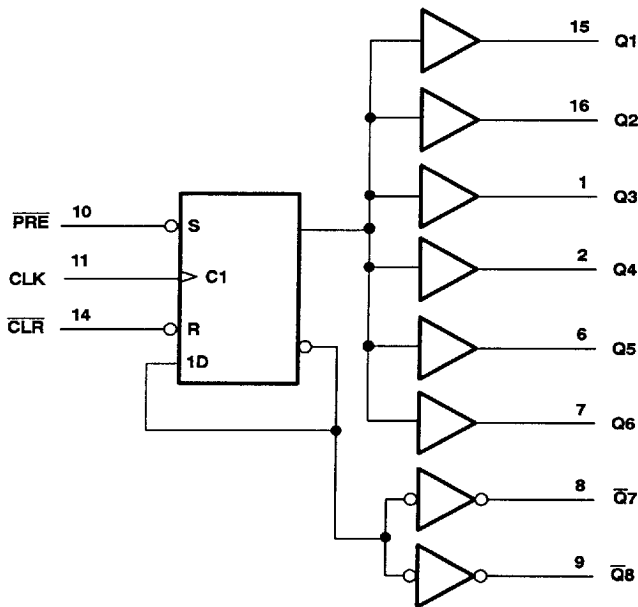
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CDC303
OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

SCAS323 – JULY 1990 – REVISED MARCH 1994

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current			–24	mA
I _{OL}	Low-level output current			48	mA
f _{clock}	Input clock frequency			80	MHz
T _A	Operating free-air temperature	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$,	$I_{OH} = -2 \text{ mA}$	$V_{CC}-2$			V
	$V_{CC} = 4.5 \text{ V}$,	$I_{OH} = -24 \text{ mA}$	2	2.8		
V_{OL}	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 48 \text{ mA}$		0.3	0.5	V
I_I	$V_{CC} = 5.5 \text{ V}$,	$V_I = 7 \text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.4 \text{ V}$			-0.5	mA
I_O^\ddagger	$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.25 \text{ V}$	-50		-150	mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$,	See Note 1		40	70	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with CLK and PRE grounded, then with CLK and CLR grounded.

timing requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	80	MHz
t_w	Pulse duration	CLR or PRE low	5	ns
		CLK high	4	
		CLK low	6	
t_{su}	Setup time before CLK†	CLR or PRE inactive	6	ns

switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}^\S				80		MHz
t_{PLH}	CLK	Q, \bar{Q}	$R_L = 500 \Omega$, $C_L = 50 \text{ pF}$	2	9	ns
t_{PHL}				2	9	
t_{PLH}	PRE or CLR	Q, \bar{Q}	$R_L = 500 \Omega$, $C_L = 50 \text{ pF}$	3	12	ns
t_{PHL}				3	12	
$t_{sk(o)}$	CLK	Q	$R_L = 500 \Omega$, $C_L = 10 \text{ pF to } 30 \text{ pF}$, See Figure 2		1	ns
		\bar{Q}			1	
		Q, \bar{Q}			2	
$t_{sk(p)}$	CLK	Q, \bar{Q}	$R_L = 500 \Omega$, $C_L = 10 \text{ pF to } 30 \text{ pF}$		1	ns
t_r					4.5	ns
t_f					3.5	ns

§ f_{max} minimum values are at $C_L = 0 \text{ to } 30 \text{ pF}$.



**TEXAS
INSTRUMENTS**

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From Output Under Test

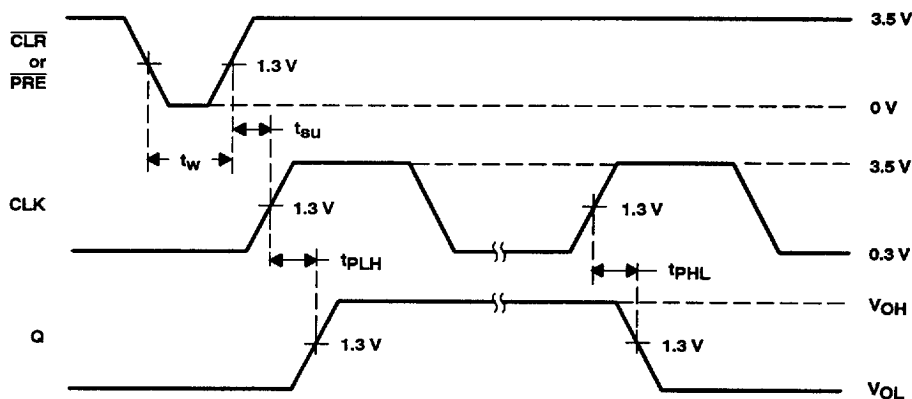
Test Point

C_L
(see Note A)

R_L

The diagram shows a horizontal line representing a circuit trace. On the left side, the text 'From Output Under Test' is written. On the right side, the text 'Test Point' is written. Below the line, there are two components connected to ground. The first component is a capacitor, represented by two parallel lines of unequal length, with the label C_L below it and '(see Note A)' below that. The second component is a resistor, represented by a zigzag line, with the label R_L below it.

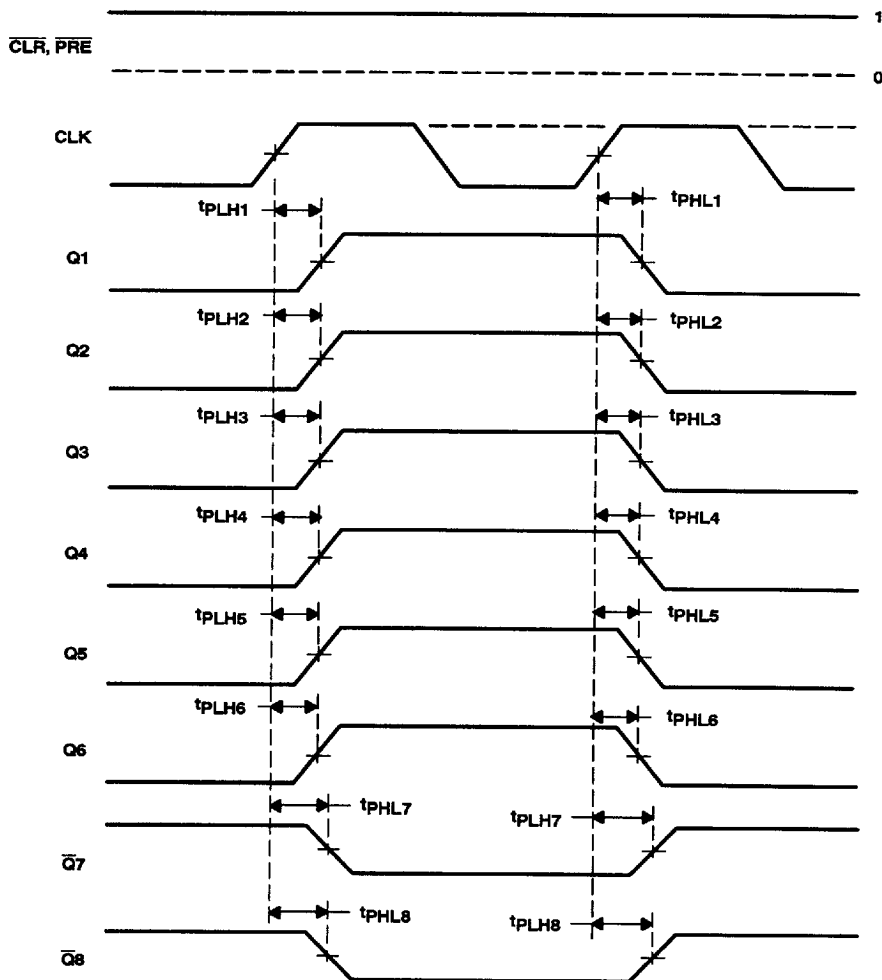
LOAD CIRCUIT



B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $t_r = 2.5$ ns, $t_f = 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. $t_{sk(o)}$, CLK to Q, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4, 5, 6$)
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3, 4, 5, 6$)
- B. $t_{sk(o)}$, CLK to \bar{Q} , is calculated as the greater of: $|t_{PLH7} - t_{PLH8}|$ and $|t_{PHL7} - t_{PHL8}|$.
- C. $t_{sk(o)}$, CLK to Q and \bar{Q} , is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4, 5, 6$), t_{PHL7} , and t_{PHL8}
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3, 4, 5, 6$), t_{PLH7} , and t_{PLH8}
- D. $t_{sk(p)}$ is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ ($n = 1, 2, 3, \dots, 8$).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$



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