1M x 16 Static RAM

Features

- **High speed**
  - **—t_{AA} = 8, 10, 12 ns**
- **Low active power**
  - **—1080 mW (max.)**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$ and CE_2 features**

Functional Description

The CY7C1061AV33 is a high-performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

Writing to the device is accomplished by enabling the chip ($\overline{CE}_1$ LOW and CE_2 HIGH) while forcing the Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A$_0$ through A$_{19}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A$_0$ through A$_{19}$).

Reading from the device is accomplished by enabling the chip by taking $\overline{CE}_1$ LOW and CE_2 HIGH while forcing the Output Enable ($\overline{OE}$) LOW and the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the truth table at the back of this data sheet for a complete description of Read and Write modes.
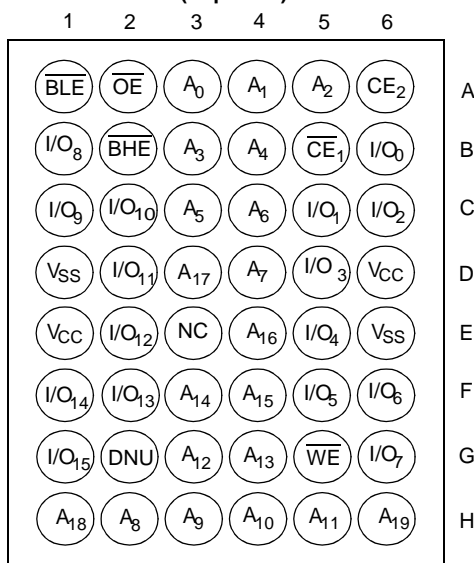
The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH/CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1061AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-ball fine-pitch ball grid array (FBGA) package.

Logic Block Diagram

Pin Configuration

TSOP II (Top View)
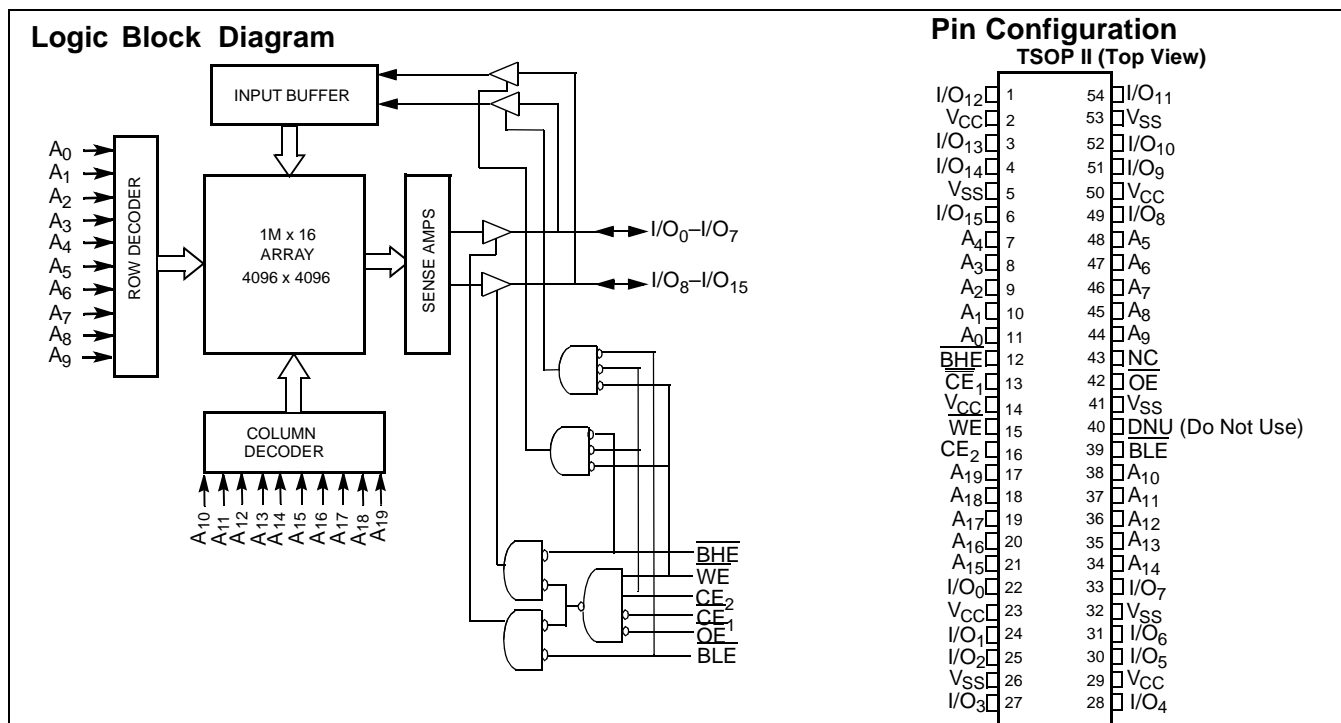
Selection Guide

		-8	-10	-12	Unit
Maximum Access Time		8	10	12	ns
Maximum Operating Current	Commercial	300	275	260	mA
	Industrial	300	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	50	mA

Pin Configurations

48-ball FBGA

(Top View)

	1	2	3	4	5	6	
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2	A
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE_1}$	I/O_0	B
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2	C
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}	D
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}	E
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6	F
G	I/O_{15}	DNU	A_{12}	A_{13}	$\overline{WE}$	I/O_7	G
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{19}	H

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied...−55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... −0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[1] ....−0.5V to V_{CC} + 0.5V

DC Input Voltage[1] .... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW).. 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	−40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		−1	+1	−1	+1	−1	+1	μA
I_{OZ}	Output Leakage Current	GND $\leq V_{OUT} \leq V_{CC}$, Output Disabled		−1	+1	−1	+1	−1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Commercial		300		275		260	mA
			Industrial		300		275		260	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	$CE_2 <= V_{IL}$ Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}			70		70		70	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	$CE_2 <= 0.3V$ Max. V_{CC}, $\overline{CE} \geq V_{CC} − 0.3V$, $V_{IN} \geq V_{CC} − 0.3V$, or $V_{IN} \leq 0.3V$, f = 0	Commercial/ Industrial		50		50		50	mA

Capacitance[2]

Parameter	Package	Description	Test Conditions	Max.	Unit
C_{IN}	Z54	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	pF
	BA48			8	pF
C_{OUT}	Z54	I/O Capacitance		8	pF
	BA48			10	pF

Notes:
1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3]

(a) * Capacitive Load consists of all components of the test environment.

(b) INCLUDING JIG AND SCOPE

(c) ALL INPUT PULSES
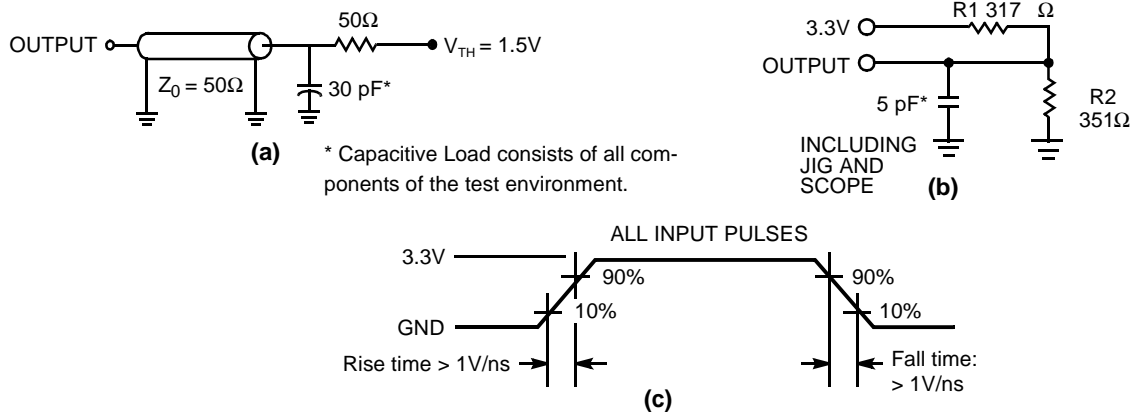
AC Switching Characteristics Over the Operating Range [4]

| Parameter	Description	-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
Read Cycle								
t_{power}	V_{CC}(typical) to the first access[5]	1		1		1		ms
t_{RC}	Read Cycle Time	8		10		12		ns
t_{AA}	Address to Data Valid		8		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW / CE_2 HIGH to Data Valid		8		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	1		1		1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6]		5		5		6	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Low-Z[6]	3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to High-Z[6]		5		5		6	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to Power-Up[7]	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to Power-Down[7]		8		10		12	ns
t_{DBE}	Byte Enable to Data Valid		5		5		6	ns
t_{LZBE}	Byte Enable to Low-Z	1		1		1		ns
t_{HZBE}	Byte Disable to High-Z		5		5		6	ns
Write Cycle[8, 9]								
t_{WC}	Write Cycle Time	8		10		12		ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Write End	6		7		8		ns

Notes:
3. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and specified transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
5. This part has a voltage regulator which steps down the voltage from 3V to 2V internally. t_{power} time has to be provided initially before a Read/Write operation is started.
6. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
7. These parameters are guaranteed by design and are not tested.
8. The internal Write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW (CE_2 HIGH) and $\overline{WE}$ LOW. Chip enables must be active and $\overline{WE}$ and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
9. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

## AC Switching Characteristics Over the Operating Range (continued)[4]

Parameter	Description	-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
t_{AW}	Address Set-up to Write End	6		7		8		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		8		ns
t_{SD}	Data Set-up to Write End	5		5.5		6		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6]		5		5		6	ns
t_{BW}	Byte Enable to End of Write	6		7		8		ns

Data Retention Waveform
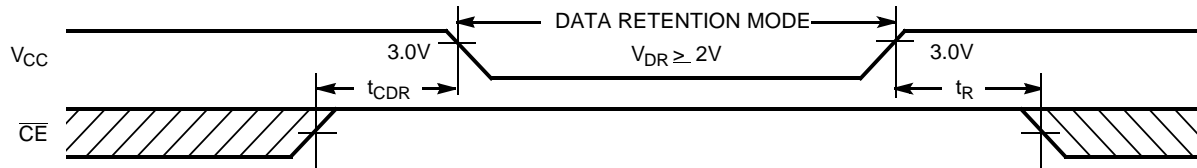
Switching Waveforms

Read Cycle No. 1[10, 11]
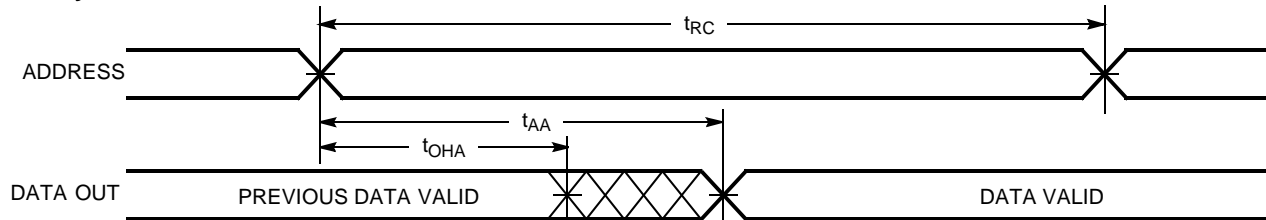
Notes:
10. Device is continuously selected. $\overline{OE}, \overline{CE}, \overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}. CE2 = V_{IH}.
11. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)[11, 12]
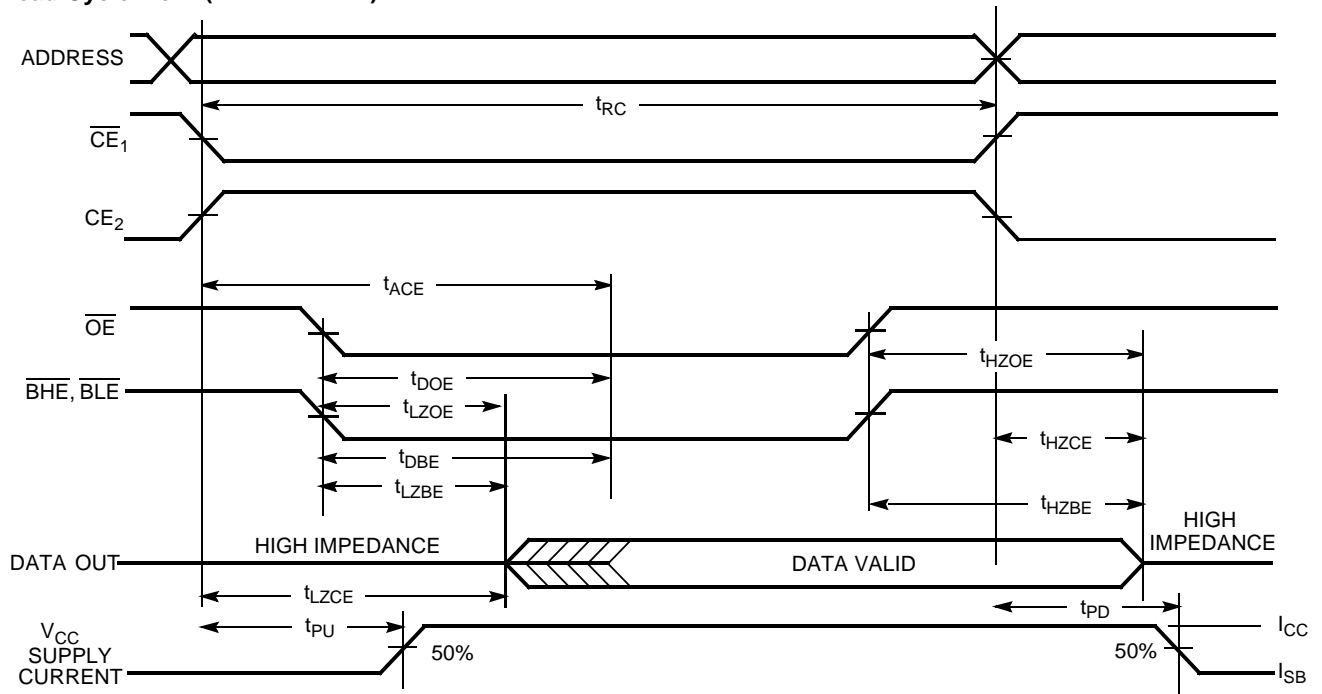
Write Cycle No. 1 ($\overline{CE}$ Controlled)[13, 14, 15]
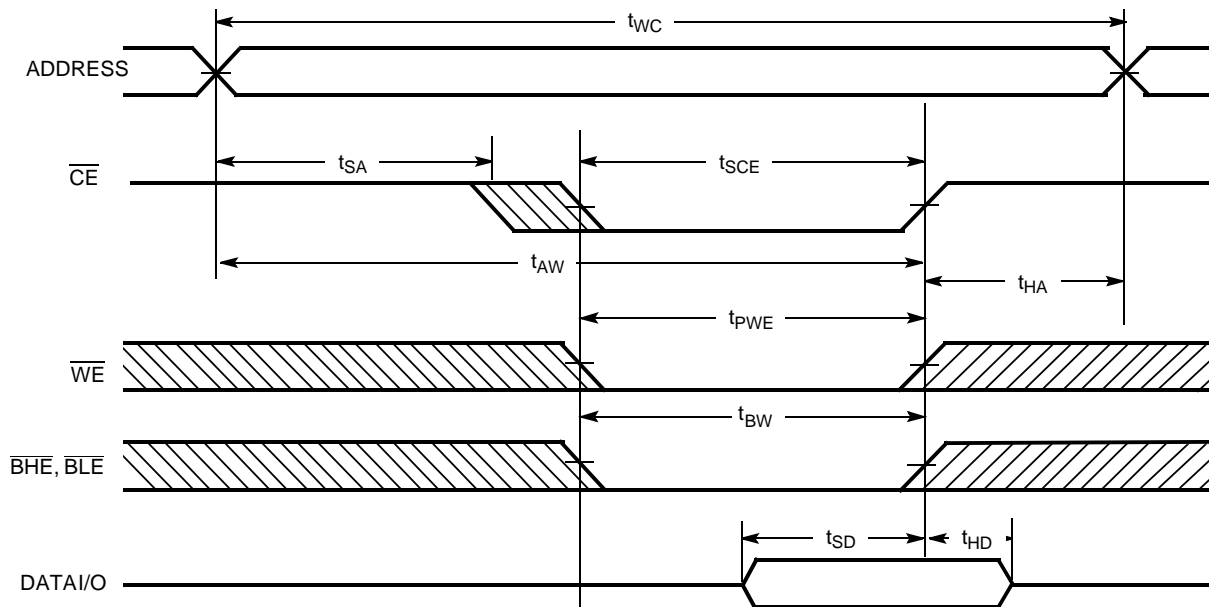
Notes:
12. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
13. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE} = V_{IH}$.
14. If $\overline{CE}_1$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
15. $\overline{CE}$ is a shorthand combination of both $\overline{CE}_1$ and CE_2 combined. It is active LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)
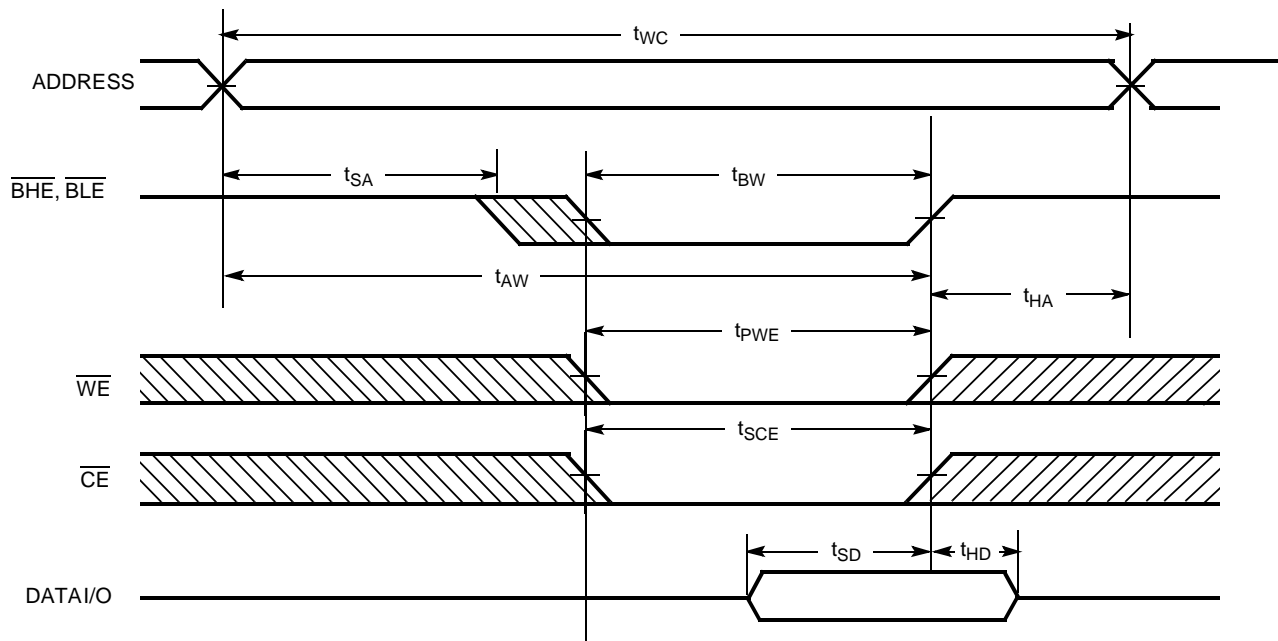
Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[13, 14, 15]
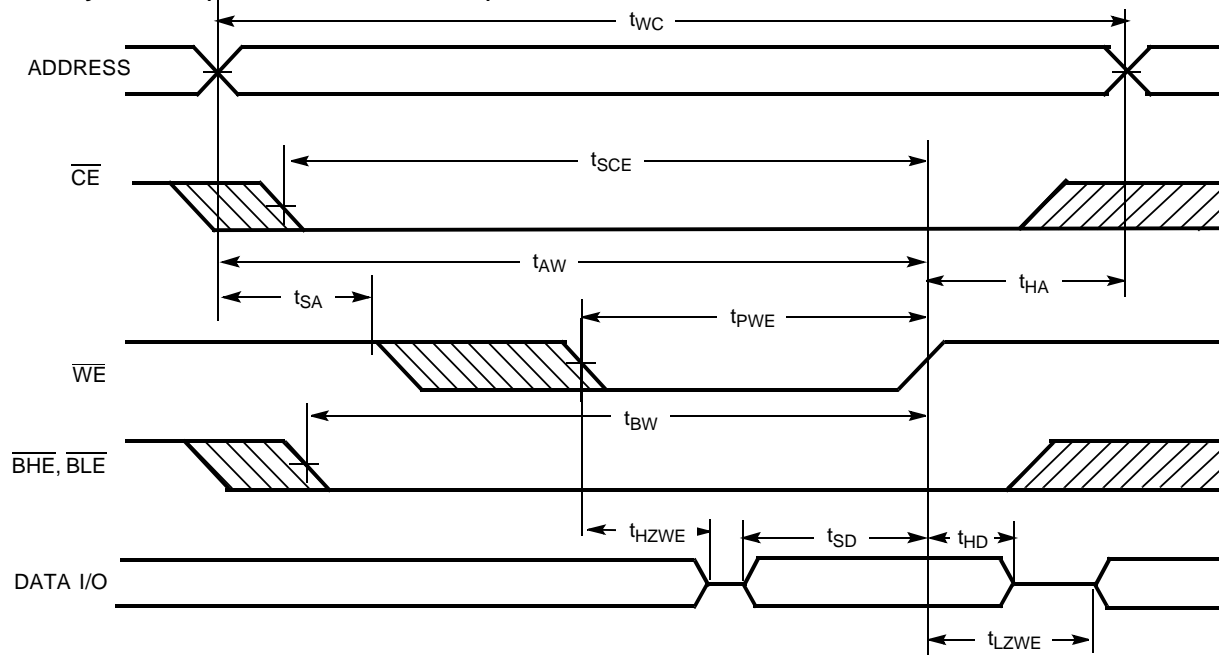
Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
X	L	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	H	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	H	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	H	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	H	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	H	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	H	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code[16]	Package Name	Package Type	Operating Range
8	CY7C1061AV33-8ZC	Z54-II	54-pin TSOP II	Commercial
	CY7C1061AV33-8ZI			Industrial
	CY7C1061AV33-8BAC	BA48G	48-ball Mini BGA	Commercial
	CY7C1061AV33-8BAI			Industrial
10	CY7C1061AV33-10ZC	Z54-II	54-pin TSOP II	Commercial
	CY7C1061AV33-10ZI			Industrial
	CY7C1061AV33-10BAC	BA48G	48-ball Mini BGA	Commercial
	CY7C1061AV33-10BAI			Industrial
12	CY7C1061AV33-12ZC	Z54-II	54-pin TSOP II	Commercial
	CY7C1061AV33-12ZI			Industrial
	CY7C1061AV33-12BAC	BA48G	48-ball Mini BGA	Commercial
	CY7C1061AV33-12BAI			Industrial

Note:
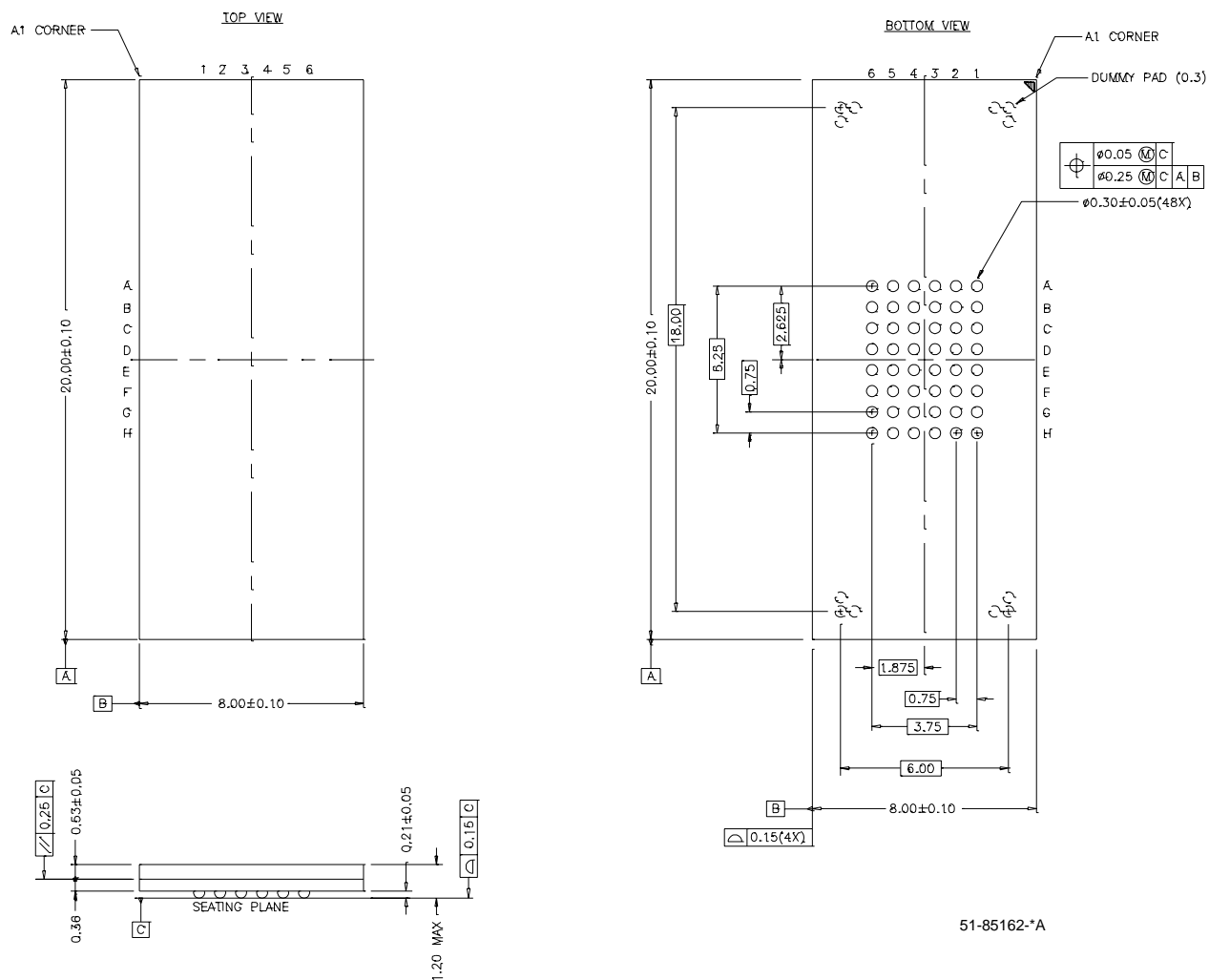16. Contact a Cypress representative for availability of the 48-ball Mini BGA (BA48) package.

Package Diagrams

54-lead Thin Small Outline Package, Type II Z54-II

DIMENSION IN MM (INCH)
$$\frac{MIN.}{MAX}$$
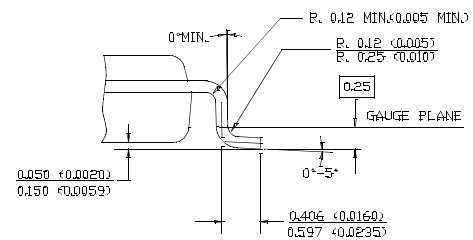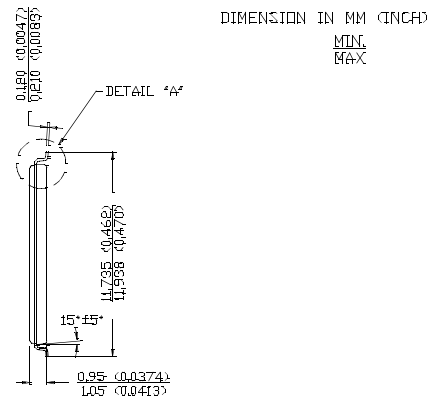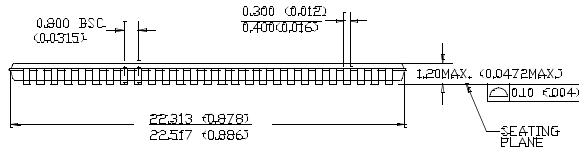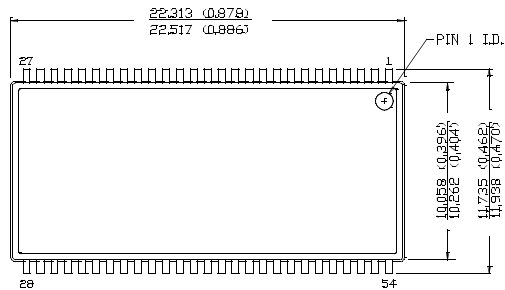
DETAIL "A"

51-85160-**

Package Diagrams (continued)

48-ball (8 mm x 20 mm x 1.2 mm) FBGA BA48G

51-85162-*A

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Document History Page

Document Title: CY7C1061AV33 1M x 16 Static RAM Document Number: 38-05256				

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113725	03/28/02	NSL	New Data Sheet
*A	117058	07/31/02	DFP	Removed 15-ns bin.
*B	117989	08/30/02	DFP	Added 8-ns bin. Changed Icc for 8, 10, 12 bins. t_{power} changed from 1 μs to 1 ms. Load Cap Comment changed (for Tx line load). t_{SD} changed to 5.5 ns for the 10-ns bin. Changed some 8-ns bin numbers (t_{HZ}, t_{DOE}, t_{DBE}). Removed hz<lz comments from data sheet.
*C	120383	11/06/02	DFP	Final data sheet. Added note 3 to "AC Test Loads and Waveforms" and note 7 to t_{pu} and t_{pd}. Updated Input/Output Caps (for 48BGA only) to 8 pF/10 pF and for the 54-pin TSOP to 6/8 pF.
*D	124439	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA. Shaded fBGA production ordering information.