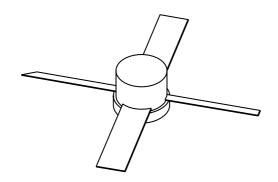
## **DISCRETE SEMICONDUCTORS**

## DATA SHEET



# **BLF521**UHF power MOS transistor

Product specification Supersedes data of 1998 Jan 07 2003 Sep 02





## **UHF power MOS transistor**

**BLF521** 

#### **FEATURES**

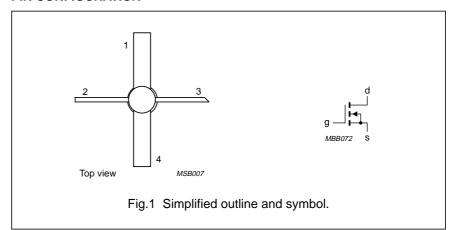
- · High power gain
- · Easy power control
- · Gold metallization
- · Good thermal stability
- · Withstands full load mismatch
- Designed for broadband operation.

#### **DESCRIPTION**

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT172D studless package, with a ceramic cap. All leads are isolated from the mounting base.

#### PIN CONFIGURATION



#### **CAUTION**

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

#### **PINNING - SOT172D**

PIN	DESCRIPTION			
1	source			
2	gate			
3	drain			
4	source			

#### WARNING

### Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

#### QUICK REFERENCE DATA

RF performance at  $T_{amb}$  = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)
CW, class-B	500	12.5	2	>10	>50

## **UHF** power MOS transistor

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#### **LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 60134).

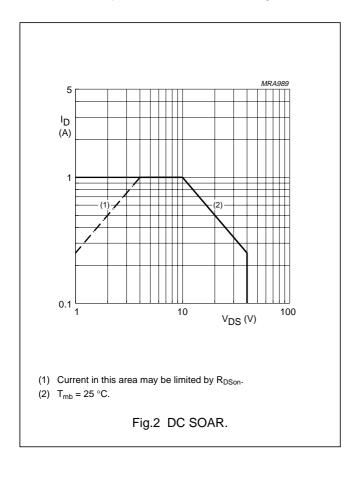
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		_	40	V
$V_{GS}$	gate-source voltage		_	±20	V
I <sub>D</sub>	drain current (DC)		_	1	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> ≤ 25 °C	_	10	W
T <sub>stg</sub>	storage temperature		-65	150	°C
Tj	junction temperature		_	200	°C

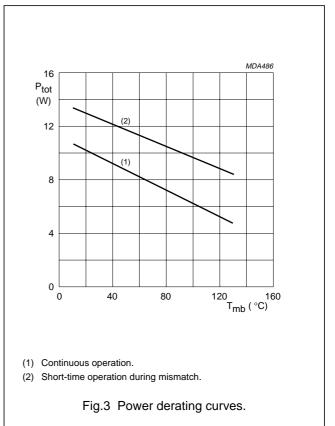
## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R <sub>th j-mb</sub>	thermal resistance from junction to mounting base	17.5	K/W
R <sub>th j-a</sub>	thermal resistance from junction to ambient; note1	75	K/W

#### Note

1. Mounted on printed-circuit board; see Fig.12.





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## **CHARACTERISTICS**

 $T_j = 25$  °C unless otherwise specified.

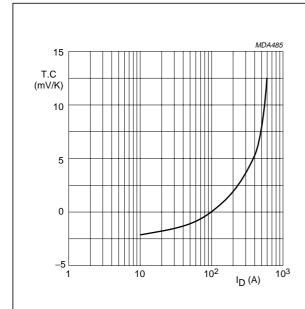
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0; I <sub>D</sub> = 3 mA	40	_	_	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>GS</sub> = 0; V <sub>DS</sub> = 12.5 V	_	_	10	μΑ
I <sub>GSS</sub>	gate-source leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$	_	_	1	μΑ
$V_{GSth}$	gate-source threshold voltage	$I_D = 3 \text{ mA}; V_{DS} = 10 \text{ V}$	2	_	4.5	V
g <sub>fs</sub>	forward transconductance	I <sub>D</sub> = 0.3 A; V <sub>DS</sub> = 10 V	80	135	_	mS
R <sub>DSon</sub>	drain-source on-state resistance	$I_D = 0.3 \text{ A}; V_{GS} = 15 \text{ V}$	_	3.5	4	Ω
I <sub>DSX</sub>	on-state drain current	V <sub>GS</sub> = 15 V; V <sub>DS</sub> = 10 V	_	1.3	_	Α
C <sub>is</sub>	input capacitance	$V_{GS} = 0$ ; $V_{DS} = 12.5 \text{ V}$ ; $f = 1 \text{ MHz}$	_	5.3	_	pF
Cos	output capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 12.5 V; f = 1 MHz	_	7.8	_	pF
C <sub>rs</sub>	feedback capacitance	$V_{GS} = 0$ ; $V_{DS} = 12.5 \text{ V}$ ; $f = 1 \text{ MHz}$	_	1.8	_	pF

## V<sub>GS</sub> group indicator

GROUP		LIMITS (V)		LIMITS (V)		
	MIN.	MAX.		MIN.	MAX.	
A	2.0	2.1	0	3.3	3.4	
В	2.1	2.2	Р	3.4	3.5	
С	2.2	2.3	Q	3.5	3.6	
D	2.3	2.4	R	3.6	3.7	
E	2.4	2.5	S	3.7	3.8	
F	2.5	2.6	Т	3.8	3.9	
G	2.6	2.7	U	3.9	4.0	
Н	2.7	2.8	V	4.0	4.1	
J	2.8	2.9	W	4.1	4.2	
K	2.9	3.0	Х	4.2	4.3	
L	3.0	3.1	Y	4.3	4.4	
М	3.1	3.2	Z	4.4	4.5	
N	3.2	3.3				

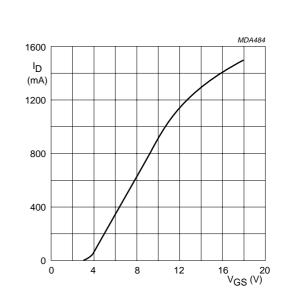
## **UHF** power MOS transistor

**BLF521** 



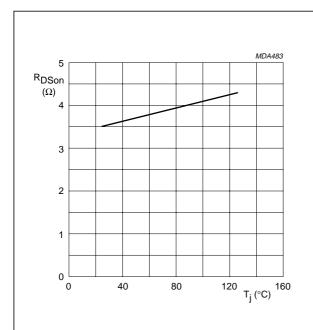
 $V_{DS} = 10 \text{ V}.$ 

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



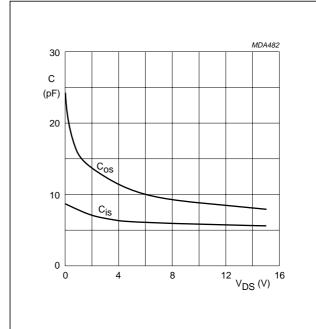
 $V_{DS}$  = 10  $V_{;}$   $T_{j}$  = 25  $^{\circ}$ C.

Fig.5 Drain current as a function of gate-source voltage; typical values.



 $I_D = 0.3 A$ ;  $V_{GS} = 15 V$ .

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.

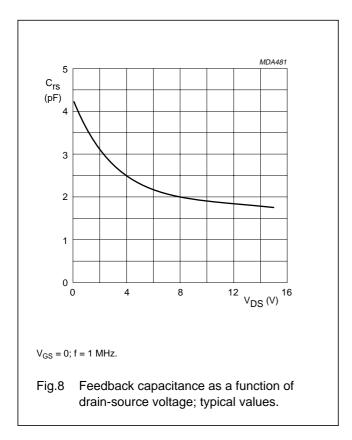


 $V_{GS} = 0$ ; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.

## **UHF** power MOS transistor

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## **APPLICATION INFORMATION FOR CLASS-B OPERATION**

 $T_{amb} = 25 \, ^{\circ}C$ ;  $R_{GS} = 274 \, \Omega$ , unless otherwise specified.

RF performance in a common source class-B test circuit.

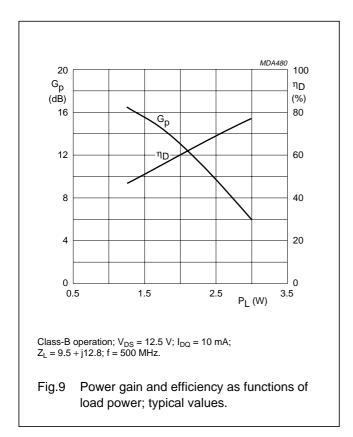
MODE OF OPERATION	f	V <sub>DS</sub>	I <sub>DQ</sub>	P <sub>L</sub>	G <sub>p</sub>	η <sub>D</sub>
	(MHz)	(V)	(mA)	(W)	(dB)	(%)
CW, class-B	500	12.5	10	2	> 10 typ. 13	> 50 typ. 60

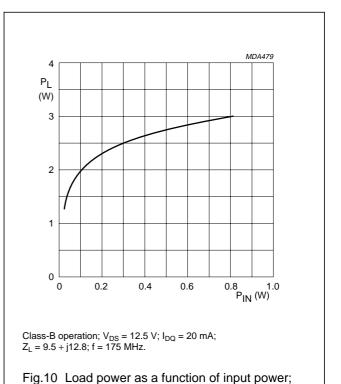
## Ruggedness in class-B operation

The BLF521 is capable of withstanding a load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:  $V_{DS} = 15.5 \text{ V}$ ; f = 500 MHz at rated output power.

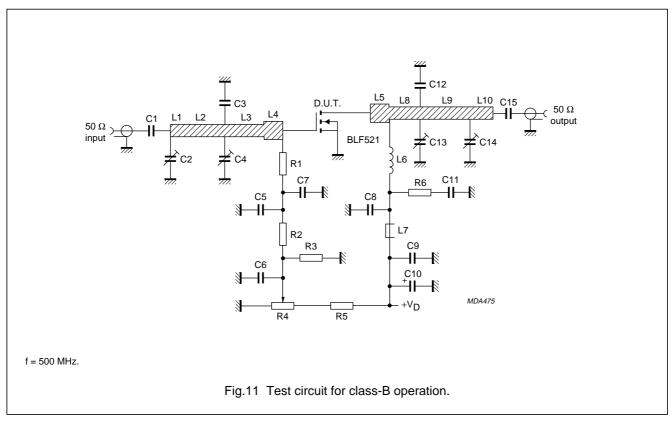
## **UHF** power MOS transistor

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typical values.



## **UHF** power MOS transistor

**BLF521** 

## List of components class-AB test circuit (see Fig.12)

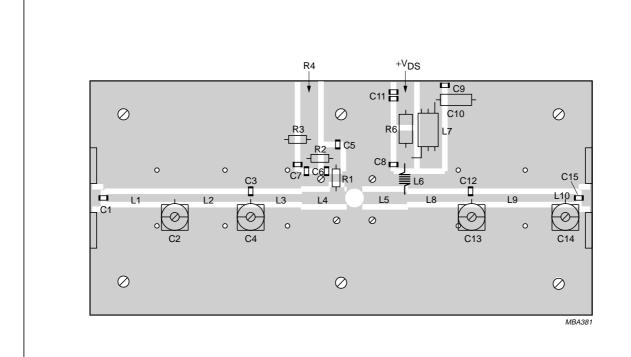
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C5, C8, C15	multilayer ceramic chip capacitor; note 1	390 pF, 500 V		
C2, C13	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3	multilayer ceramic chip capacitor; note 2	5.6 pF, 500 V		
C4	film dielectric trimmer	2 to 18 pF		2222 809 09003
C6, C11	multilayer ceramic chip capacitor	2 × 100 nF in parallel, 50 V		2222 852 47104
C7, C9	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C10	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C12	multilayer ceramic chip capacitor; note 2	9.1 pF, 50 V		
C14	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
L1	stripline; note 3		20 × 2 mm	
L2	stripline; note 3	83 Ω	21 × 2 mm	
L3	stripline; note 3	83 Ω	19 × 2 mm	
L4, L5	stripline; note 3	67 Ω	12 × 3 mm	
L6	5 turns enamelled 0.5 mm copper wire	62 nH	length 3.75 mm int. dia. 3 mm leads 2 × 4 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L8	stripline; note 3	83 Ω	18.6 × 2 mm	
L9	stripline; note 3	83 Ω	31.6 × 2 mm	
L10	stripline; note 3	83 Ω	2 × 2 mm	
R1	0.4 W metal film resistor	274 Ω		2322 151 72741
R2	0.4 W metal film resistor	1.96 kΩ		2322 151 71962
R3	0.4 W metal film resistor	1 ΜΩ		2322 151 71005
R4	cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

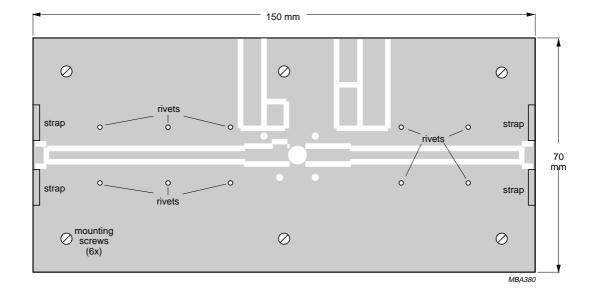
#### **Notes**

- 1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- 2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
- 3. The striplines are on a double copper-clad printed-circuit board, with PTFE fibre-glass dielectric ( $\varepsilon_r$  = 2.2), thickness 1.6 mm.

## **UHF** power MOS transistor

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The circuit and components are situated on one side of the printed-circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz test circuit.

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2003 Sep 02

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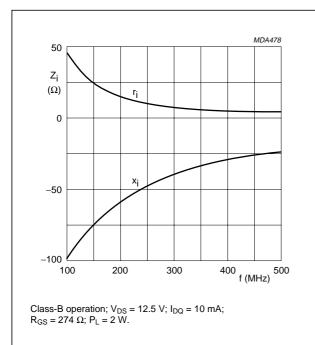


Fig.13 Input impedance as a function of frequency (series components); typical values per section.

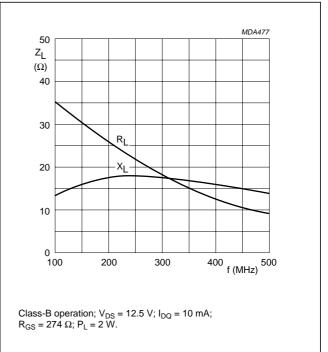
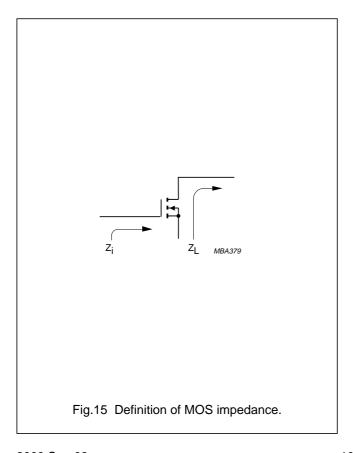
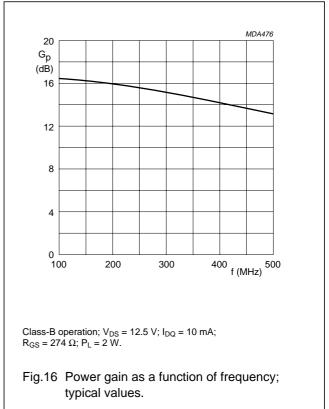


Fig.14 Load impedance as a function of frequency (series components); typical values.





## **UHF** power MOS transistor

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## **BLF521** scattering parameters

 $V_{DS} = 12.5 \text{ V}; I_D = 10 \text{ mA.}; \text{ note 1}$ 

f (MHz)		S <sub>11</sub>	S	11	s <sub>1</sub>	2	s <sub>22</sub>		
1 (WITIZ)	s <sub>11</sub>	∠Φ	s <sub>21</sub>	∠Φ	s <sub>12</sub>	∠Φ	s <sub>22</sub>	∠Φ	
5	1.00	-1.6	4.51	178.5	0.01	88.5	0.98	-2.0	
10	1.00	-3.2	4.51	177.0	0.01	87.2	0.98	-4.0	
20	1.00	-6.4	4.50	173.9	0.02	84.5	0.98	-8.0	
30	1.00	-9.6	4.48	170.9	0.03	81.7	0.98	-12.0	
40	0.99	-12.8	4.45	167.9	0.04	79.0	0.97	-16.0	
50	0.99	-16.0	4.43	164.9	0.05	76.2	0.97	-19.9	
60	0.98	-19.1	4.39	161.9	0.06	73.5	0.97	-23.8	
70	0.97	-22.1	4.34	158.9	0.07	70.9	0.96	-27.6	
80	0.97	-25.1	4.28	156.1	0.08	68.3	0.96	-31.3	
90	0.96	-28.0	4.22	153.3	0.08	65.8	0.95	-34.9	
100	0.95	-30.9	4.16	150.5	0.09	63.3	0.94	-38.5	
125	0.92	-37.9	4.00	144.0	0.11	57.5	0.93	-47.1	
150	0.90	-44.3	3.83	137.6	0.13	51.8	0.91	-55.2	
175	0.87	-50.4	3.64	131.8	0.14	46.7	0.89	-62.7	
200	0.85	-56.0	3.46	126.5	0.15	42.2	0.88	-69.6	
250	0.80	-66.2	3.12	116.4	0.17	33.4	0.85	-81.9	
300	0.77	-75.1	2.81	108.0	0.18	26.4	0.82	-92.3	
350	0.74	-82.9	2.54	100.1	0.19	19.8	0.81	-101.3	
400	0.72	-89.7	2.31	93.5	0.19	14.4	0.79	-108.9	
450	0.70	-95.9	2.10	87.1	0.19	9.5	0.79	-115.5	
500	0.69	-101.5	1.93	81.4	0.19	4.9	0.78	-121.2	
600	0.69	-111.3	1.64	71.2	0.19	-2.6	0.78	-130.7	
700	0.69	-119.9	1.41	62.2	0.18	-8.7	0.77	-138.5	
800	0.69	-127.9	1.23	54.3	0.17	-13.6	0.78	-145.2	
900	0.70	-135.1	1.08	47.3	0.15	-17.7	0.78	-151.4	
1000	0.72	-142.0	0.97	40.9	0.14	-21.1	0.79	-156.9	

## Note

<sup>1.</sup> For more extensive s-parameters see internet: http://www.semiconductors.philips.com/markets/communications/wirelesscommunication/broadcast

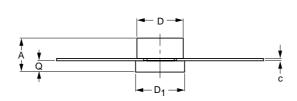
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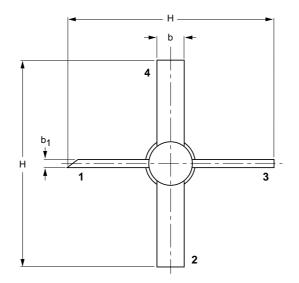
**BLF521** 

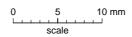
## **PACKAGE OUTLINE**

Studless ceramic package; 4 leads

SOT172D







## DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	С	D	D <sub>1</sub>	н	Q
mm	3.71	3.31	0.89	0.16	5.20	5.33	26.17	1.15
	2.89	3.04	0.63	0.10	4.95	5.08	24.63	0.88
inches	0.146	0.13	0.035	0.006	0.205	0.210	1.03	0.045
	0.114	0.12	0.025	0.004	0.195	0.200	0.97	0.035

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT172D						97-06-28

## **UHF** power MOS transistor

**BLF521** 

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