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Team Nexperia

# 74LVT16500A

## 3.3 V 18-bit universal bus transceiver; 3-state

Rev. 03 — 29 May 2006 Product data sheet

## 1. General description

The 74LVT16500A is a high-performance BiCMOS product designed for $V_{CC}$ operation at 3.3 V.

This device is an 18-bit universal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock ($\overline{CPAB}$ and $\overline{CPBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{CPAB}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A-bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CPAB}$. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and $\overline{CPBA}$. The output enables are complimentary (OEAB is active HIGH, and $\overline{OEBA}$ is active LOW).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## 2. Features

- 18-bit bidirectional bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Negative edge-triggered clock inputs
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 Method 3015: exceeds 2000 V
  - CDM JESD22-C101-C exceeds 1000 V

PHILIPS

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVT16500ADGG | –40 °C to +85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |
| 74LVT16500ADL | –40 °C to +85 °C | SSOP56 | plastic shrink small outline package; 56 leads; body width 7.5 mm | SOT371-1 |

## 4. Functional diagram

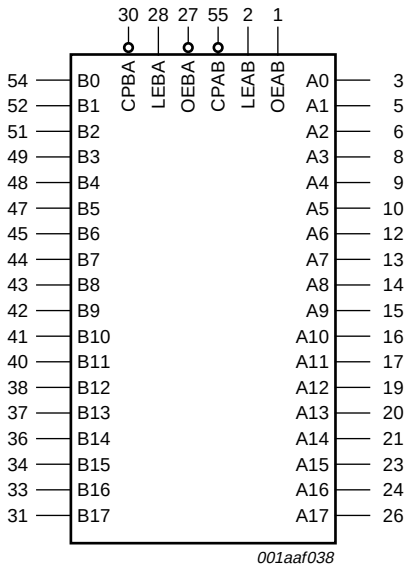



Fig 1. Logic symbol

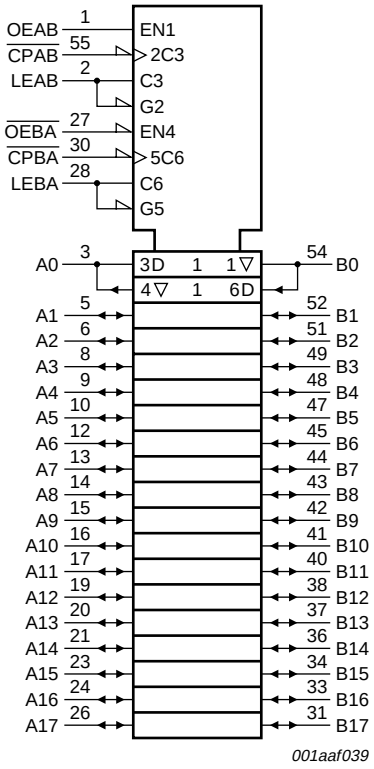



Fig 2. IEC logic symbol

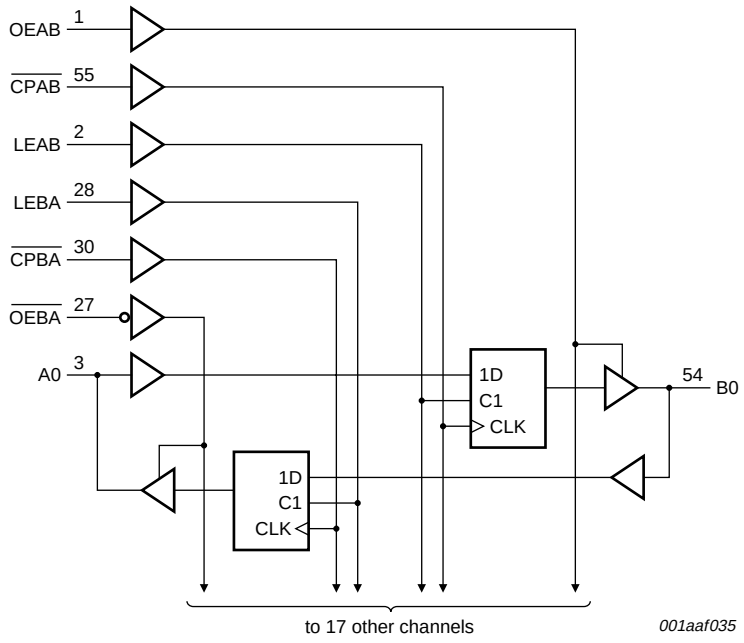



**Fig 3. Logic diagram**

# 5. Pinning information

## 5.1 Pinning

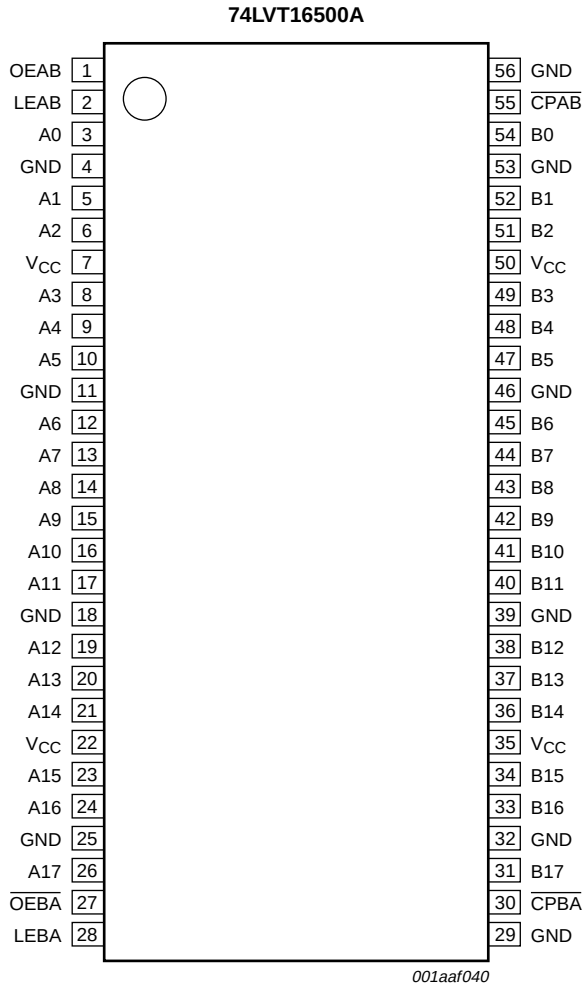



**Fig 4. Pin configuration**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| OEAB | 1 | A-to-B output enable input |
| LEAB | 2 | A-to-B latch enable input |
| A0 | 3 | data input/output A0 |
| GND | 4 | ground (0 V) |
| A1 | 5 | data input/output A1 |
| A2 | 6 | data input/output A2 |
| $V_{CC}$ | 7 | supply voltage |

**Table 2. Pin description** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| A3 | 8 | data input/output A3 |
| A4 | 9 | data input/output A4 |
| A5 | 10 | data input/output A5 |
| GND | 11 | ground (0 V) |
| A6 | 12 | data input/output A6 |
| A7 | 13 | data input/output A7 |
| A8 | 14 | data input/output A8 |
| A9 | 15 | data input/output A9 |
| A10 | 16 | data input/output A10 |
| A11 | 17 | data input/output A11 |
| GND | 18 | ground (0 V) |
| A12 | 19 | data input/output A12 |
| A13 | 20 | data input/output A13 |
| A14 | 21 | data input/output A14 |
| $V_{CC}$ | 22 | supply voltage |
| A15 | 23 | data input/output A15 |
| A16 | 24 | data input/output A16 |
| GND | 25 | ground (0 V) |
| A17 | 26 | data input/output A17 |
| $\overline{OEBA}$ | 27 | B-to-A output enable input (active LOW) |
| LEBA | 28 | B-to-A latch enable input |
| GND | 29 | ground (0 V) |
| $\overline{CPBA}$ | 30 | B-to-A clock input (active falling edge) |
| B17 | 31 | data input/output B17 |
| GND | 32 | ground (0 V) |
| B16 | 33 | data input/output B16 |
| B15 | 34 | data input/output B15 |
| $V_{CC}$ | 35 | supply voltage |
| B14 | 36 | data input/output B14 |
| B13 | 37 | data input/output B13 |
| B12 | 38 | data input/output B12 |
| GND | 39 | ground (0 V) |
| B11 | 40 | data input/output B11 |
| B10 | 41 | data input/output B10 |
| B9 | 42 | data input/output B9 |
| B8 | 43 | data input/output B8 |
| B7 | 44 | data input/output B7 |
| B6 | 45 | data input/output B6 |
| GND | 46 | ground (0 V) |
| B5 | 47 | data input/output B5 |
| B4 | 48 | data input/output B4 |

**Table 2. Pin description** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| B3 | 49 | data input/output B3 |
| $V_{CC}$ | 50 | supply voltage |
| B2 | 51 | data input/output B2 |
| B1 | 52 | data input/output B1 |
| GND | 53 | ground (0 V) |
| B0 | 54 | data input/output B0 |
| $\overline{CPAB}$ | 55 | A-to-B clock input (active falling edge) |
| GND | 56 | ground (0 V) |

# 6. Functional description

**Table 3. Function table[1]**

| Operating mode | Control | | | Input | Internal register | Output |
|---|---|---|---|---|---|---|
| | OEAB | LEAB | $\overline{CPAB}$ | An | | Bn |
| | $\overline{OEBA}$ | LEBA | $\overline{CPBA}$ | Bn | | An |
| disabled | L | H | X | X | X | Z |
| disabled, latch data | L | ↓ | X | h | H | Z |
| disabled, latch data | L | ↓ | X | l | L | Z |
| disabled, hold data | L | L | H or L | X | NC | Z |
| disabled, clock data | L | L | ↓ | h | H | Z |
| disabled, clock data | L | L | ↓ | l | L | Z |
| transparent | H | H | X | H | H | H |
| transparent | H | H | X | L | L | L |
| latch data and display | H | ↓ | X | h | H | H |
| latch data and display | H | ↓ | X | l | L | L |
| clock data and display | H | L | ↓ | h | H | H |
| clock data and display | H | L | ↓ | l | L | L |
| hold data and display | H | L | H or L | X | H | H |
| hold data and display | H | L | H or L | X | L | L |

[1] H = HIGH voltage level;
h = HIGH voltage level one setup time prior to the enable or clock transition;
L = LOW voltage level;
l = LOW voltage level one setup time prior to the enable or clock transition;
NC = no change;
X = don't care;
Z = high-impedance OFF-state;
↓ = HIGH-to-LOW enable or clock transition.

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +4.6 | V |
| $V_I$ | input voltage | | [1] | –0.5 | +7.0 | V |
| $V_O$ | output voltage | output in OFF-state or HIGH-state | [1] | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | - | –50 | mA |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | - | –50 | mA |
| $I_O$ | output current | output in LOW-state | | - | 128 | mA |
| | | output in HIGH-state | | - | –64 | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $T_j$ | junction temperature | | [2] | - | 150 | °C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.7 | - | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.8 | V |
| $I_{OH}$ | HIGH-level output current | | - | - | –32 | mA |
| $I_{OL}$ | LOW-level output current | none | - | - | 32 | mA |
| | | current duty cycle ≤ 50 %; $f_i \geq 1$ kHz | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +85 | °C |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **$T_{amb}$ = −40 °C to 85 °C** [1] | | | | | | | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 2.7 V; $I_{IK}$ = −18 mA | | - | −0.85 | −1.2 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC}$ = 2.7 V to 3.6 V; $I_{OH}$ = −100 µA | | $V_{CC}$ − 0.2 | $V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.7 V; $I_{OH}$ = −8 mA | | 2.4 | 2.55 | - | V |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −32 mA | | 2.0 | 2.3 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 2.7 V | | | | | |
| | | $I_{OL}$ = 100 µA | | - | 0.07 | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | - | 0.3 | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | | | | | |
| | | $I_{OL}$ = 16 mA | | - | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 32 mA | | - | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 64 mA | | - | 0.36 | 0.55 | V |
| $V_{RST}$ | power-up output low voltage | $V_{CC}$ = 3.6 V; $I_O$ = 1 mA; $V_I$ = $V_{CC}$ or GND | [2] | - | 0.1 | 0.55 | V |
| $I_{LI}$ | input leakage current | | | | | | |
| | control pins | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | | - | 0.1 | ±1 | µA |
| | | $V_{CC}$ = 0 V or 3.6 V; $V_I$ = 5.5 V | | - | 0.1 | 10 | µA |
| | I/O data pins | $V_{CC}$ = 3.6 V | [3] | | | | |
| | | $V_I$ = 5.5 V | | - | 1.0 | 20 | µA |
| | | $V_I$ = $V_{CC}$ | | - | 0.1 | 10 | µA |
| | | $V_I$ = 0 V | | - | +0.1 | −5 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 4.5 V | | - | 1.0 | ±100 | µA |
| $I_{HOLD}$ | bus hold current data input | $V_{CC}$ = 3 V | [4] | | | | |
| | | $V_I$ = 0.8 V | | 75 | 130 | - | µA |
| | | $V_I$ = 2.0 V | | −75 | −130 | - | µA |
| | | $V_I$ = 0 V to 3.6 V; $V_{CC}$ = 3.6 V | | ±500 | - | - | µA |
| $I_{EX}$ | external current into output | output in the HIGH-state when $V_O$ > $V_{CC}$; $V_O$ = 5.5 V; $V_{CC}$ = 3.0 V | | - | 50 | 125 | µA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC}$ ≤ 1.2 V; $V_O$ = 0.5 V to $V_{CC}$; $V_I$ = GND or $V_{CC}$; OEAB or $\overline{OEBA}$ don't care | [5] | - | 40 | ±100 | µA |
| $I_{CC}$ | quiescent supply current | $V_{CC}$ = 3.6 V; $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A | | | | | |
| | | outputs HIGH-state | | - | 0.07 | 0.12 | mA |
| | | outputs LOW-state | | - | 4 | 6 | mA |
| | | outputs disabled | [6] | - | 0.07 | 0.12 | mA |

**Table 6. Static characteristics** *...continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | additional quiescent supply current | per input pin; $V_{CC}$ = 3 V to 3.6 V; one input at $V_{CC}$ – 0.6 V; other inputs at $V_{CC}$ or GND | [7] | - | 0.1 | 0.2 | mA |
| $C_i$ | input capacitance | control pins; $V_I$ = 0 V or 3.0 V | | - | 3 | - | pF |
| $C_{io}$ | input/output capacitance | I/O pins; $V_{I/O}$ = 0 V or 3.0 V | | - | 9 | - | pF |

[1] Typical values are at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at $V_{CC}$ or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any $V_{CC}$ between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC}$ = 1.2 V to $V_{CC}$ = 3.0 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for $T_{amb}$ = 25 °C only.

[6] $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{CC}$ = 2.7 V; $T_{amb}$ = −40 °C to 85 °C** | | | | | | |
| $t_{PLH}$ | propagation delay | | | | | |
| | An to Bn or Bn to An | see Figure 5 | - | - | 5.4 | ns |
| | $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An | see Figure 6 | - | - | 6.4 | ns |
| | LEAB to Bn or LEBA to An | see Figure 7 | - | - | 6.4 | ns |
| $t_{PHL}$ | propagation delay | | | | | |
| | An to Bn or Bn to An | see Figure 5 | - | - | 5.4 | ns |
| | $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An | see Figure 6 | - | - | 6.4 | ns |
| | LEAB to Bn or LEBA to An | see Figure 7 | - | - | 6.4 | ns |
| $t_{PZH}$ | output enable time to HIGH-level | see Figure 8 | - | - | 5.5 | ns |
| $t_{PZL}$ | output enable time to LOW-level | see Figure 9 | - | - | 5.2 | ns |
| $t_{PHZ}$ | output disable time from HIGH-level | see Figure 8 | - | - | 6.3 | ns |
| $t_{PLZ}$ | output disable time from LOW-level | see Figure 9 | - | - | 5.6 | ns |
| $t_{su(H)}$ | setup time HIGH | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 2.5 | - | - | ns |
| | An to LEAB with $\overline{CPAB}$ LOW or Bn to LEBA with $\overline{CPBA}$ LOW | see Figure 10 | 2.2 | - | - | ns |
| | An to LEAB with $\overline{CPAB}$ HIGH or Bn to LEBA with $\overline{CPBA}$ HIGH | see Figure 10 | 2.7 | - | - | ns |

**Table 7. Dynamic characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{su(L)}$ | setup time LOW | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 2.5 | - | - | ns |
| | An to LEAB with $\overline{CPAB}$ LOW or Bn to LEBA with $\overline{CPBA}$ LOW | see Figure 10 | 2.2 | - | - | ns |
| | An to LEAB with $\overline{CPAB}$ HIGH or Bn to LEBA with $\overline{CPBA}$ HIGH | see Figure 10 | 2.7 | - | - | ns |
| $t_{h(H)}$ | hold time HIGH | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 0 | - | - | ns |
| | An to LEAB or Bn to LEBA | see Figure 10 | 0 | - | - | ns |
| $t_{h(L)}$ | hold time LOW | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 0 | - | - | ns |
| | An to LEAB or Bn to LEBA | see Figure 10 | 0 | - | - | ns |
| $t_{WH}$ | pulse width HIGH | | | | | |
| | $\overline{CPAB}$ or $\overline{CPBA}$ | see Figure 6 | 1.5 | - | - | ns |
| | LEAB or LEBA | see Figure 7 | 1.5 | - | - | ns |
| $t_{WL}$ | pulse width LOW | | | | | |
| | $\overline{CPAB}$ or $\overline{CPBA}$ | see Figure 6 | 1.5 | - | - | ns |
| **$V_{CC}$ = 3.0 V ± 0.3 V; $T_{amb}$ = −40 °C to 85 °C[1]** | | | | | | |
| $t_{PLH}$ | propagation delay | | | | | |
| | An to Bn or Bn to An | see Figure 5 | 0.5 | 1.9 | 4.2 | ns |
| | $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An | see Figure 6 | 1.0 | 3.2 | 5.4 | ns |
| | LEAB to Bn or LEBA to An | see Figure 7 | 1.0 | 2.4 | 5.4 | ns |
| $t_{PHL}$ | propagation delay | | | | | |
| | An to Bn or Bn to An | see Figure 5 | 0.5 | 1.9 | 4.2 | ns |
| | $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An | see Figure 6 | 1.0 | 3.2 | 5.4 | ns |
| | LEAB to Bn or LEBA to An | see Figure 7 | 1.0 | 2.9 | 5.4 | ns |
| $t_{PZH}$ | output enable time to HIGH-level | see Figure 8 | 1.0 | 2.4 | 4.8 | ns |
| $t_{PZL}$ | output enable time to LOW-level | see Figure 9 | 1.0 | 2.2 | 4.8 | ns |
| $t_{PHZ}$ | output disable time from HIGH-level | see Figure 8 | 1.0 | 2.8 | 5.8 | ns |
| $t_{PLZ}$ | output disable time from LOW-level | see Figure 9 | 1.0 | 3.2 | 5.2 | ns |
| $t_{su(H)}$ | setup time HIGH | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 2.4 | 1.0 | - | ns |
| | An to LEAB with $\overline{CPAB}$ LOW or Bn to LEBA with $\overline{CPBA}$ LOW | see Figure 10 | 2.3 | 0.9 | - | ns |
| | An to LEAB with $\overline{CPAB}$ HIGH or Bn to LEBA with $\overline{CPBA}$ HIGH | see Figure 10 | 2.4 | 0.9 | - | ns |
| $t_{su(L)}$ | setup time LOW | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 2.4 | 0.7 | - | ns |
| | An to LEAB with $\overline{CPAB}$ LOW or Bn to LEBA with $\overline{CPBA}$ LOW | see Figure 10 | 2.3 | 0.9 | - | ns |
| | An to LEAB with $\overline{CPAB}$ HIGH or Bn to LEBA with $\overline{CPBA}$ HIGH | see Figure 10 | 2.4 | 0.8 | - | ns |

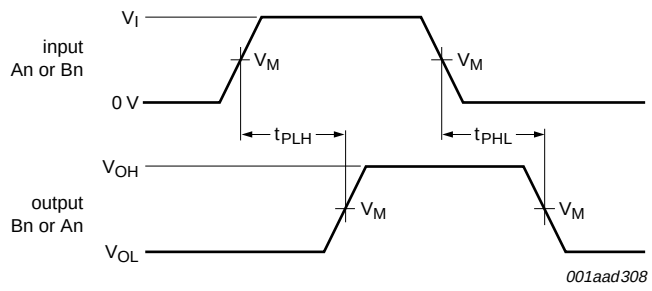
**Table 7. Dynamic characteristics** *...continued*

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{h(H)}$ | hold time HIGH | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 0 | 0 | - | ns |
| | An to LEAB or Bn to LEBA | see Figure 10 | 0 | 0 | - | ns |
| $t_{h(L)}$ | hold time LOW | | | | | |
| | An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$ | see Figure 10 | 0 | 0 | - | ns |
| | An to LEAB or Bn to LEBA | see Figure 10 | 0 | 0 | - | ns |
| $t_{WH}$ | pulse width HIGH | | | | | |
| | $\overline{CPAB}$ or $\overline{CPBA}$ | see Figure 6 | 1.2 | 0.8 | - | ns |
| | LEAB or LEBA | see Figure 7 | 1.2 | 0.8 | - | ns |
| $t_{WL}$ | pulse width LOW | | | | | |
| | $\overline{CPAB}$ or $\overline{CPBA}$ | see Figure 6 | 1.2 | 0.8 | - | ns |
| $f_{max}$ | maximum input clock frequency | see Figure 6 | 150 | 350 | - | MHz |

[1] All typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

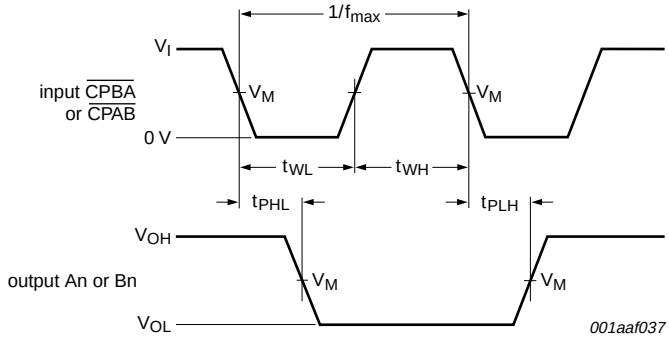
## 11. Waveforms




Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output drop that occur with the output load.

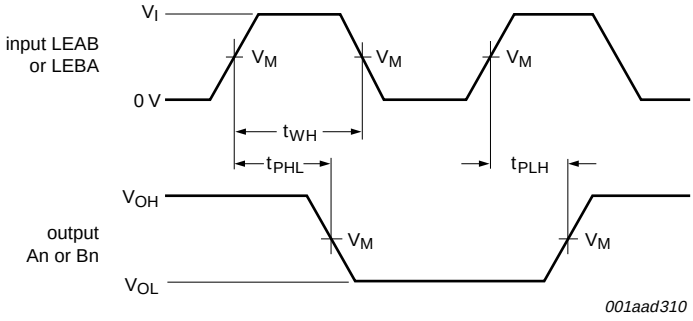
**Fig 5. Propagation delay input (An, Bn) to output (Bn, An) in transparent mode**




Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output drop that occur with the output load.

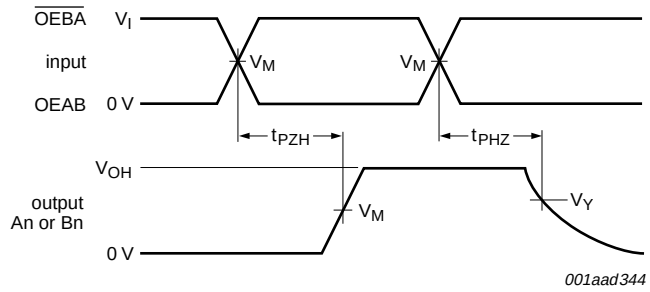
**Fig 6. Propagation delay clock ($\overline{CPAB}$, $\overline{CPBA}$) to output (An, Bn), clock ($\overline{CPAB}$, $\overline{CPBA}$) pulse width and maximum clock frequency ($\overline{CPAB}$, $\overline{CPBA}$)**




Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output drop that occur with the output load.

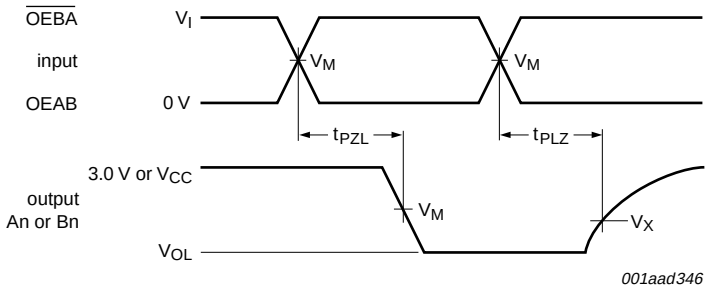
**Fig 7. Propagation delay latch enable (LEAB, LEBA) to output (An, Bn) and latch enable (LEAB, LEBA) pulse width**




Measurements points are given in Table 8.

$V_{OH}$ is typical voltage output drop that occur with the output load.

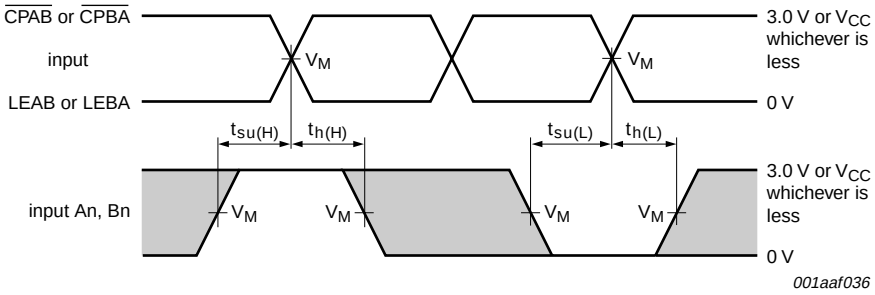
**Fig 8. 3-state output enable time to HIGH-level and output disable time from HIGH-level**




Measurements points are given in Table 8.

$V_{OL}$ is typical voltage output drop that occur with the output load.

**Fig 9. 3-state output enable time to LOW-level and output disable time from LOW-level**



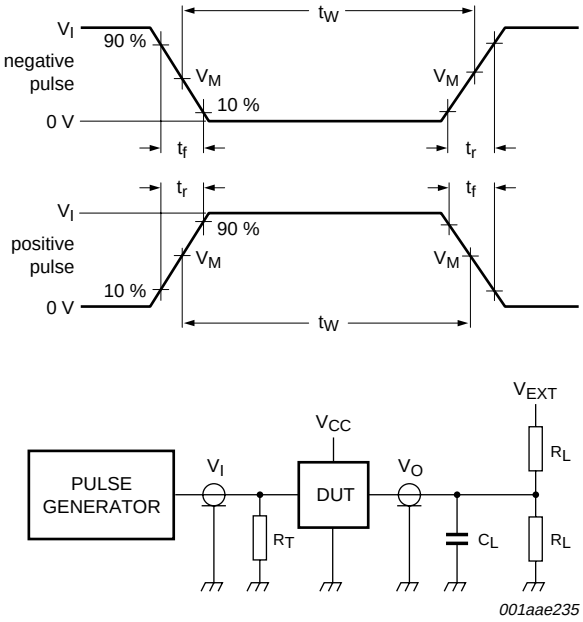

Measurements points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 10. Data setup and hold times**

**Table 8. Measurement points**

| Supply voltage | Input | Output | | |
|---|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |
| 3.3 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Test data is given in Table 9.

Definitions test circuit:

$R_L$ = Load resistor.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = Test voltage for switching times.

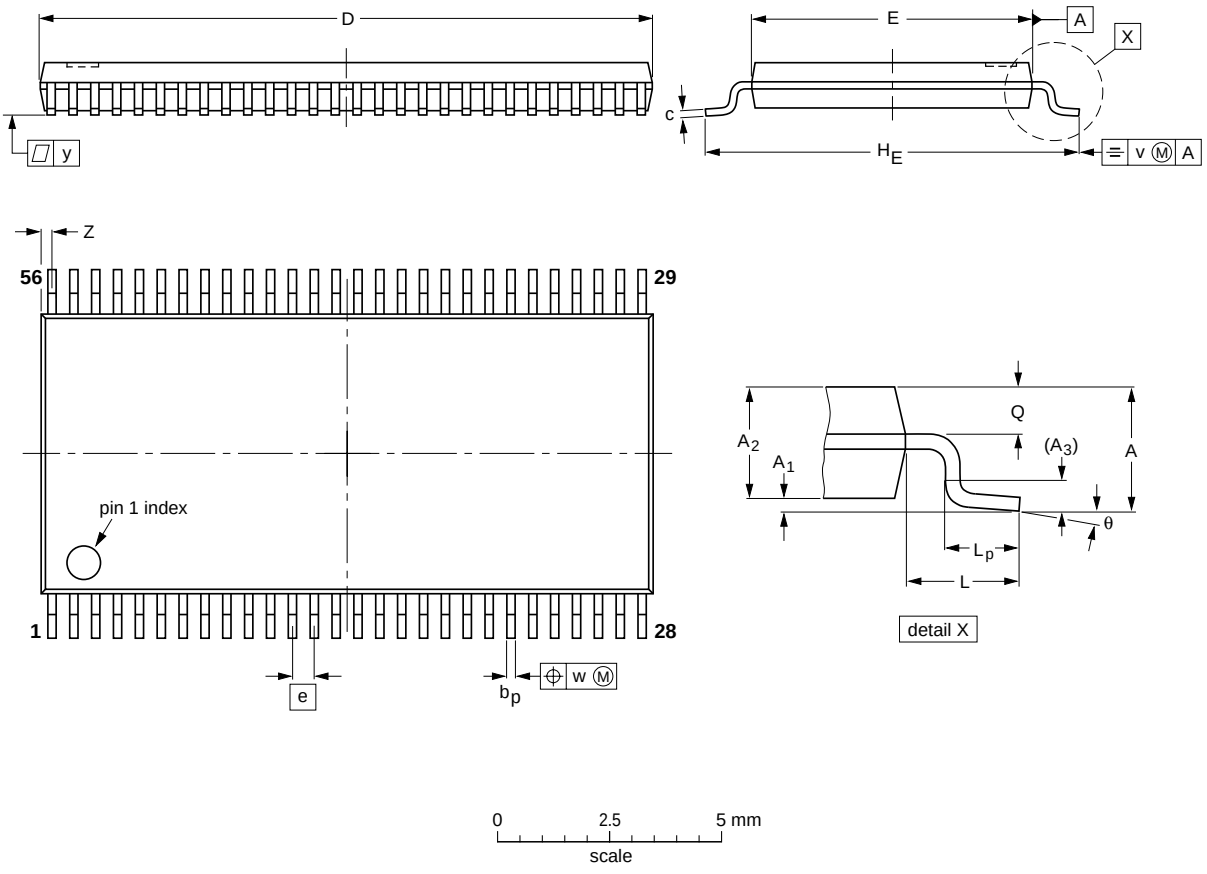
**Fig 11. Load circuitry for switching times**

**Table 9. Test data**

| Input | | | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

## 12. Package outline

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm** **SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | **0.2**<br>**0.1** | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | $8^o$<br>$0^o$ |

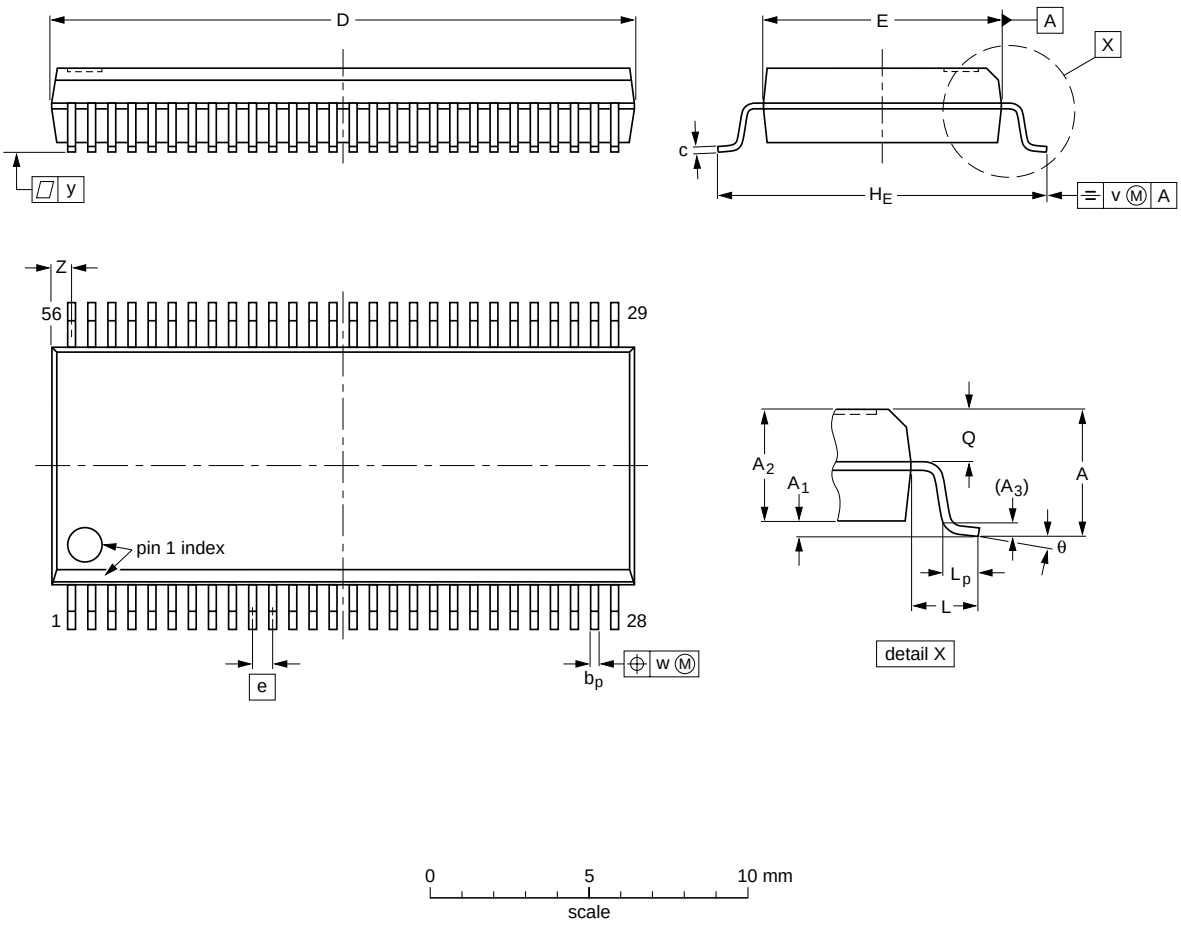
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT364-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 12. Package outline SOT364-1 (TSSOP56)**

**SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm** **SOT371-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 18.55<br>18.30 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT371-1 | | MO-118 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 13. Package outline SOT371-1 (SSOP56)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVT16500A_3 | 20060529 | Product data sheet | - | 74LVT16500A_2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors<br>• Section 2 “Features”: replaced JEDEC JC40.2 Std 17 with JESD78<br>• Figure 3 “Logic diagram”: corrected clock names and pin names<br>• Table 7 “Dynamic characteristics”: splitting up $t_{su(H)}$ and $t_{su(L)}$ parameter ‘An to LEAB or Bn to LEBA’ in 2 parameters with clock conditions and new values | | | |
| 74LVT16500A_2 (9397 750 03556) | 19980219 | Product specification | - | 74LVT16500A_1 |
| 74LVT16500A_1 | 19970612 | Product specification | - | 74LVT16500A |
| 74LVT16500A | 19950320 | Product specification | - | - |

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## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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