

# SN74CBTLV3861 LOW-VOLTAGE 10-BIT FET BUS SWITCH

SCDS041H – DECEMBER 1997 – REVISED OCTOBER 2003

- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## description/ordering information

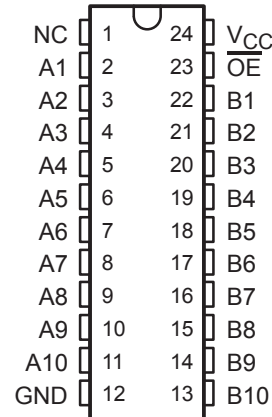
The SN74CBTLV3861 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit bus switch. When output enable ( $\overline{OE}$ ) is low, the 10-bit bus switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBQ, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – DBQ	Tape and reel	SN74CBTLV3861DBQR	CBTLV3861
	SOIC – DW	Tube	SN74CBTLV3861DW	CBTLV3861
		Tape and reel	SN74CBTLV3861DWR	
	SOP – NS	Tape and reel	SN74CBTLV3861NSR	CBTLV3861
	TSSOP – PW	Tape and reel	SN74CBTLV3861PWR	CL861
	TVSOP – DGV	Tape and reel	SN74CBTLV3861DGVR	CL861

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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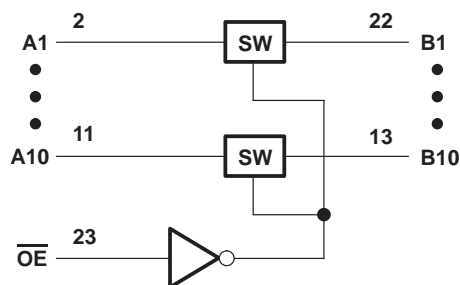
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# SN74CBTLV3861

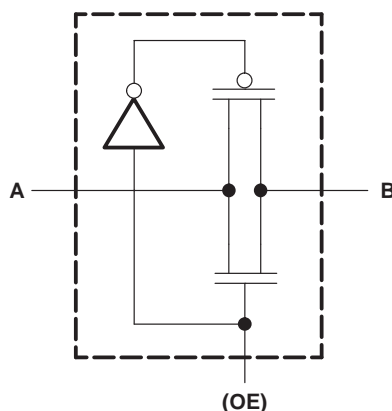
## LOW-VOLTAGE 10-BIT FET BUS SWITCH

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### logic diagram (positive logic)



### simplified schematic, each FET switch



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
NS package	65°C/W
PW package	88°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
$T_A$	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3 \text{ V}$ , $I_I = -18 \text{ mA}$				-1.2	V
$I_I$		$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC}$ or GND				±1	μA
$I_{off}$		$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to 3.6 V				10	μA
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND				10	μA
$\Delta I_{CC}‡$	Control inputs	$V_{CC} = 3.6 \text{ V}$ , One input at 3 V, Other inputs at $V_{CC}$ or GND				300	μA
$C_i$	Control inputs	$V_I = 3 \text{ V or } 0$				3	pF
$C_{iO(OFF)}$		$V_O = 3 \text{ V or } 0$ , $\overline{OE} = V_{CC}$				5	pF
$r_{on}§$	$V_{CC} = 2.3 \text{ V}$ , TYP at $V_{CC} = 2.5 \text{ V}$	$V_I = 0$	$I_I = 64 \text{ mA}$			5	Ω
			$I_I = 24 \text{ mA}$			5	
		$V_I = 1.7 \text{ V}$	$I_I = 15 \text{ mA}$			27	
	$V_{CC} = 3 \text{ V}$	$V_I = 0$	$I_I = 64 \text{ mA}$			5	
			$I_I = 24 \text{ mA}$			5	
		$V_I = 2.4 \text{ V}$	$I_I = 15 \text{ mA}$			10	

† All typical values are at  $V_{CC} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}¶$	A or B	B or A		0.15		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	2.1	5.5	2.1	4.9	ns
$t_{dis}$	$\overline{OE}$	A or B	1.7	5.5	2.5	5.8	ns

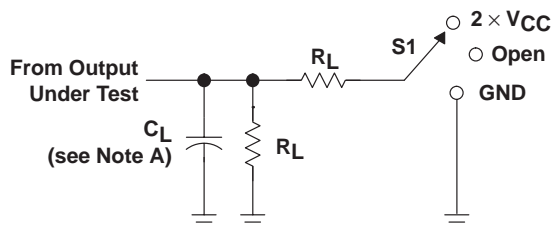
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

# SN74CBTLV3861

## LOW-VOLTAGE 10-BIT FET BUS SWITCH

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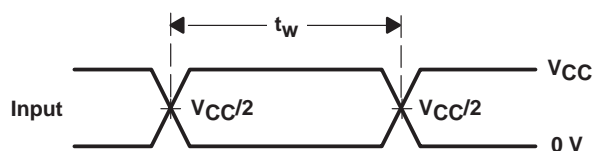
### PARAMETER MEASUREMENT INFORMATION



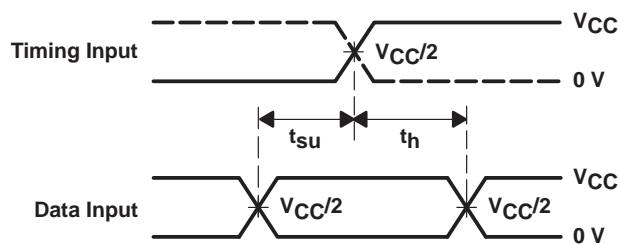
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

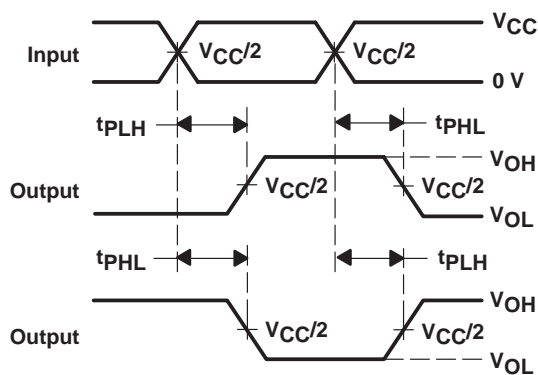
$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 $\Omega$	0.3 V



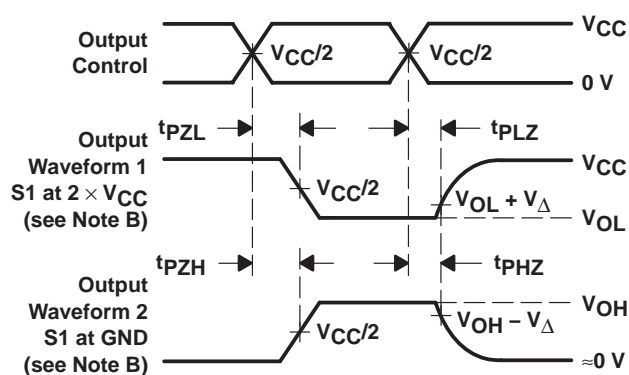
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV3861DBQRE4	ACTIVE	SSOP	DBQ	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861DBQRG4	ACTIVE	SSOP	DBQ	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861DGVRE4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861DGVRG4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861DWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861DWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861NSRG4	ACTIVE	SO	NS	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861PWRE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74CBTLV3861PWVG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74CBTLV3861DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3861	<a href="#">Samples</a>
SN74CBTLV3861DGV	OBSOLETE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		
SN74CBTLV3861DGVV	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL861	<a href="#">Samples</a>
SN74CBTLV3861DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3861	<a href="#">Samples</a>
SN74CBTLV3861DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3861	<a href="#">Samples</a>
SN74CBTLV3861NSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3861	<a href="#">Samples</a>
SN74CBTLV3861PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL861	<a href="#">Samples</a>
SN74CBTLV3861PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL861	<a href="#">Samples</a>
SN74CBTLV3861PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL861	<a href="#">Samples</a>
SN74CBTLV3861PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL861	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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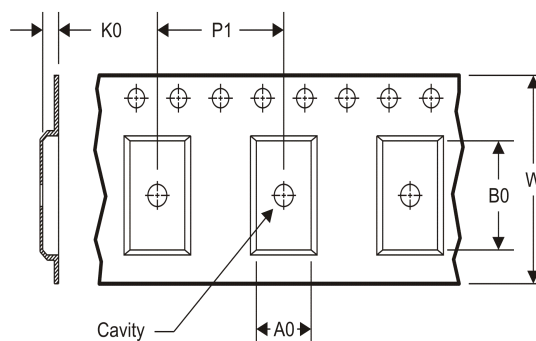
**OTHER QUALIFIED VERSIONS OF SN74CBTLV3861 :**

- Automotive: [SN74CBTLV3861-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


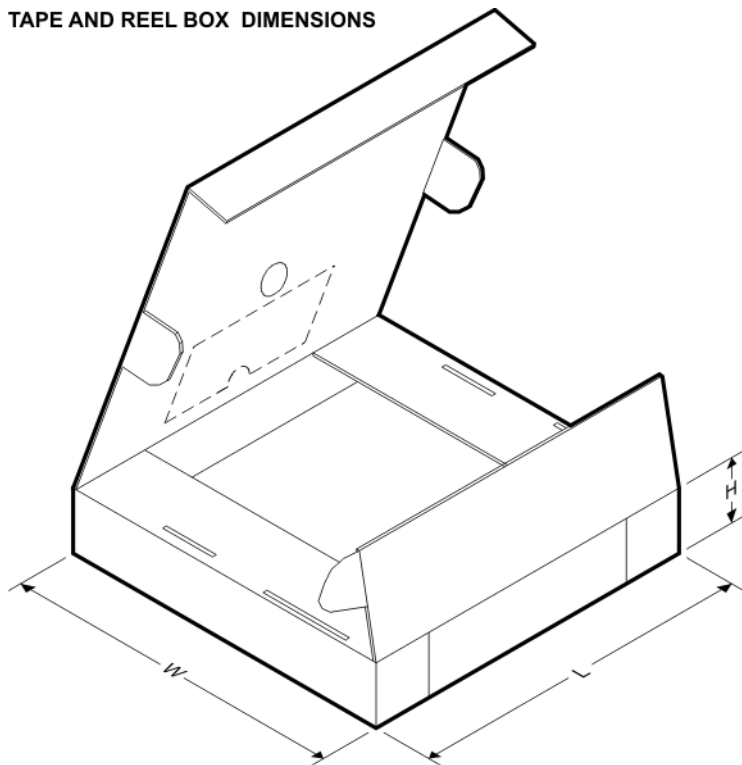
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3861DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3861DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3861DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTLV3861NSR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1
SN74CBTLV3861PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



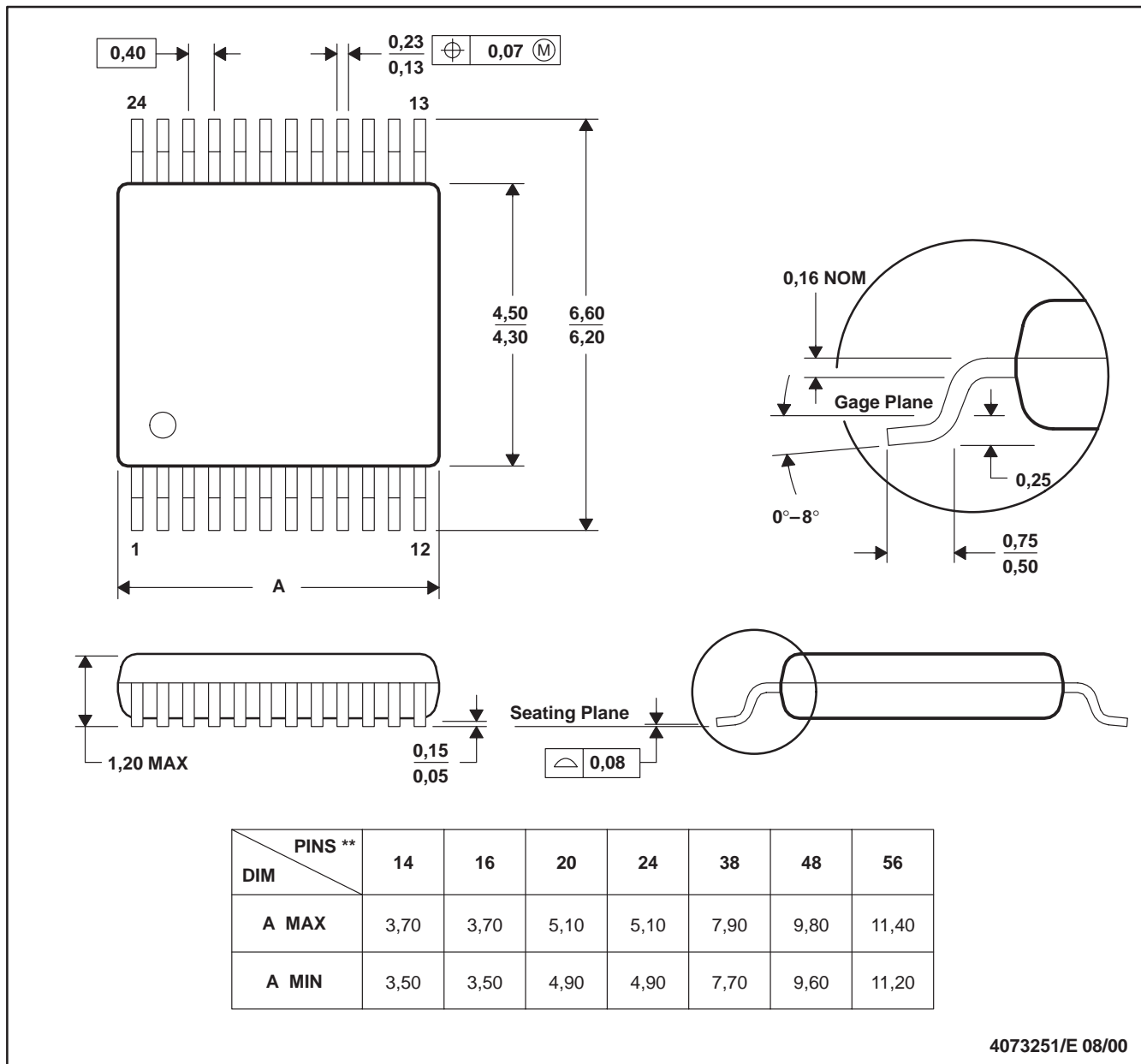
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3861DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74CBTLV3861DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74CBTLV3861DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74CBTLV3861NSR	SO	NS	24	2000	367.0	367.0	45.0
SN74CBTLV3861PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

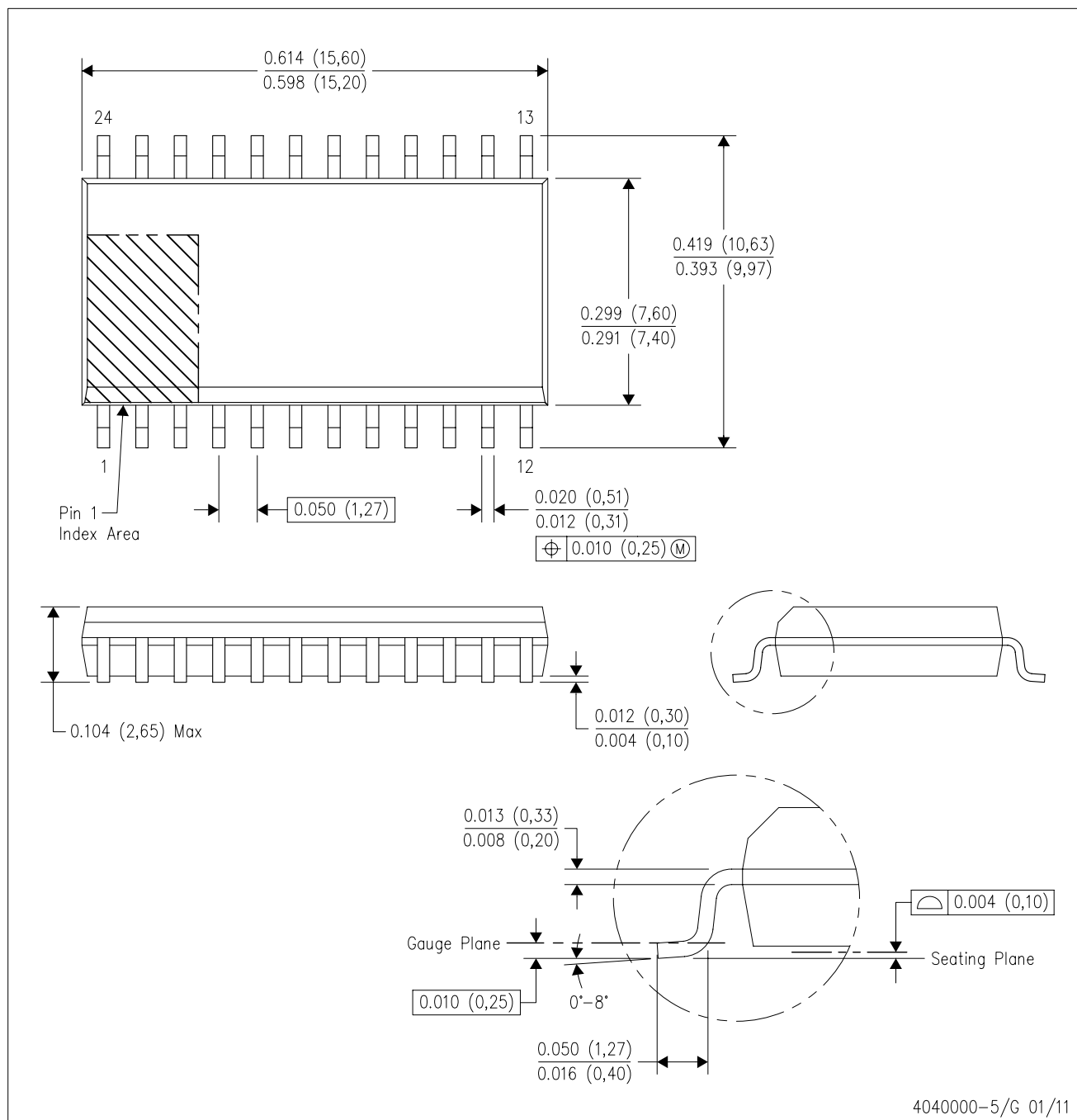
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

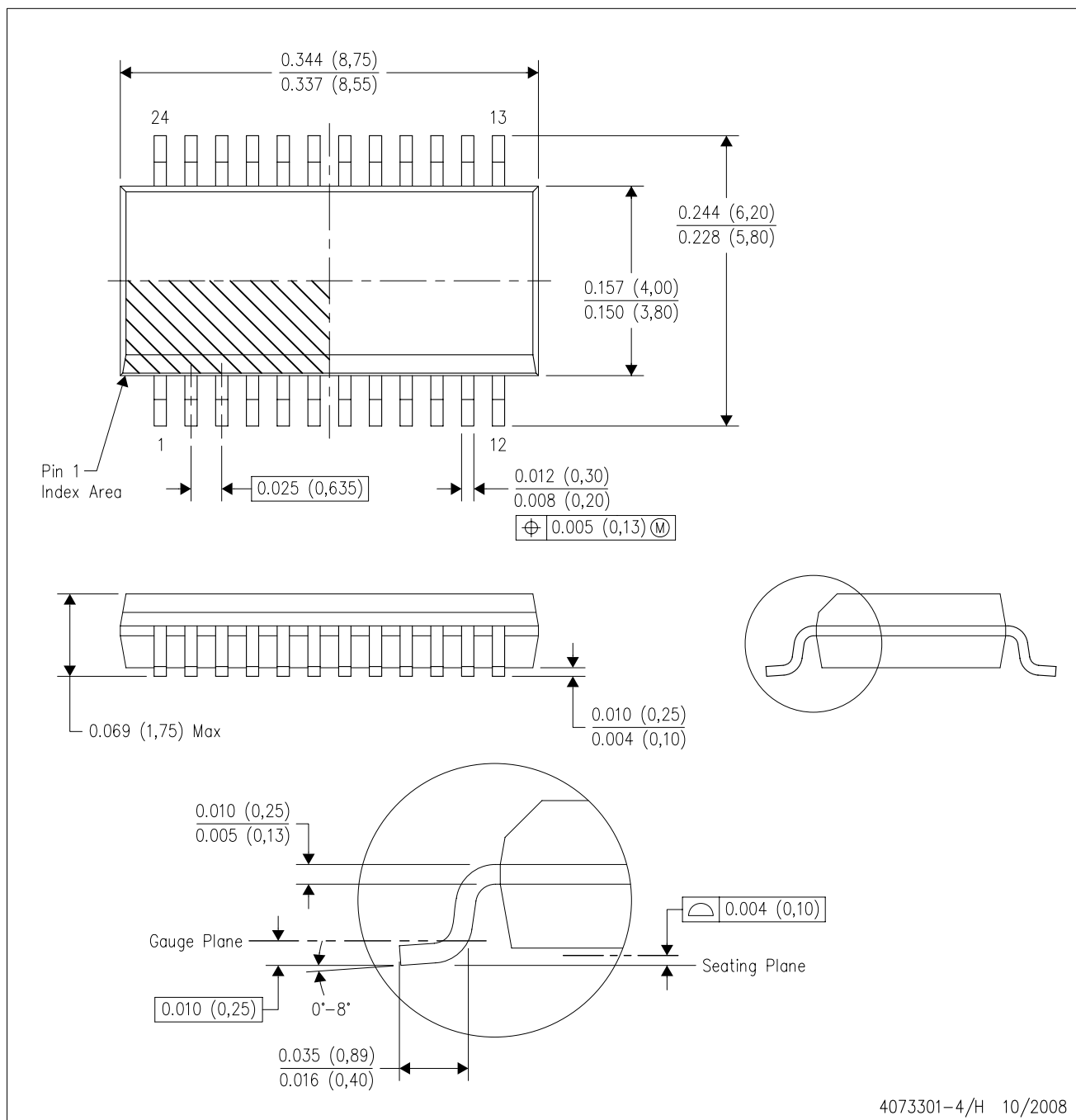


NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

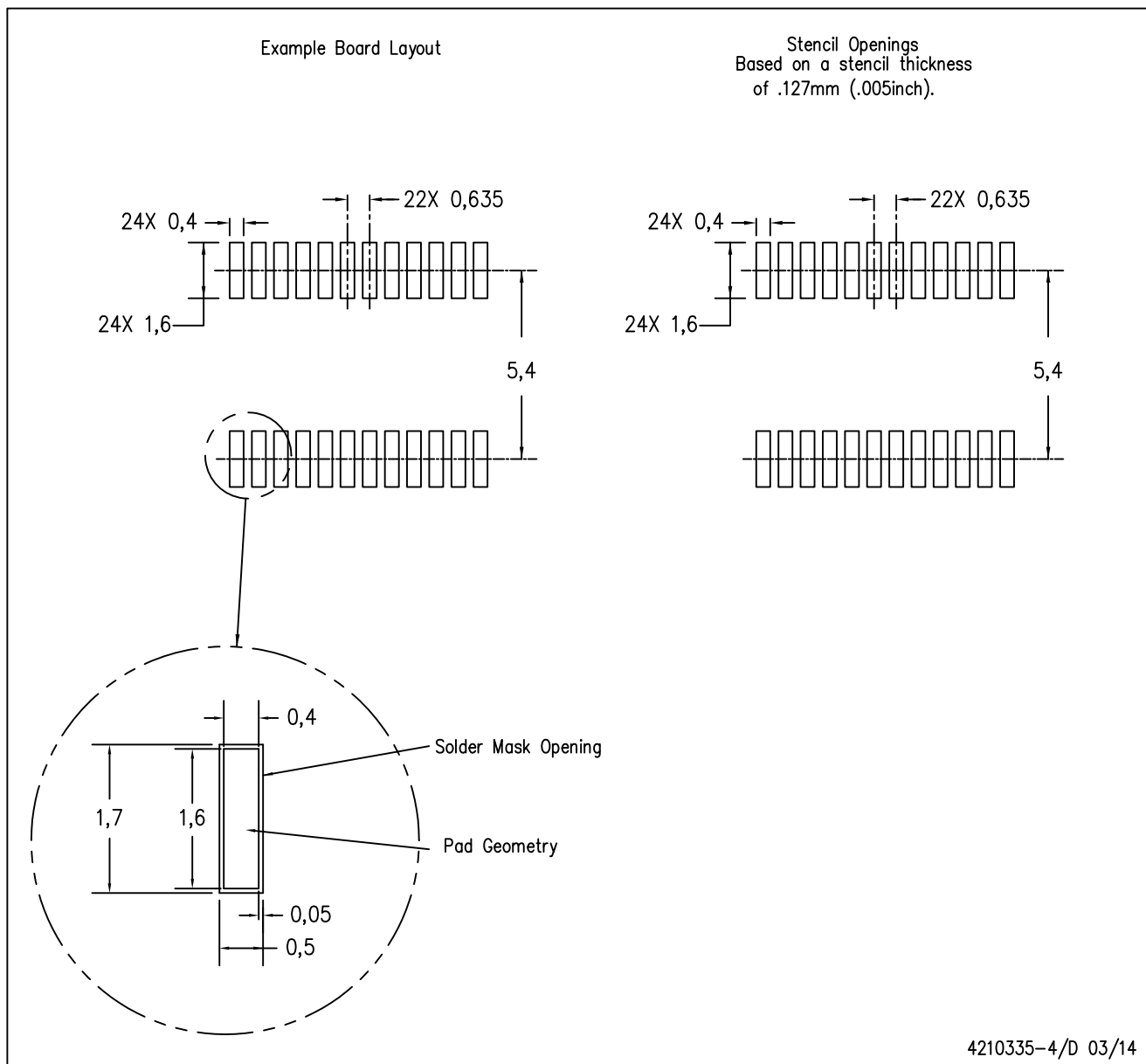
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

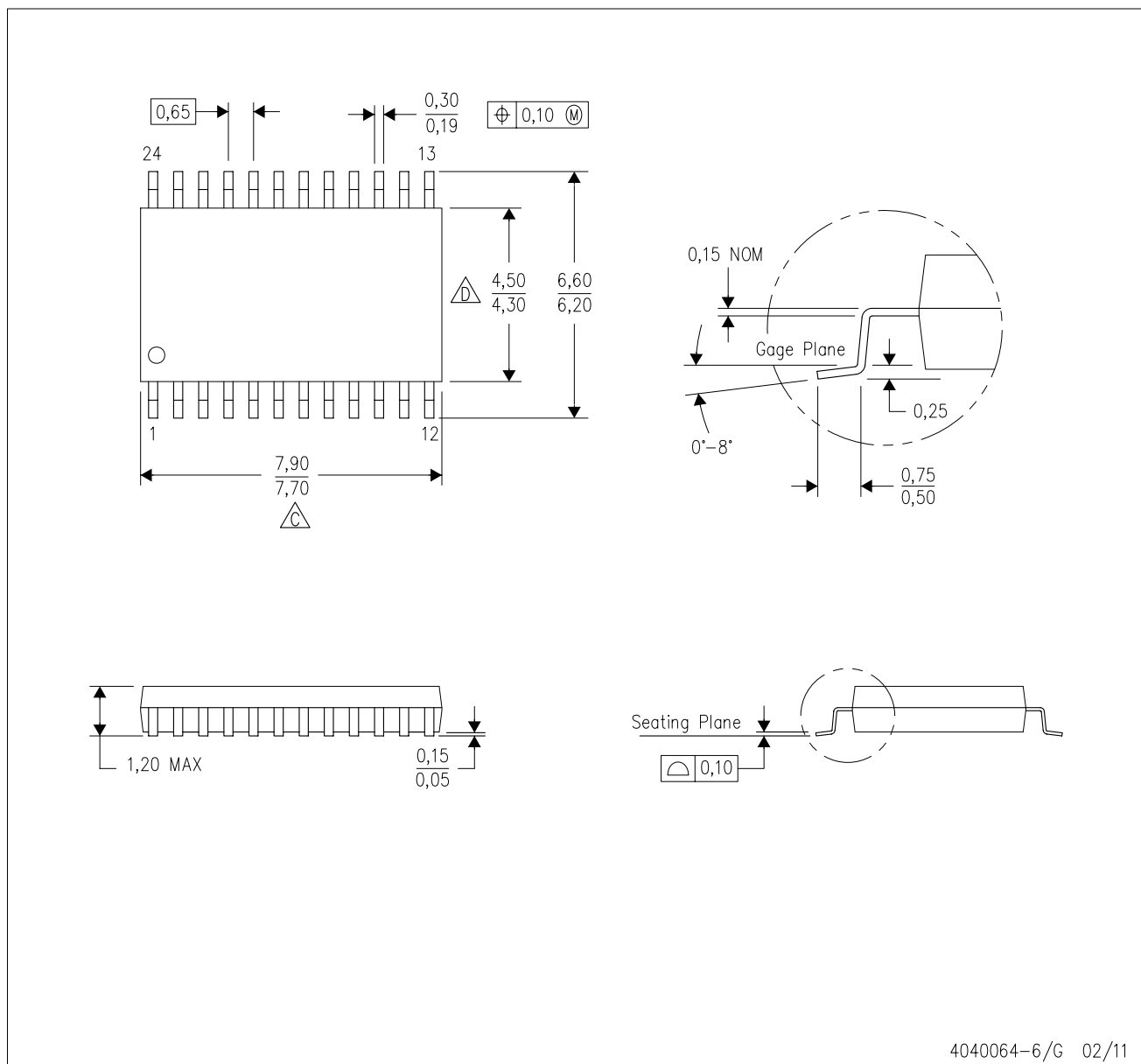
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G24)

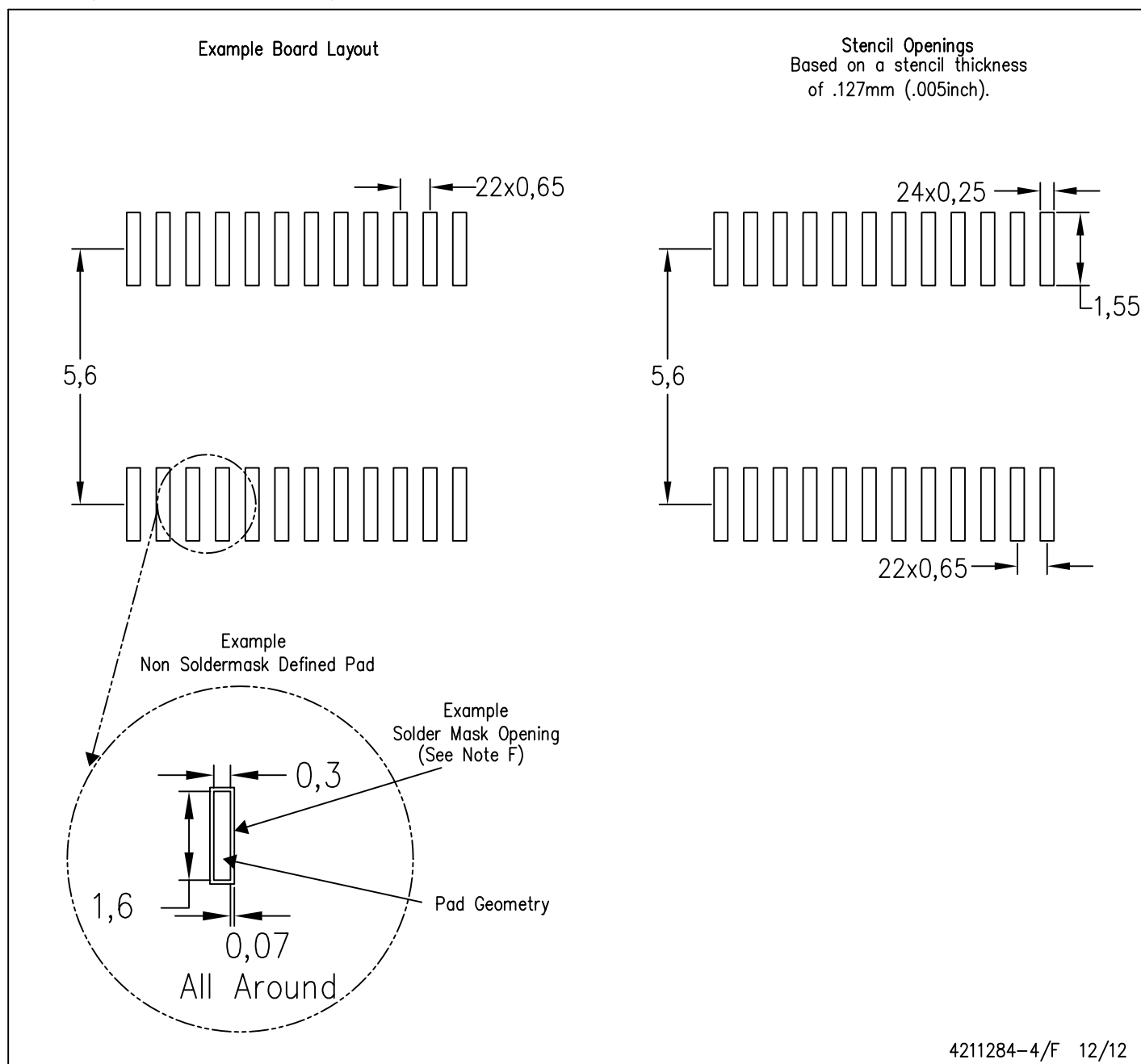
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



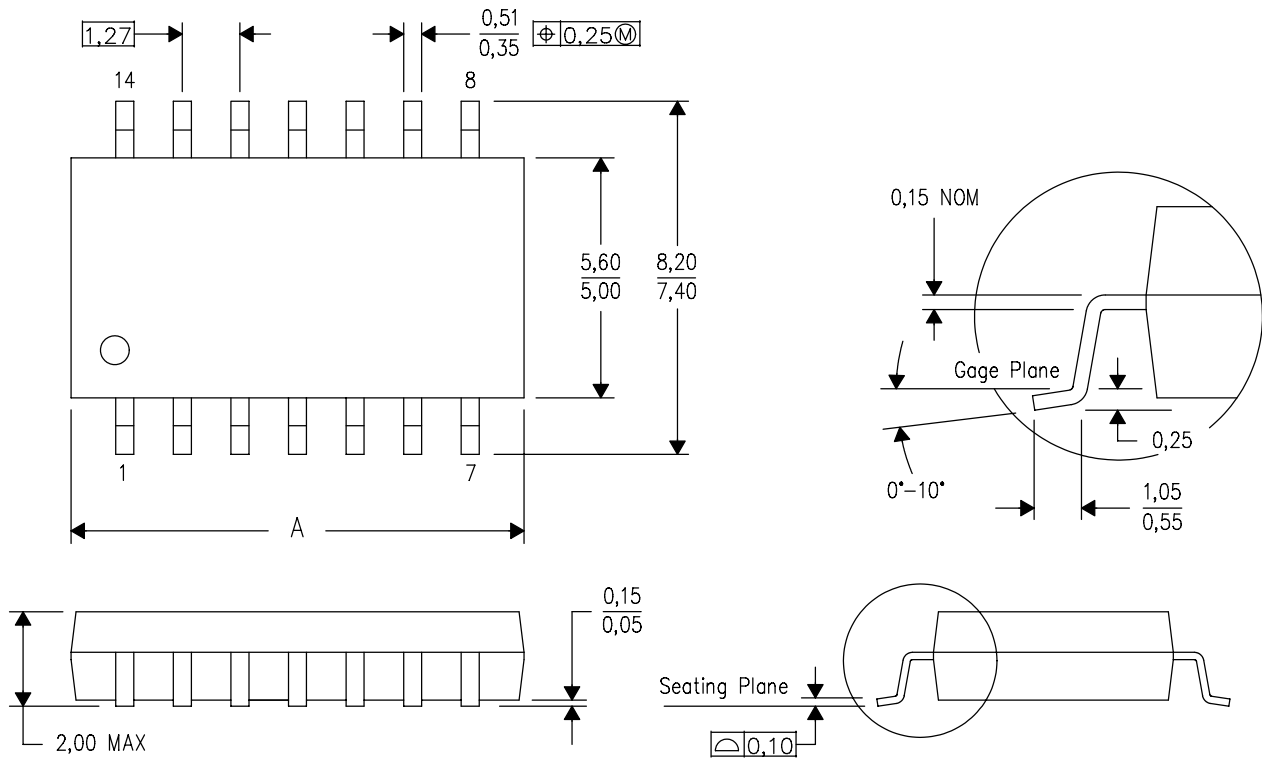
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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