



SY84113BU

Low Power 2.5V 1.25Gbps Limiting Post Amplifier with Ultra Wide LOS Range

General Description

The SY84113BU low power limiting post amplifier is designed for use in fiber-optic optical modules for multirate applications up to 1.25Gbps. The device connects to a typical transimpedance amplifier (TIA) and can produce output signals to CML-level waveforms. Intended for the GbE and Fibre Channel applications, the SY84113BU offers a wide loss-of-signal (LOS) range. It is able to detect input signals for as low as 5mVpp and as high as 100mVpp. The SY84113BU is intended to be used in AC-coupled input applications.

The SY84113BU generates a LOS open-collector TTL output. A programmable LOS level set pin (LOS_{LVL}) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOS_{LVL} and de-asserts low otherwise. The enable input (/EN) de-asserts the true output signal without removing the input signal. The LOS output can be fed back to the /EN input to implement the squelch function that maintains output stability under an LOS condition.

The SY84113BU operates on a single 2.5V power supply and offers ultra-low power consumption. This device is perfectly suited to meet the stringent power requirements of the CSFP/SFP/SFF optical modules.

All support documentation can be found on Micrel's website at: www.micrel.com.

Features

- Ultra-wide loss-of-signal (LOS) range (5mVpp to 100mVpp)
- Single 2.5V power supply
- Ultra-low power consumption (55mW typical)
- 125Mbps to 1.25 Gbps operation
- Low-noise CML data outputs
- TTL /EN input
- Programmable LOS level (LOS_{LVL})
- Internal 50 Ω termination
- Available in a tiny 3mm \times 3mm QFN package
- Extensive temperature range (-40°C to $+95^{\circ}\text{C}$)

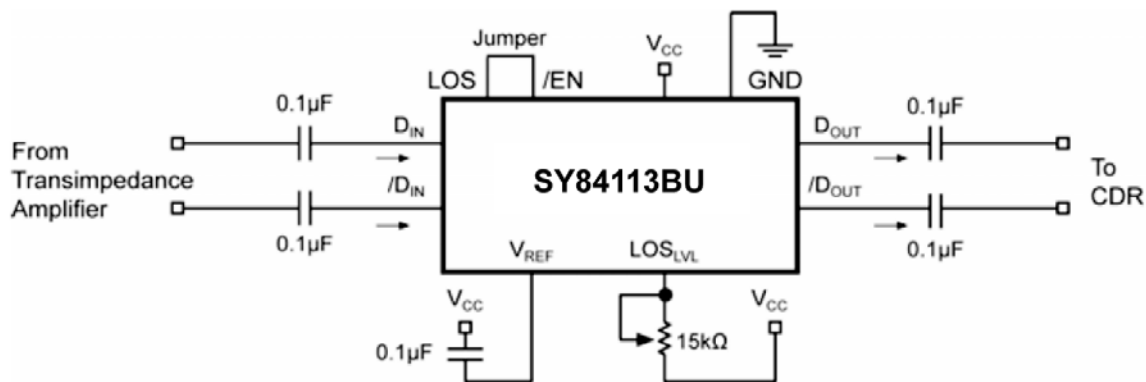
Applications

- Gigabit Ethernet
- Fibre Channel
- GEAPON

Markets

- Datacom/telecom
- Compact SFP/SFF optical transceiver
- SFP/SFF optical transceiver

Typical Application



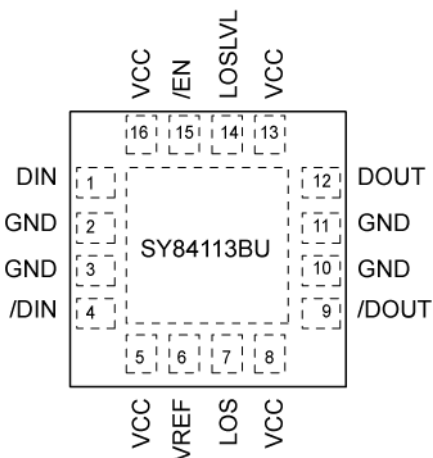
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY84113BUMG	QFN-16	Industrial	113B with Pb-Free Bar-Line Indicator	NiPdAu Pb-Free
SY84113BUMGTR ⁽¹⁾	QFN-16	Industrial	113B with Pb-Free Bar-Line Indicator	NiPdAu Pb-Free

Notes:

1. Tape and Reel.

Pin Configuration



16-Pin (3mm × 3mm) QFN-16

Pin Description

Pin Number	Pin Name	Type	Pin Function
15	/EN	TTL Input	/Enable: This input enables the outputs when LOW. Internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
1, 4	DIN, /DIN	Data Input	Differential data inputs. Each input is internally terminated to the VREF pin by a 50Ω resistor.
6	VREF		Reference Voltage: Place 0.1μF capacitor to Vcc to help stabilize LOSLVL.
14	LOSLVL	DC Input	Loss-of-Signal Level Set. A resistor from this pin to V _{CC} sets the threshold for the data input amplitude at which LOS will be asserted.
2, 3, 10, 11, ePad	GND	Ground	Device Ground. Exposed pad (ePad) must be connected to PCB ground plane.
7	LOS	Open-Collector TTL Output	Loss-of-signal: asserts high when the data input amplitude falls below the threshold set by LOS _{LVL} .
12, 9	/DOUT, DOUT	CML Output	Differential data outputs. Unused output should be terminated 50Ω to VCC.
5, 8, 13, 16	VCC	Positive Rail	Positive power supply. . Bypass with a 0.1μF 0.01μF low-ESR capacitor as close to VCC pin as possible.

Absolute Maximum Ratings⁽²⁾

Supply Voltage (V_{CC}) 0V to +4.0V
 Input Voltage (DIN, /DIN) 0 to V_{CC}
 Output Current (I_{OUT}) ± 25 mA
 EN Voltage 0 to V_{CC}
 V_{REF} Current $-800\mu A$ to $+500\mu A$
 LOS_{LVL} Voltage V_{REF} to V_{CC}
 Lead Temperature (soldering, 20s) 260°C
 Storage Temperature (T_s) $-65^\circ C$ to $+150^\circ C$

Operating Ratings⁽³⁾

Supply Voltage (V_{CC}) +2.375 to +2.625V
 Ambient Temperature (T_A) $-40^\circ C$ to $+95^\circ C$
 Junction Temperature (T_J) $-40^\circ C$ to $+120^\circ C$
 Package Thermal Resistance⁽⁴⁾
 (θ_{JA}) Still-Air 60°C/W
 (ψ_{JB}) 33°C/W

DC Electrical Characteristics

$V_{CC} = 2.5 \pm 5\%$; $T_A = -40^\circ C$ to $+95^\circ C$, typical values at $V_{CC} = 2.5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power Supply Current	Outputs terminated 50 Ω to V_{CC}		22	35	mA
LOS_{LVL}	LOS_{LVL} Voltage		V_{REF}		V_{CC}	V
V_{OH}	DOUT, /DOUT HIGH Voltage		$V_{CC} - 0.020$	$V_{CC} - 0.005$	V_{CC}	V
V_{OL}	DOUT, /DOUT LOW Voltage		$V_{CC} - 0.475$	$V_{CC} - 0.400$	$V_{CC} - 0.350$	V
V_{REF}	Reference Voltage			$V_{CC} - 0.6$		V
Z_0	Single-Ended Output Impedance		40	50	60	Ω
Z_I	Single-Ended Input Impedance		40	50	60	Ω

TTL DC Electrical Characteristics

$V_{CC} = 2.5 \pm 5\%$; $T_A = -40^\circ C$ to $+95^\circ C$, typical values at $V_{CC} = 2.5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	/EN Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	$V_{IN} = V_{CC}$			20	μA
I_{IL}	/EN Input LOW Current	$V_{IN} = 0.5V$	-0.3			mA
V_{OH}	LOS Output HIGH Level	$V_{CC} = 2.5V$. $I_{OH} < 50\mu A$	2			V
V_{OL}	LOS Output LOW Level	$I_{OL} = 2mA$			0.5	V

Notes:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. ψ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.

AC Electrical Characteristics

$V_{CC} = 2.5 \pm 5\%$; $T_A = -40^\circ\text{C}$ to $+95^\circ\text{C}$, typical values at $V_{CC} = 2.5\text{V}$, $T_A = 25^\circ\text{C}$; $R_{Load} = 50\Omega$ to V_{CC} ;

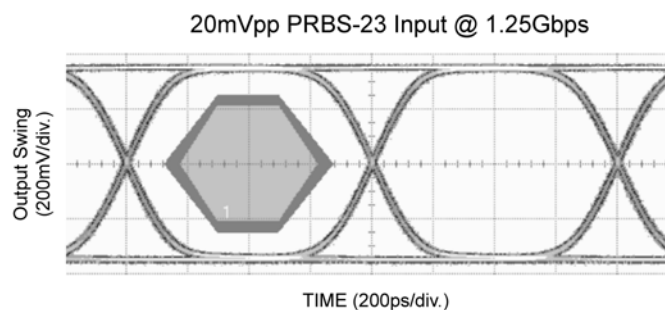
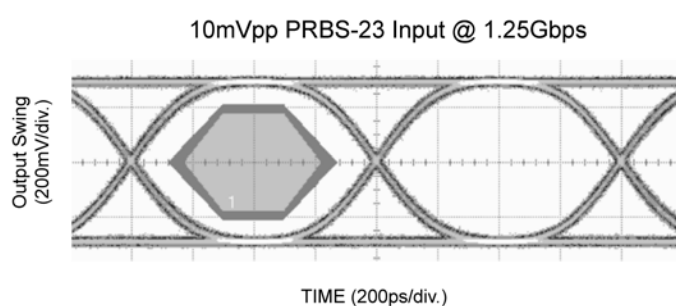
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 5		150	260	ps
t_{JITTER}	Deterministic Random	Note 6 Note 7		15 5		ps _{PP} ps _{RMS}
V_{ID}	Differential Input Voltage Swing		5		1800	mV _{PP}
V_{OD}	Differential Output Voltage Swing	Note 5	700	800	950	mV _{PP}
T_{OFF}	LOS Release Time	Note 10		2	10	μs
T_{ON}	LOS Assert Time	Note 10		2	10	μs
LOS_{AL}	Low LOS Assert Level	$R_{LOSLVL} = 10\text{k}\Omega^{(8)}$		3.9		mV _{PP}
LOS_{DL}	Low LOS De-assert Level	$R_{LOSLVL} = 10\text{k}\Omega^{(8)}$		5.6		mV _{PP}
HYS_L	Low LOS Hysteresis	$R_{LOSLVL} = 10\text{k}\Omega^{(8)}$	2	3.1	4.5	dB
LOS_{AM}	Medium LOS Assert Level	$R_{LOSLVL} = 5\text{k}\Omega^{(8)}$	7	9.2		mV _{PP}
LOS_{DM}	Medium LOS De-assert Level	$R_{LOSLVL} = 5\text{k}\Omega^{(8)}$		13.6	16	mV _{PP}
HYS_M	Medium LOS Hysteresis	$R_{LOSLVL} = 5\text{k}\Omega^{(9)}$	2	3.4	4.5	dB
LOS_{AH}	High LOS Assert Level	$R_{LOSLVL} = 100\Omega^{(8)}$	60	73		mV _{PP}
LOS_{DH}	High LOS De-assert Level	$R_{LOSLVL} = 100\Omega^{(8)}$		103	130	mV _{PP}
HYS_H	High LOS Hysteresis	$R_{LOSLVL} = 100\Omega^{(9)}$	2	3.0	4.5	dB
B_{3dB}	3dB Bandwidth			850		MHz
$A_{V(Diff)}$	Differential Voltage Gain			38		dB
S_{21}	Single-Ended Small-Signal Gain		26	32		dB

Notes:

- Amplifier in limiting mode. Input is a 200MHz square wave.
- Deterministic jitter measured using 1.250 Gbps K28.5 pattern, $V_{ID} = 60\text{mV}_{PP}$.
- Random jitter measured using 1.250Gbps K28.7 pattern, $V_{ID} = 60\text{mV}_{PP}$.
- See "Typical Operating Characteristics" for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.
- This specification defines electrical hysteresis as $20\log(\text{LOS De-Assert/LOS Assert})$. The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-4.5 dB, shown in the AC characteristics table, will be 1dB-3dB Optical Hysteresis.
- In real world applications, the LOS Release/Assert time can be strongly influenced by the RC time constant of the AC-coupling cap and the 50 Ω input termination. To keep this time low, use a decoupling cap with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001 μF to 1.0 μF).

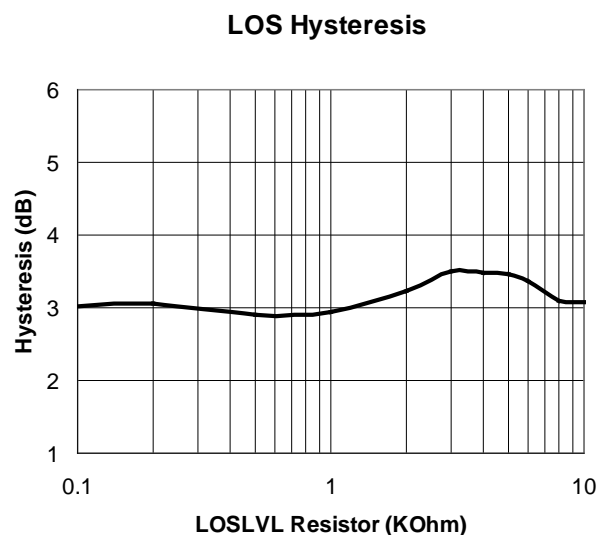
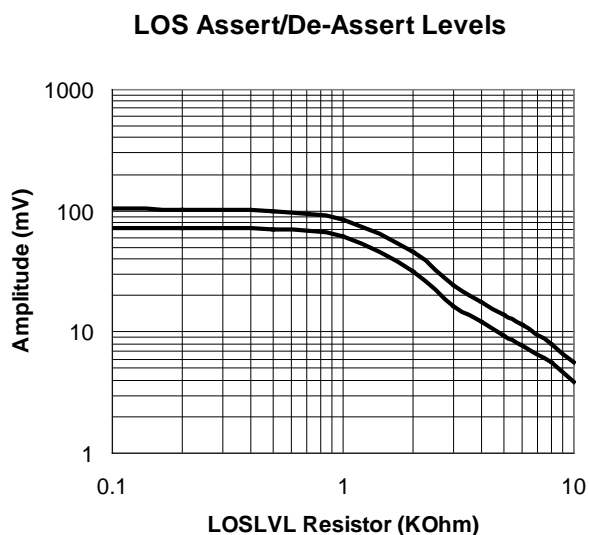
Typical Functional Characteristics

$V_{CC} = 2.5 \pm 5\%$; $T_A = -40^\circ\text{C}$ to $+95^\circ\text{C}$, typical values at $V_{CC} = 2.5\text{V}$, $T_A = 25^\circ\text{C}$.; $R_{Load} = 50\Omega$ to V_{CC} .

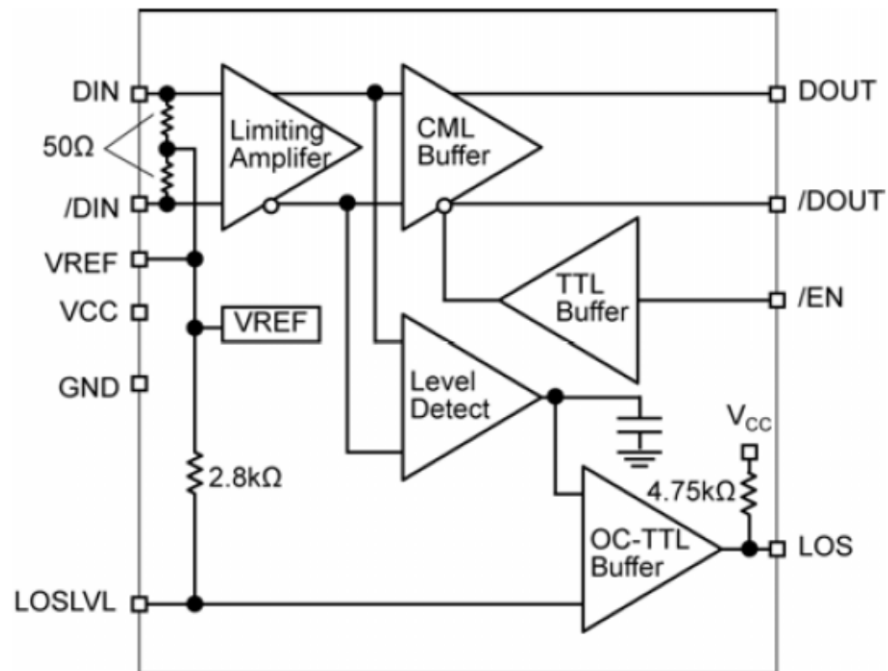


Typical Operating Characteristics

$V_{CC} = 2.5 \pm 5\%$; $T_A = -40^\circ\text{C}$ to $+95^\circ\text{C}$, typical values at $V_{CC} = 2.5\text{V}$, $T_A = 25^\circ\text{C}$.; $R_{Load} = 50\Omega$ to V_{CC} .



Functional Block Diagram



Functional Description

The SY84113BU is a high-sensitivity limiting post amplifier that operates from a single +2.5V power supply over temperatures from -40°C to $+85^{\circ}\text{C}$. Signals with data rates up to 1.25Gbps, and as small as 5mVpp, can be amplified. Figure 1 shows the allowed input voltage swing. The SY84113BU generates a LOS output signal that can be fed back to /EN for output stability in the absence of a signal at the input. LOS_{LVL} sets the sensitivity of the input amplitude detection. SY84113BU offers ultra wide LOS detection range. This allows the device to be used in multiple AC-coupled applications.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier can detect and amplify AC-coupled signals as small as 5mV_{pp} to full CML output level. The input stage also can allow signals as large as 1800mV_{pp}. Input signals are amplified with a typically 38dB differential voltage gain until they reach the limiting mode of the amplifier. SY84113BU outputs in standard 400mV CML output levels.

Output Buffer

The SY84113BU's CML output buffer is designed to drive 50Ω lines and is internally terminated with 50Ω to VCC. Figure 3 shows a schematic of the output stage.

Loss-of-Signal (LOS)

The SY84113BU generates a chatter-free LOSs-of-signal (LOS) open-collector TTL output as shown in Figure 4. LOS is used to determine that the input amplitude is too small to be considered as a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a LOSs of signal condition. /EN de-asserts low the true output signal without removing the input signals. Typically, 3dB LOS hysteresis is provided to prevent chattering.

LOS Level Set

A programmable LOS level set pin (LOS_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOS_{LVL} sets the voltage at LOS_{LVL} . This voltage ranges from V_{CC} to VREF. The external resistor creates a voltage divider between V_{CC} and VREF, as shown in Figure 5.

Hysteresis

The SY84113BU provides typically 3dB LOS electrical hysteresis, which is defined as $20\log(V_{\text{IN}_{\text{LOS-Assert}}} / V_{\text{IN}_{\text{LOS-De-Assert}}})$. Because the relationship between the voltage out of the ROSA to optical power at its input is linear, the optical hysteresis will be typically half of the electrical hysteresis reported in the datasheet, but in practice the ratio between electrical and optical hysteresis is found to be within the range 1.5 - 1.8. Thus 3dB electrical hysteresis will correspond to an optical hysteresis within the range 1.7dB - 2dB.

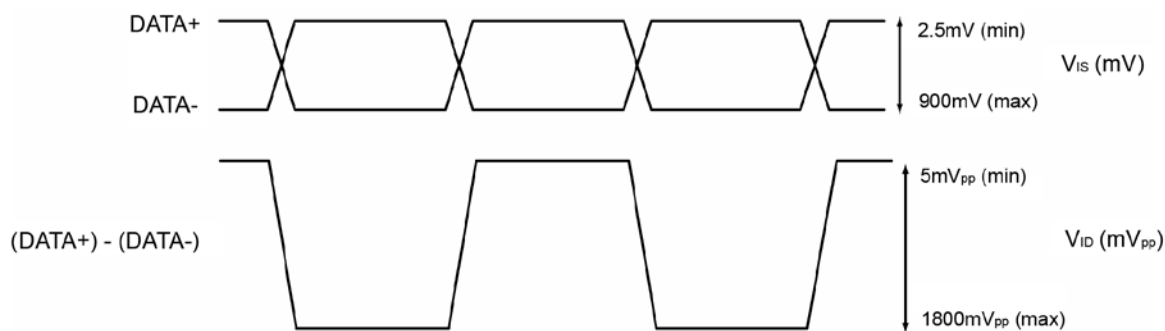


Figure 1. VIS and VID Definition

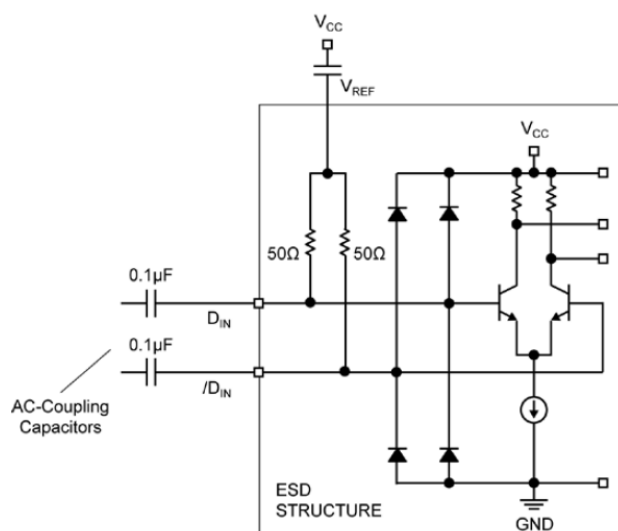


Figure 2. Input Structure

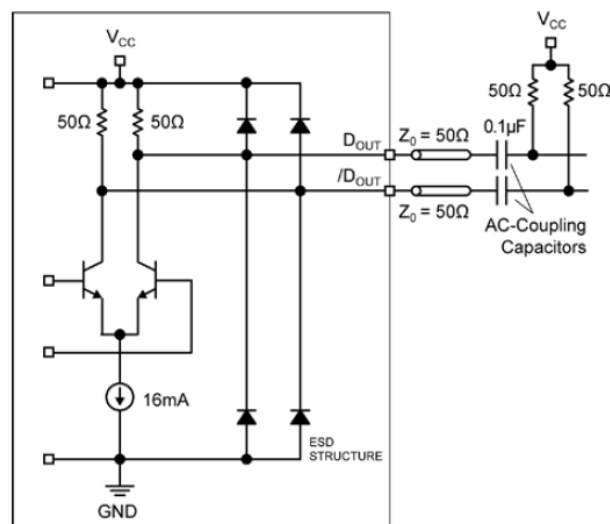


Figure 3. Output Structure

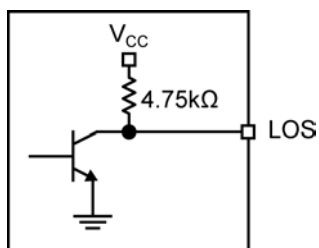
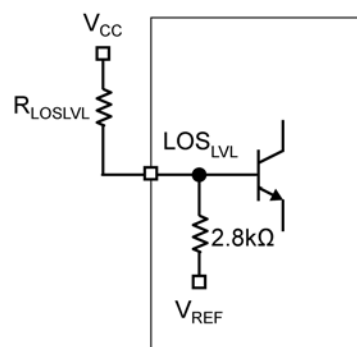
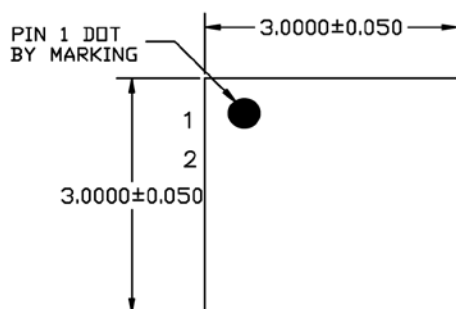


Figure 4. LOS Output Structure

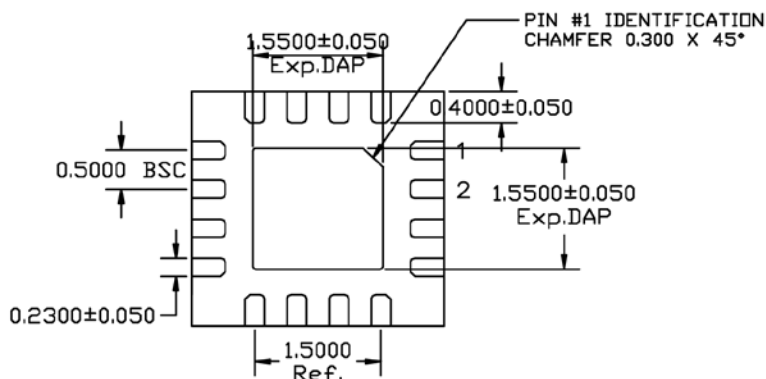
Figure 5. LOS_{LVL} Setting Circuit

Note: Recommended value for R_{LOSLVL} is $15k\Omega$ or less.

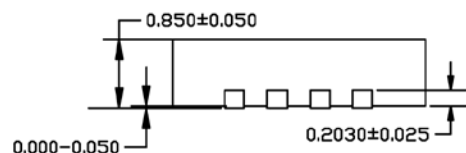
Package Information and Recommended Land Pattern⁽¹¹⁾



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3

NOTE:

1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

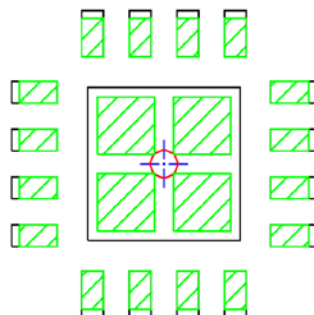
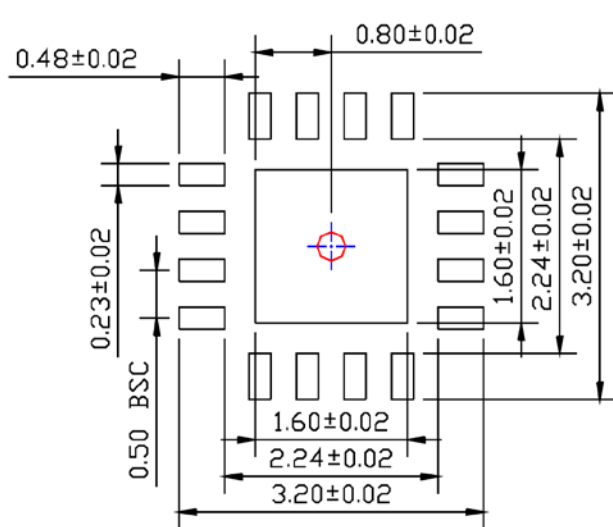
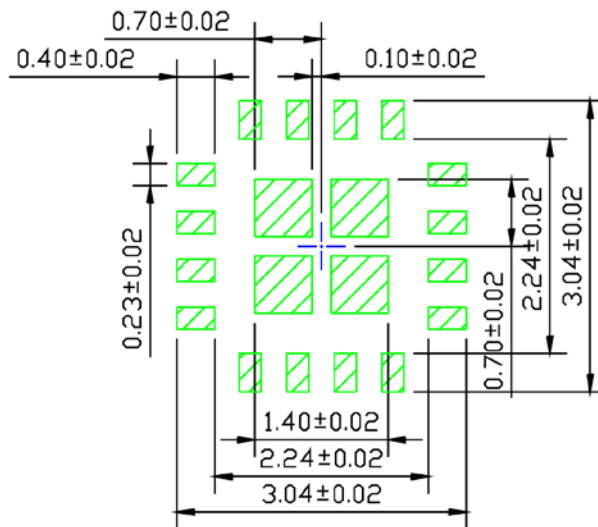
16-Pin (3mm x 3mm) QFN (QFN-16)

Note:

11. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Land Pattern⁽¹¹⁾ (Continued)RECOMMENDED LAND PATTERN

NOTE: 4, 5

STACKED-UPEXPOSED METAL TRACESOLDER STENCIL OPENING

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