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P1 98.2

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTORS

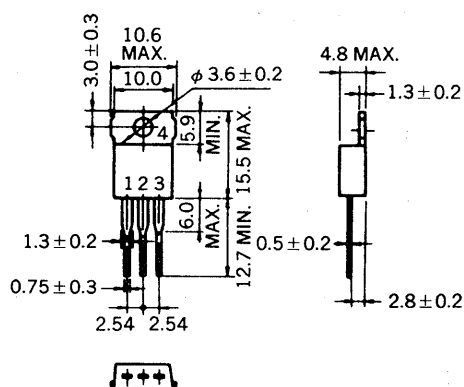
2SK1495, 2SK1495-Z/2SK1496, 2SK1496-Z

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

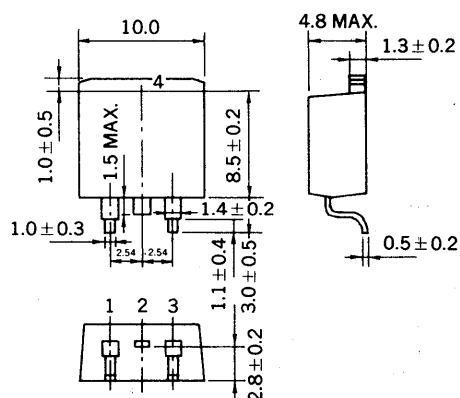
PACKAGE DIMENSIONS

(Unit: mm)

2SK1495.2SK1496

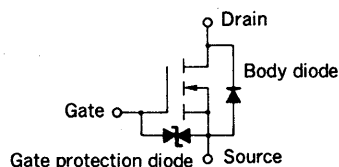


2SK1495-Z, 2SK1496-Z



PIN CONNECTIONS

1. Gate
2. Drain
3. Source
4. Fin (Drain)



DESCRIPTION

The 2SK1495/2SK1496 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.9 \Omega \text{ MAX.} / 1.0 \Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 4 \text{ A})$
- Low C_{iss} $C_{iss} = 1\,060 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	T _{stg}	−55 to +150	°C
Channel Temperature	T _{ch}	150	°C MAX.

Maximum Power Dissipation

Total Power Dissipation ($T_A = 25^\circ\text{C}$) P_T	70	W
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Maximum Voltages and Currents ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	450/500	V
		(2SK1495/2SK1496)	

Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 7	A
Drain Current (pulse)	$I_{D(pulse)}^*$	± 28	A

* $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

Maximum Avalanche Capability Ratings**

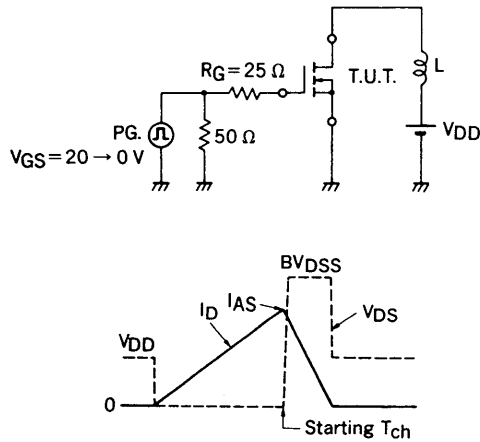
Single Avalanche Current	I_{AS}	10.5	A
Single Avalanche Energy	E_{AS}	206	mJ

**** Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25\ \Omega$, $V_{GS} = 20\text{ V} \rightarrow 0$**

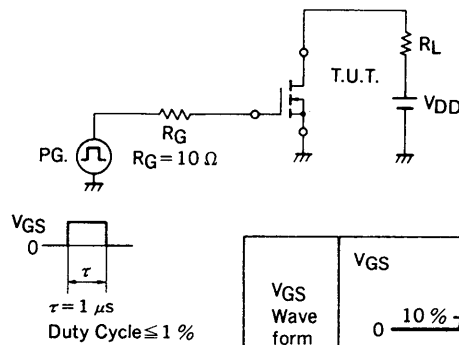
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1493/2SK1494)	$R_{DS(on)}$		0.7/0.8	0.9/1.0	Ω	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	3.0			S	$V_{DS} = 10\text{ V}, I_D = 4\text{ A}$
Drain Leakage Current	I_{DSS}			100	μA	$V_{DS} = 450\text{V}/500\text{V}, V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0$
Input Capacitance	C_{iss}		1 060		pF	$V_{DS} = 10\text{ V}$
Output Capacitance	C_{oss}		340		pF	$V_{GS} = 0$
Reverse Transfer Capacitance	C_{rss}		150		pF	$f = 1\text{ MHz}$
Turn-On Delay Time	$t_{d(on)}$		20		ns	$V_{GS} = 10\text{ V}$
Rise Time	t_r		30		ns	$V_{DD} = 150\text{ V}$
Turn-Off Delay Time	$t_{d(off)}$		70		ns	$I_D = 4\text{ A}, R_G = 10\ \Omega$
Fall Time	t_f		20		ns	$R_L = 37.5\ \Omega$
Total Gate Charge	Q_G		36		nC	$V_{GS} = 10\text{ V}$
Gate to Source Charge	Q_{GS}		7		nC	$I_D = 7\text{ A}$
Gate to Drain Charge	Q_{GD}		21		nC	$V_{DD} = 400\text{ V}$
Diode Forward Voltage	$V_F(S-D)$		1.0		V	$I_F = 7\text{ A}, V_{GS} = 0$
Reverse Recovery Time	t_{rr}		420		ns	$I_F = 7\text{ A}$
Reverse Recovery Charge	Q_{rr}		2.1		μC	$di/dt = 50\text{ A}/\mu\text{s}$

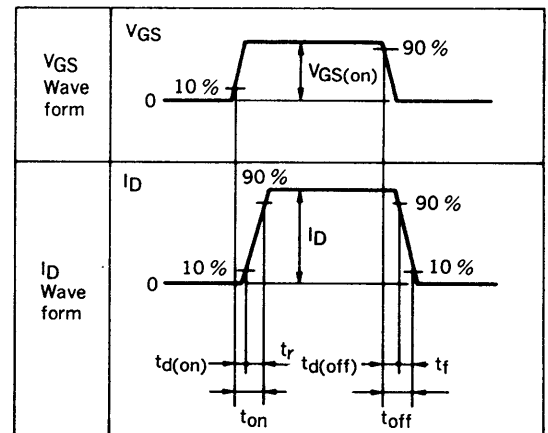
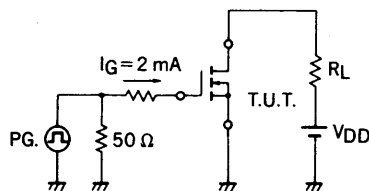
Test Circuit 1: Avalanche Capability



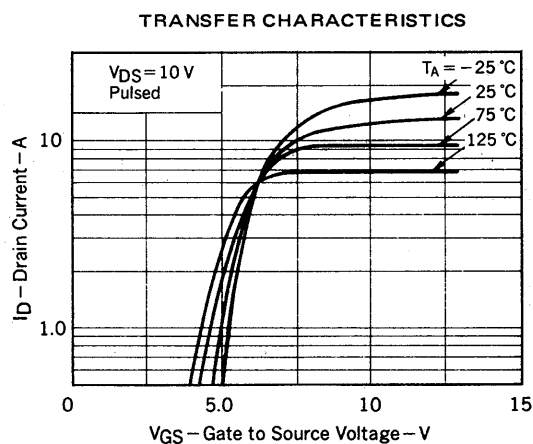
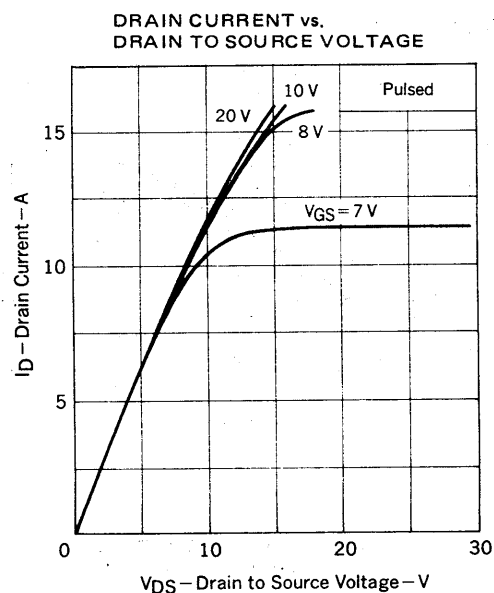
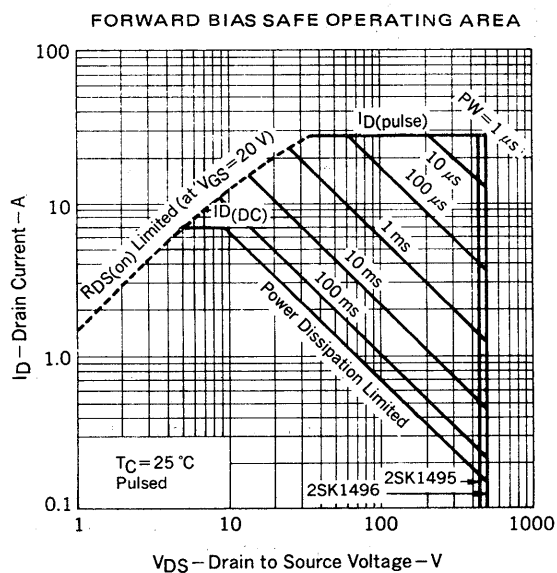
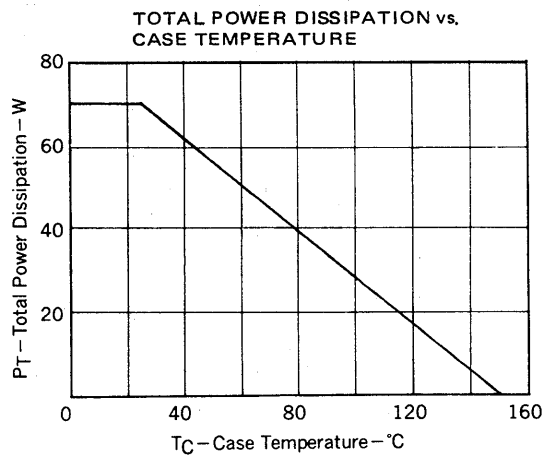
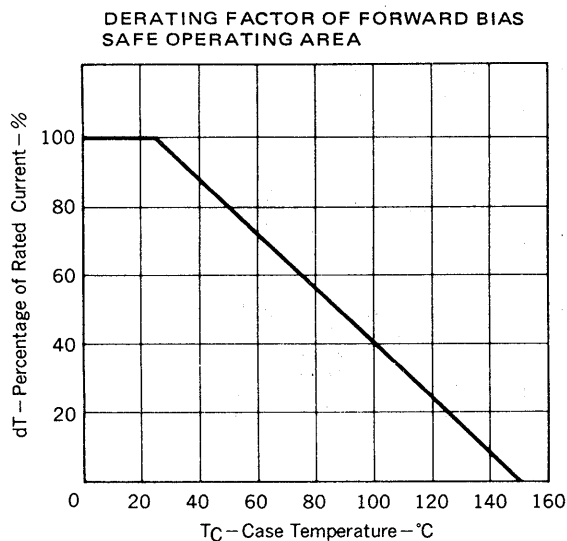
Test Circuit 2: Switching Time



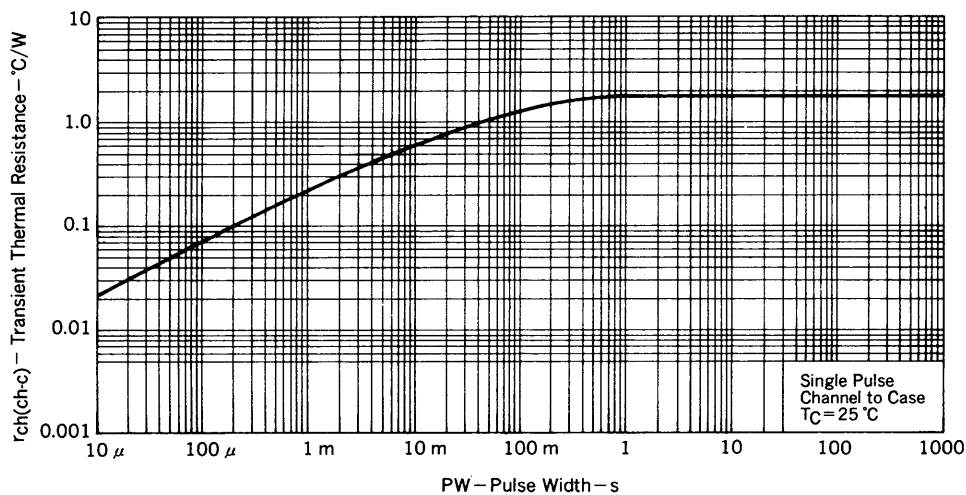
Test Circuit 3: Gate Charge



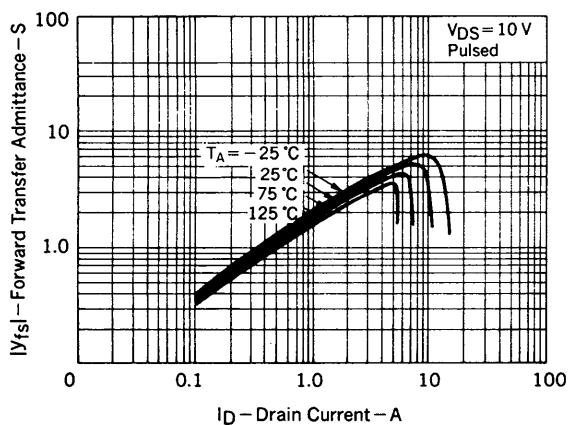
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



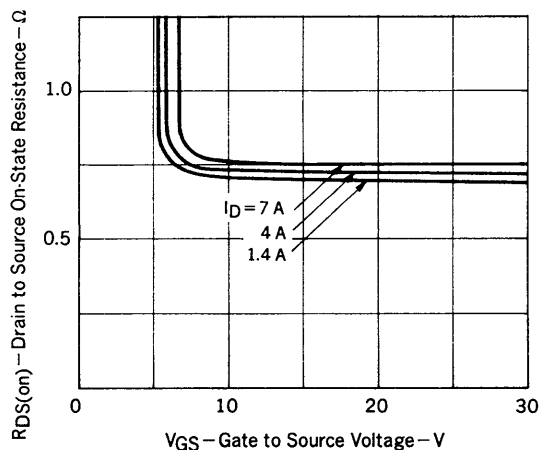
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



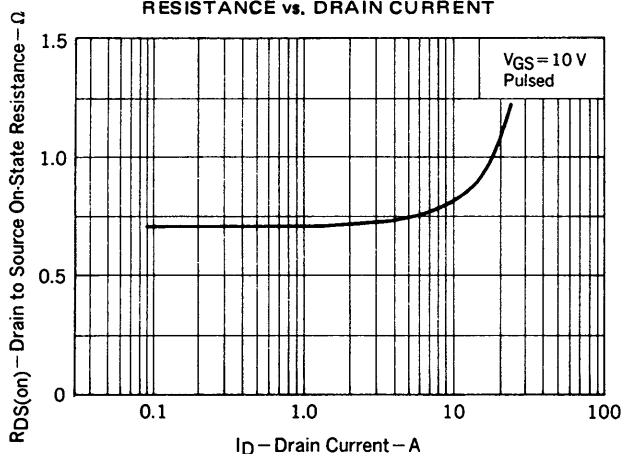
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



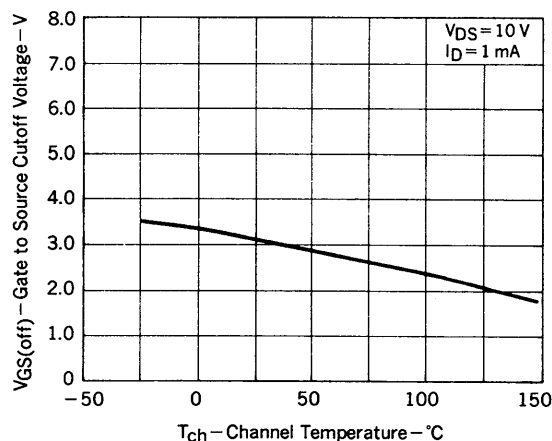
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

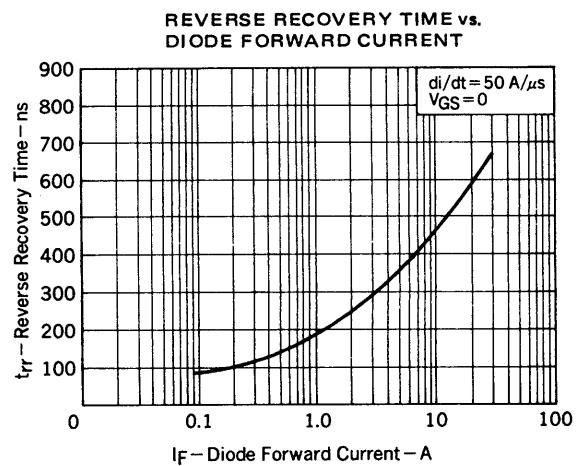
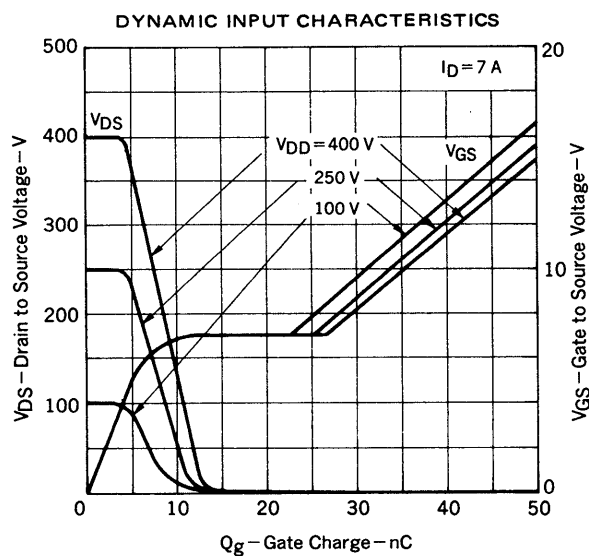
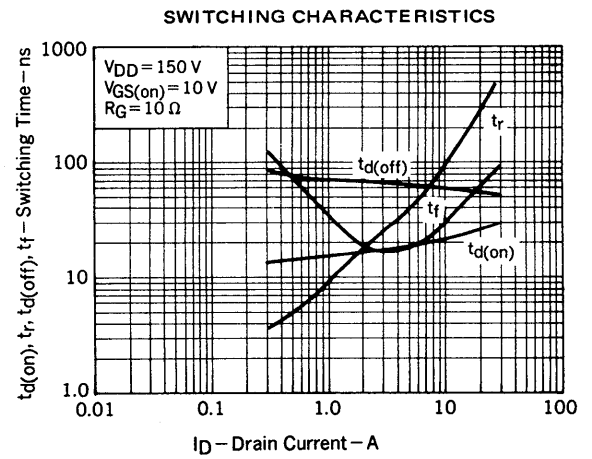
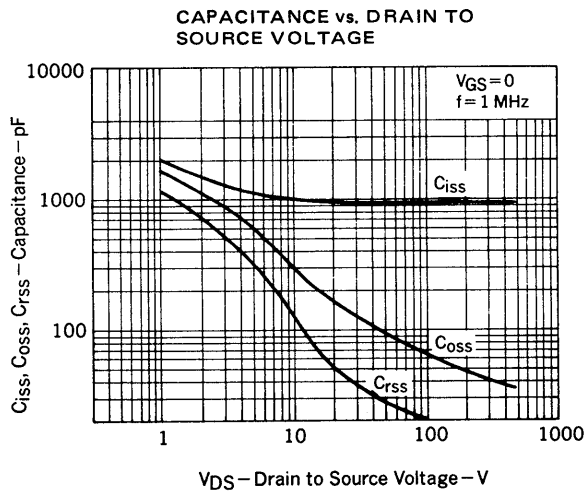
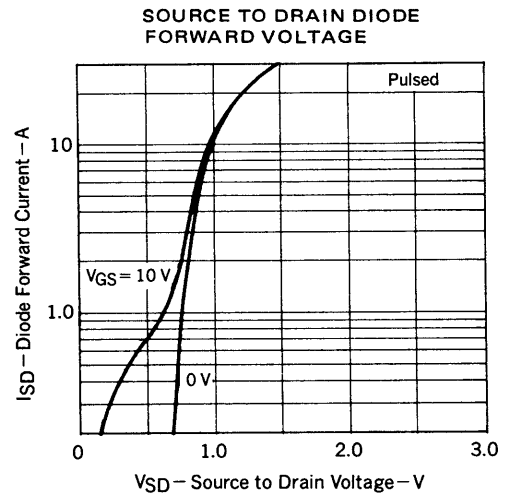
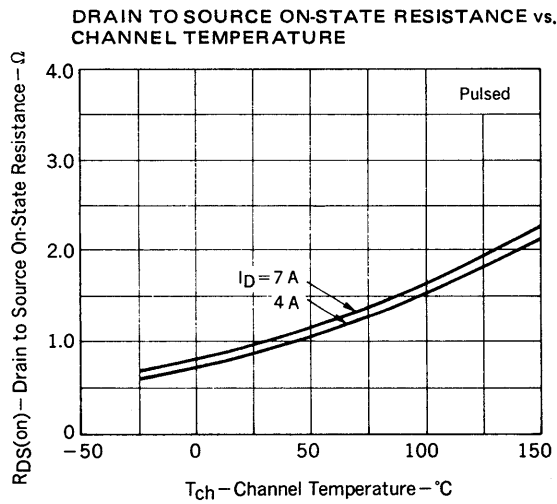


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

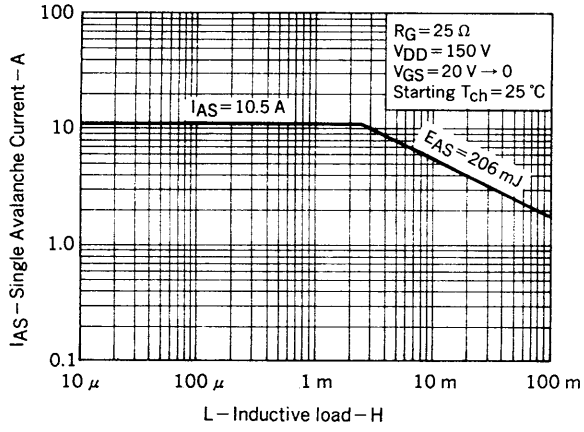


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

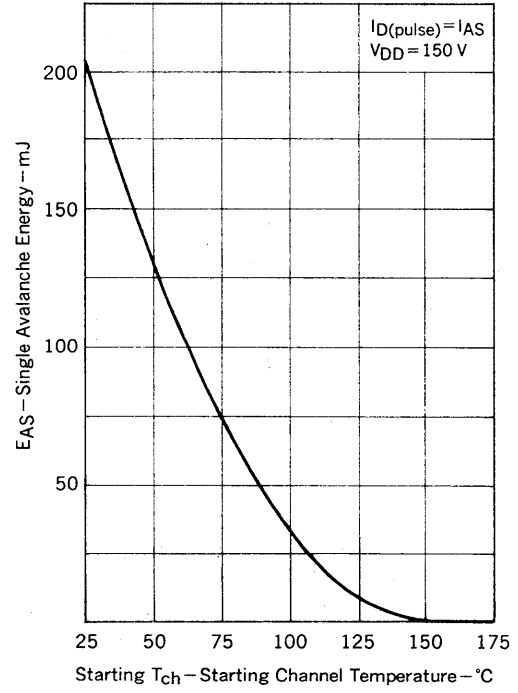




SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



REFERENCE

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1037
Application circuit using Power MOS FET.	TEA-1035
Guide to quality assurance for semiconductor device.	MEI-1202
Power MOS FET features and application switching power supply	TEA-1034

[MEMO]

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Anti-radioactive design is not implemented in this product.