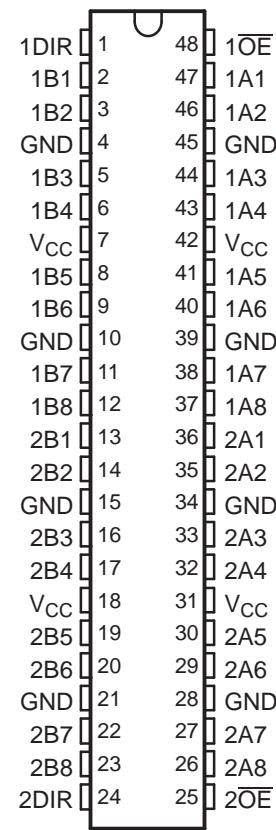


## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC16245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN74LVC16245A

## 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES0620—DECEMBER 1995—REVISED JANUARY 2008

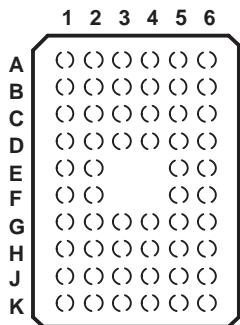
 **TEXAS  
INSTRUMENTS**  
www.ti.com

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Tape and reel	SN74LVC16245AGRDR	LD245A
	FBGA – ZRD (Pb-free)		SN74LVC16245AZRDR	
	SSOP – DL	Tube	SN74LVC16245ADL	LVC16245A
			SN74LVC16245ADLG4	
		Tape and reel	SN74LVC16245ADLR	
			SN74LVC16245ADLRG4	
	TSSOP – DGG	Tape and reel	SN74LVC16245ADGGR	LVC16245A
			74LVC16245ADGGRG4	
	TVSOP – DGV	Tape and reel	SN74LVC16245ADGVR	LD245A
			74LVC16245ADGVRE4	
	VFBGA – GQL	Tape and reel	SN74LVC16245AGQLR	LD245A
			SN74LVC16245AZQLR	

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).  
 (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

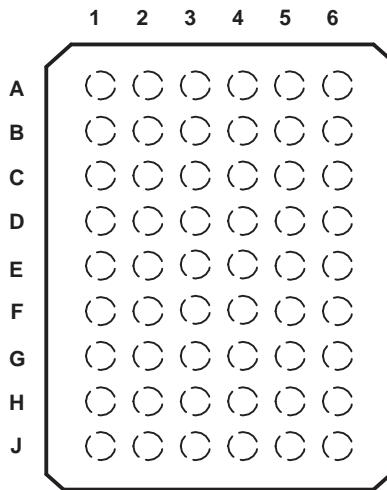


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	1OE
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	V <sub>CC</sub>	V <sub>CC</sub>	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2DIR	NC	NC	NC	NC	2OE

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

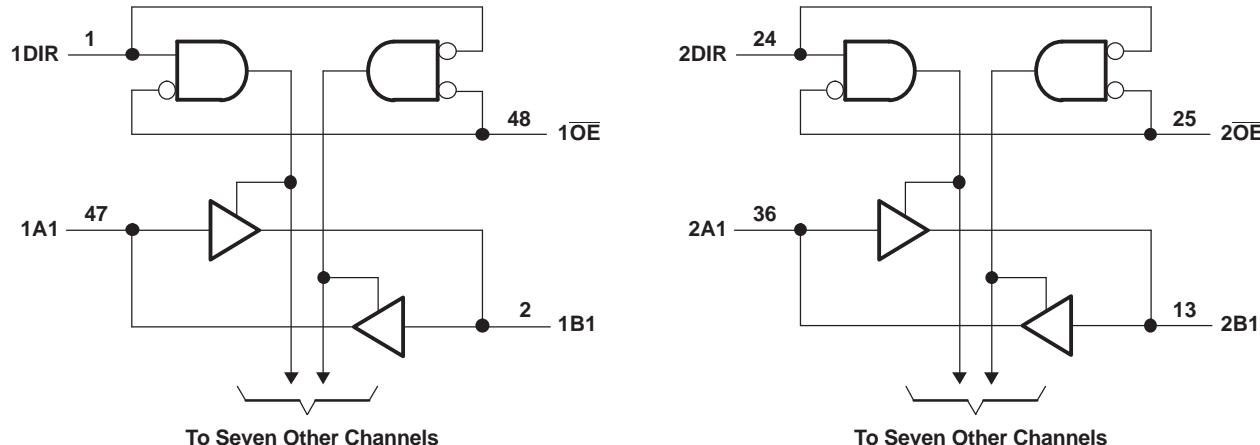
	1	2	3	4	5	6
<b>A</b>	1B1	NC	1DIR	1OE	NC	1A1
<b>B</b>	1B3	1B2	NC	NC	1A2	1A3
<b>C</b>	1B5	1B4	V <sub>CC</sub>	V <sub>CC</sub>	1A4	1A5
<b>D</b>	1B7	1B6	GND	GND	1A6	1A7
<b>E</b>	2B1	1B8	GND	GND	1A8	2A1
<b>F</b>	2B3	2B2	GND	GND	2A2	2A3
<b>G</b>	2B5	2B4	V <sub>CC</sub>	V <sub>CC</sub>	2A4	2A5
<b>H</b>	2B7	2B6	NC	NC	2A6	2A7
<b>J</b>	2B8	NC	2DIR	2OE	NC	2A8

(1) NC – No internal connection

**FUNCTION TABLE  
(EACH 8-BIT SECTION)**

INPUTS		OPERATION
<b>OE</b>	<b>DIR</b>	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG, DGV, and DL packages.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50 mA
$I_O$	Continuous output current			50 mA
Continuous current through each $V_{CC}$ or GND			100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
$T_{stg}$	Storage temperature range	-65	150	C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74LVC16245A**  
**16-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES0620—DECEMBER 1995—REVISED JANUARY 2008



**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		-4	mA
		V <sub>CC</sub> = 2.3 V		-8	
		V <sub>CC</sub> = 2.7 V		-12	
		V <sub>CC</sub> = 3 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 2.7 V		12	
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate			5	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA			1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V
	I <sub>OH</sub> = -4 mA			1.65 V	1.2			
	I <sub>OH</sub> = -8 mA			2.3 V	1.7			
	I <sub>OH</sub> = -12 mA			2.7 V	2.2			
	I <sub>OH</sub> = -24 mA			3 V	2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA			1.65 V to 3.6 V		0.2		V
	I <sub>OL</sub> = 4 mA			1.65 V		0.45		
	I <sub>OL</sub> = 8 mA			2.3 V		0.7		
	I <sub>OL</sub> = 12 mA			2.7 V		0.4		
	I <sub>OL</sub> = 24 mA			3 V		0.55		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V		3.6 V		±5	µA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0		±10	µA	
I <sub>OZ</sub> <sup>(2)</sup>		V <sub>O</sub> = 0 to 5.5 V		2.3 V to 3.6 V		±5	µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V			20		µA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(3)</sup>					20		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6, Other inputs at V <sub>CC</sub> or GND		2.3 V to 3.6 V			500	µA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		5	pF	
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		7.5	pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

(3) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

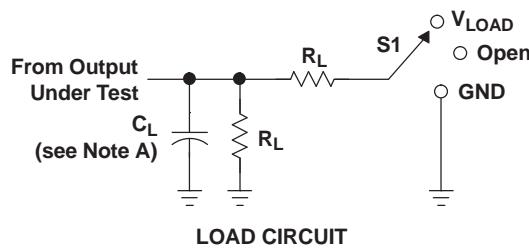
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1.5	7.1	1	4.5	1	4.7	1	4	ns
t <sub>en</sub>	OE	A or B	1.5	8.9	1	5.6	1.5	6.7	1.5	5.5	ns
t <sub>dis</sub>	OE	A or B	1.5	11.9	1	6.8	1.5	7.1	1.5	6.6	ns
t <sub>sk(o)</sub>										1	ns

## Operating Characteristics

T<sub>A</sub> = 25°C

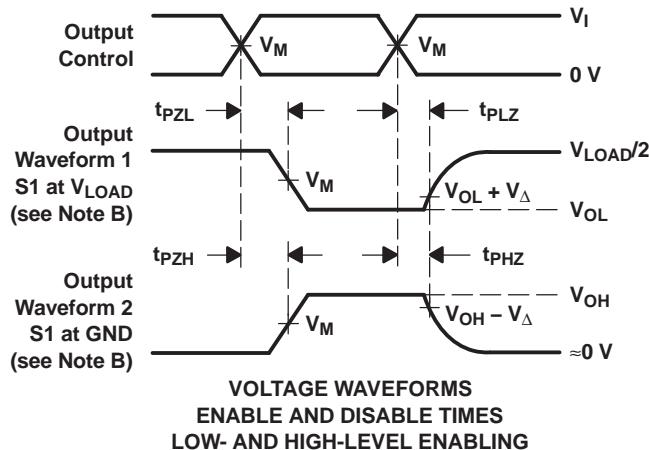
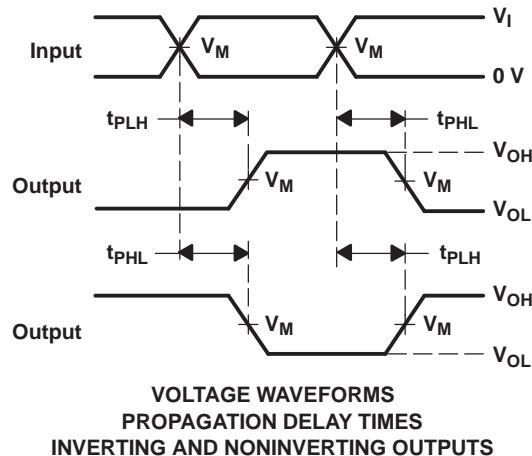
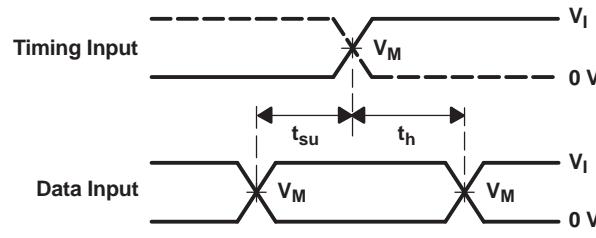
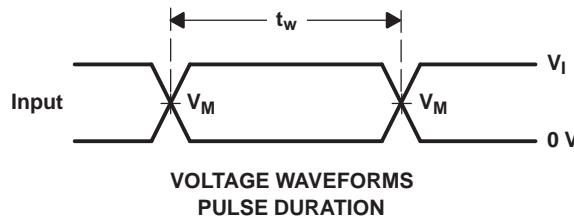
PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT	
		TYP	TYP	TYP		
C <sub>pd</sub>	Power dissipation capacitance per transceiver	f = 10 MHz	34	37	38	pF
			3	3	4	

### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74LVC16245ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC16245ADGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LD245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC16245ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LD245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LD245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245AGQLR	OBsolete	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	LD245A	
SN74LVC16245AGRDR	OBsolete	BGA MICROSTAR JUNIOR	GRD	54		TBD	Call TI	Call TI	-40 to 85	LD245A	
SN74LVC16245AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LD245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC16245AZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LD245A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

---

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

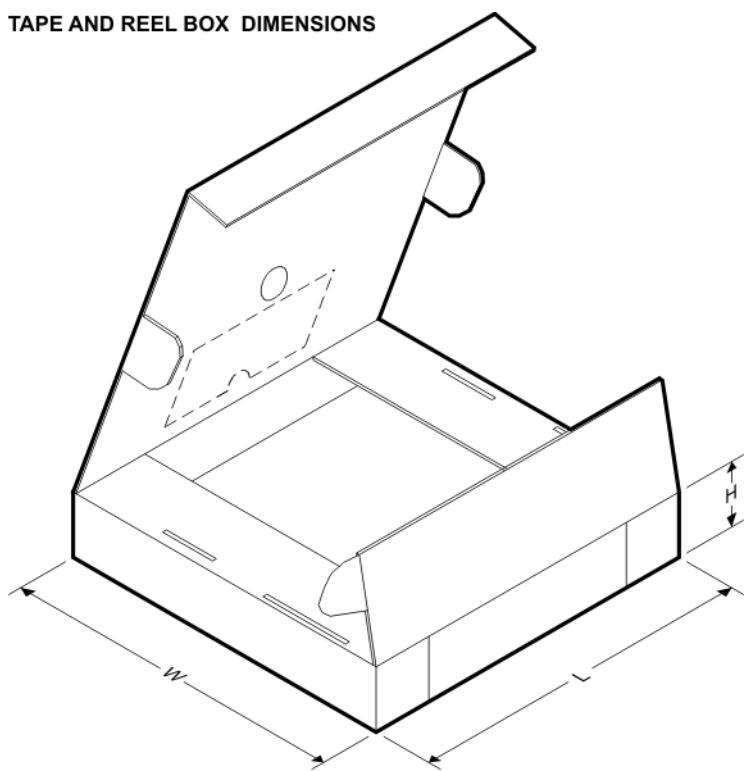
**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC16245ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVC16245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVC16245AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74LVC16245AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

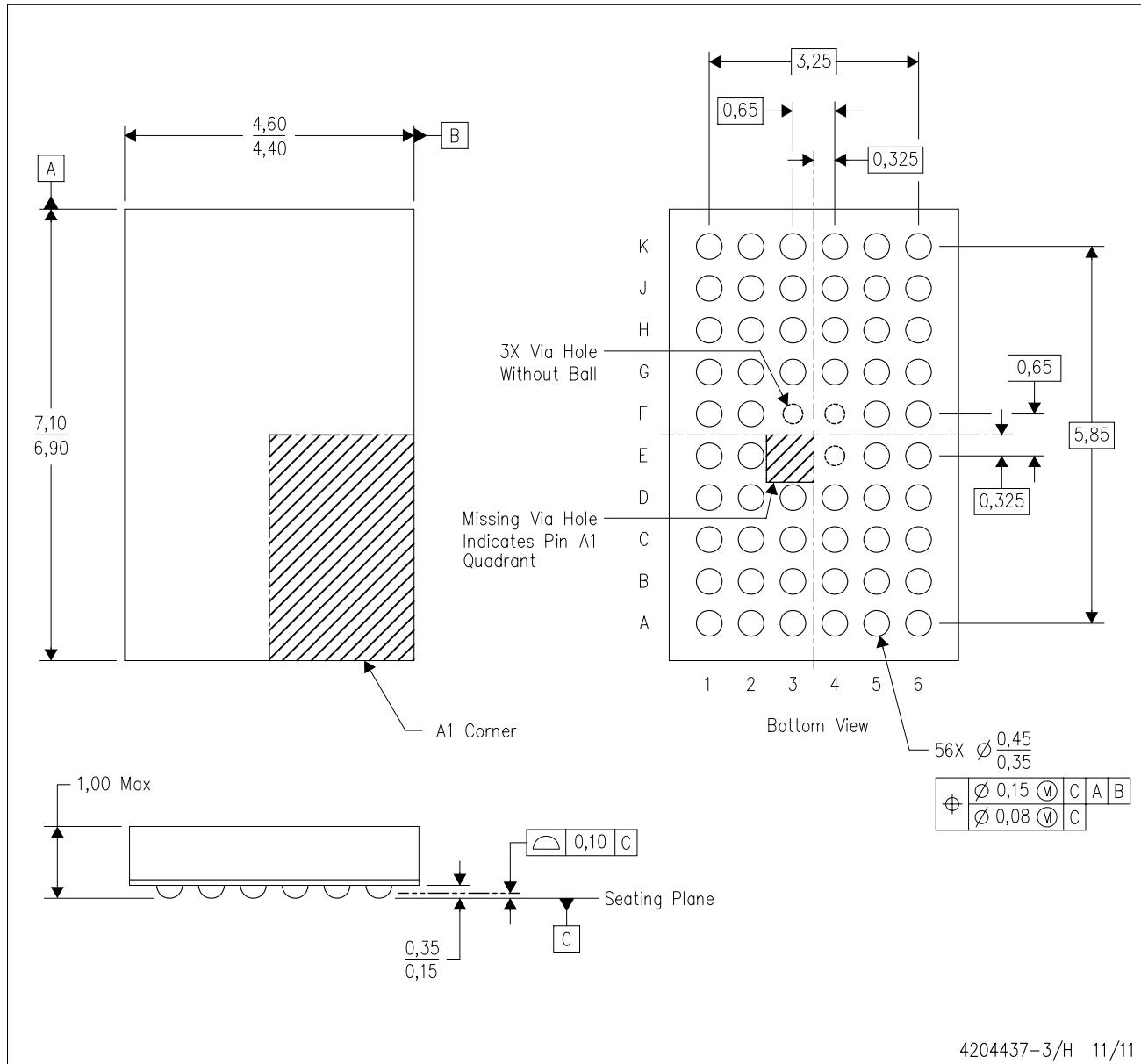
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC16245ADGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74LVC16245ADLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVC16245AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6
SN74LVC16245AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	336.6	336.6	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

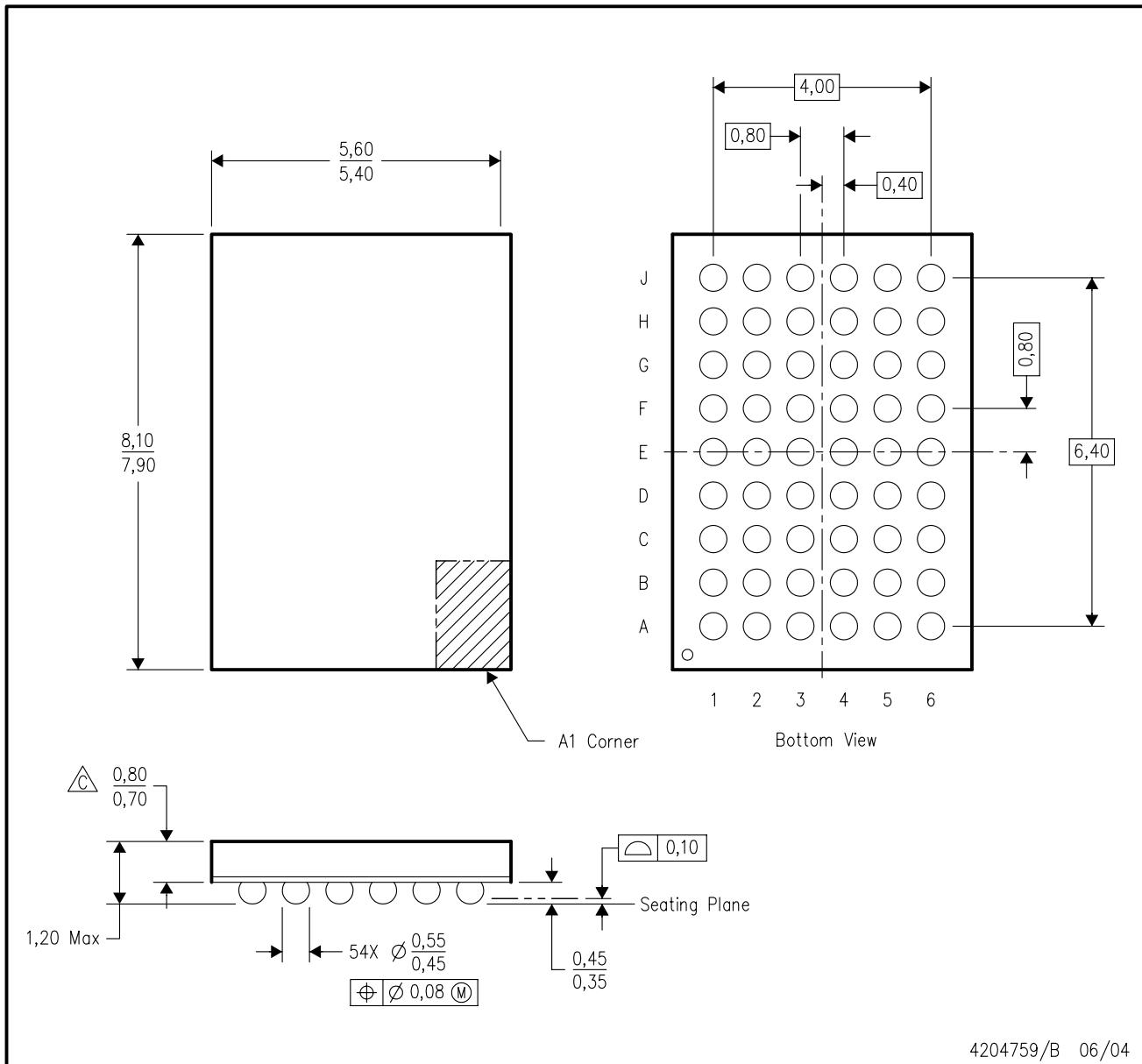


NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is Pb-free. Refer to the 56 QGL package (drawing 4200583) for tin-lead (SnPb).

## GRD (R-PBGA-N54)

## PLASTIC BALL GRID ARRAY



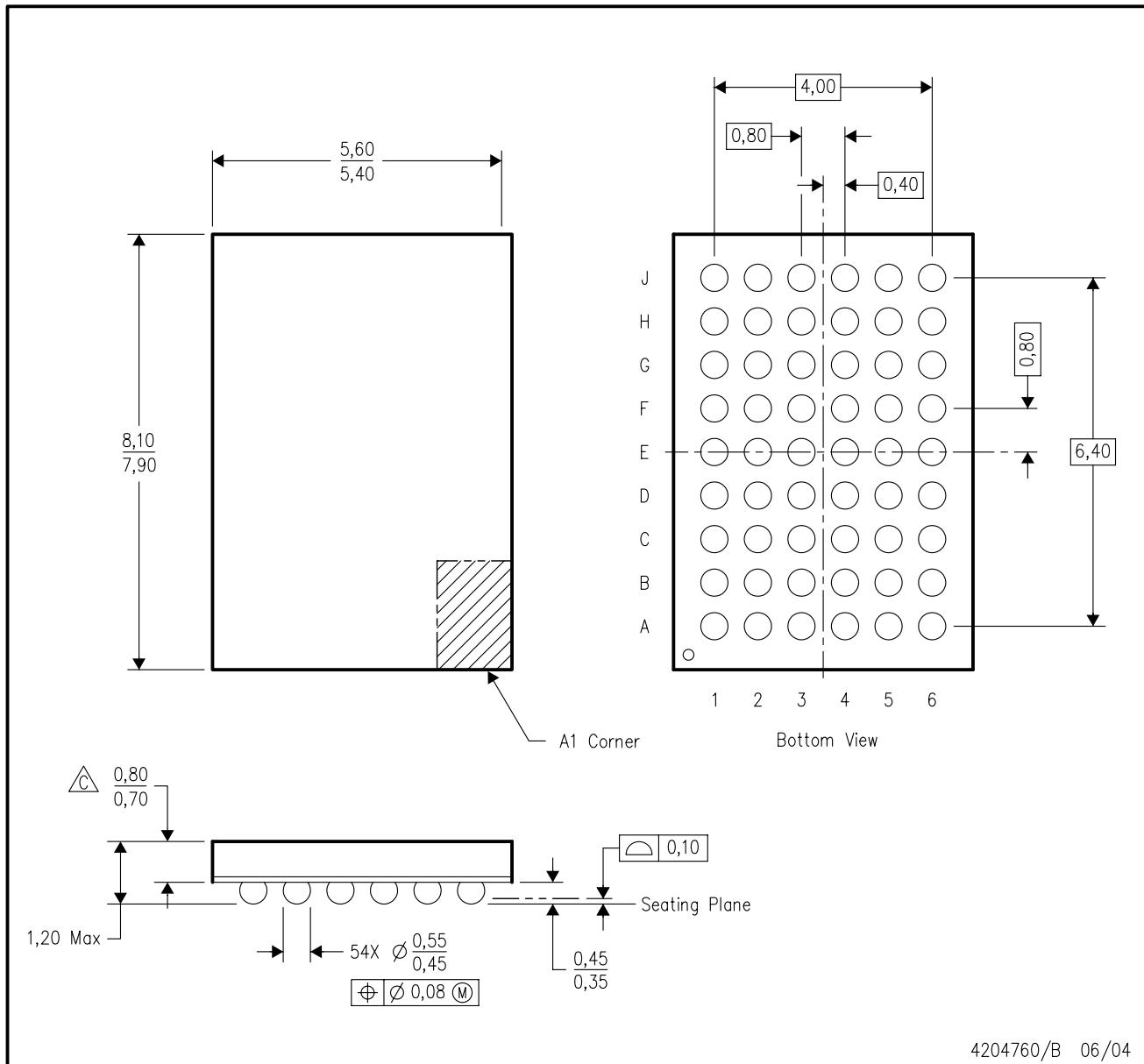
NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.

Falls within JEDEC MO-205 variation DD.

D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

## ZRD (R-PBGA-N54)

## PLASTIC BALL GRID ARRAY



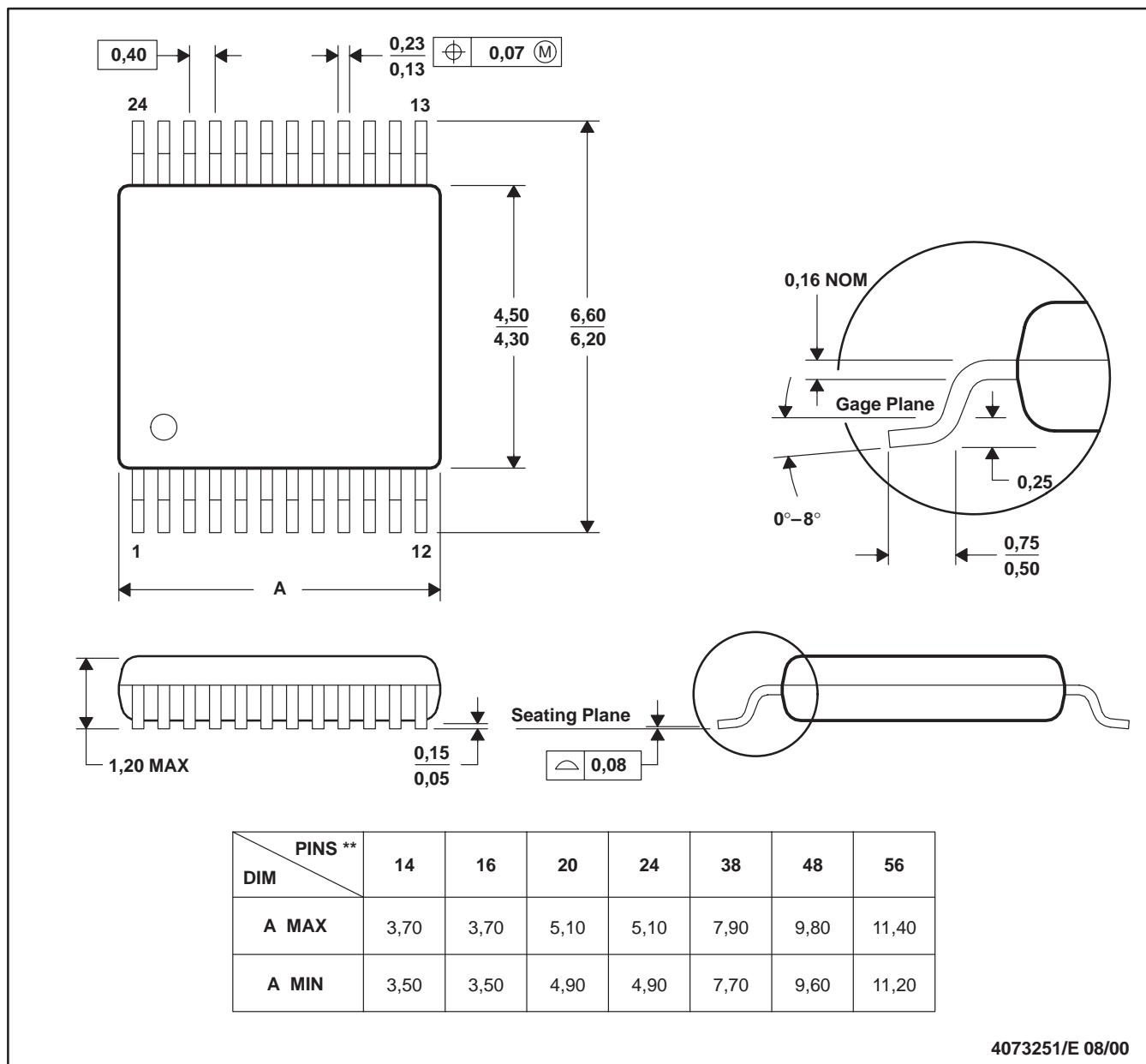
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation DD.
- D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

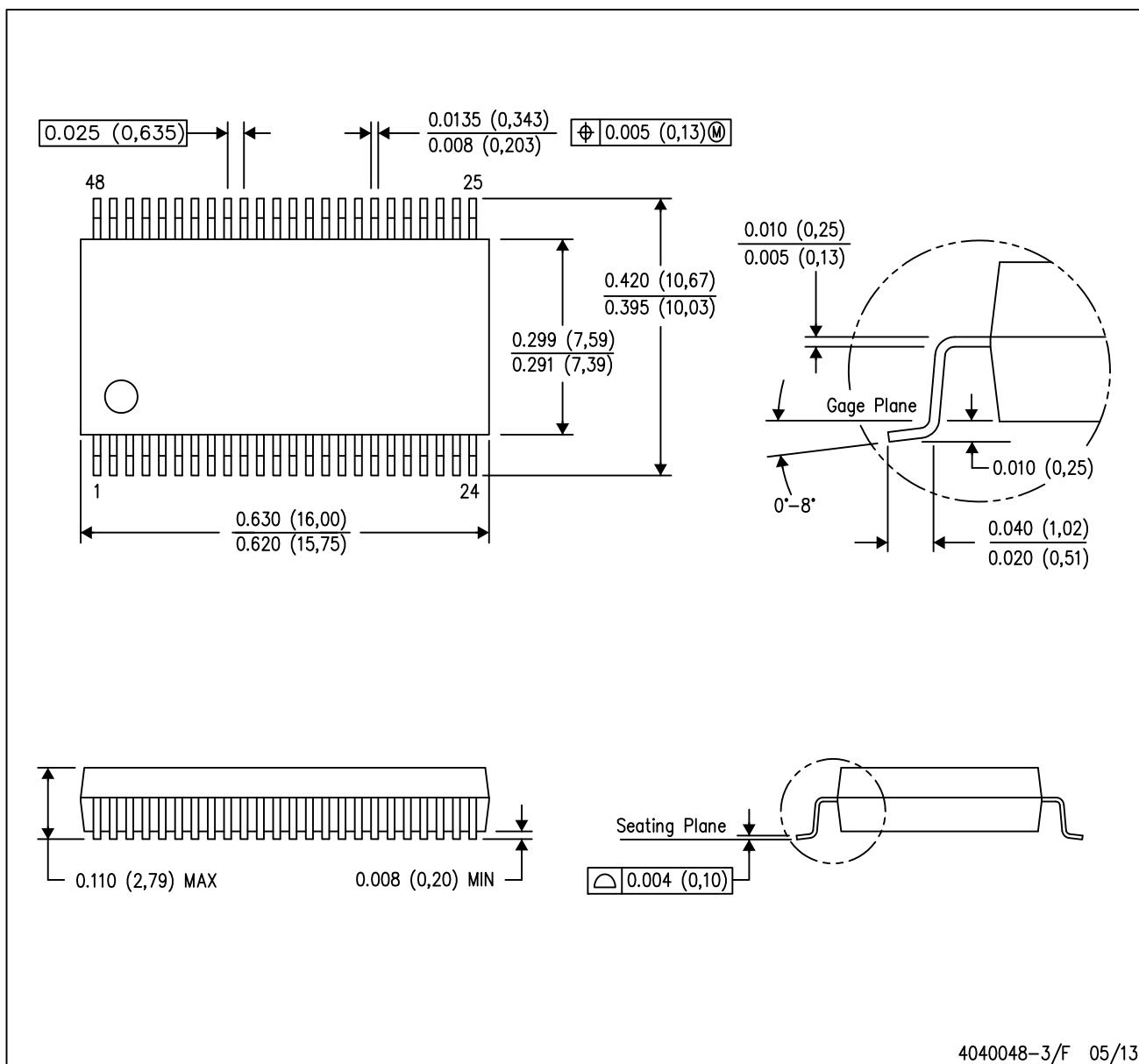
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

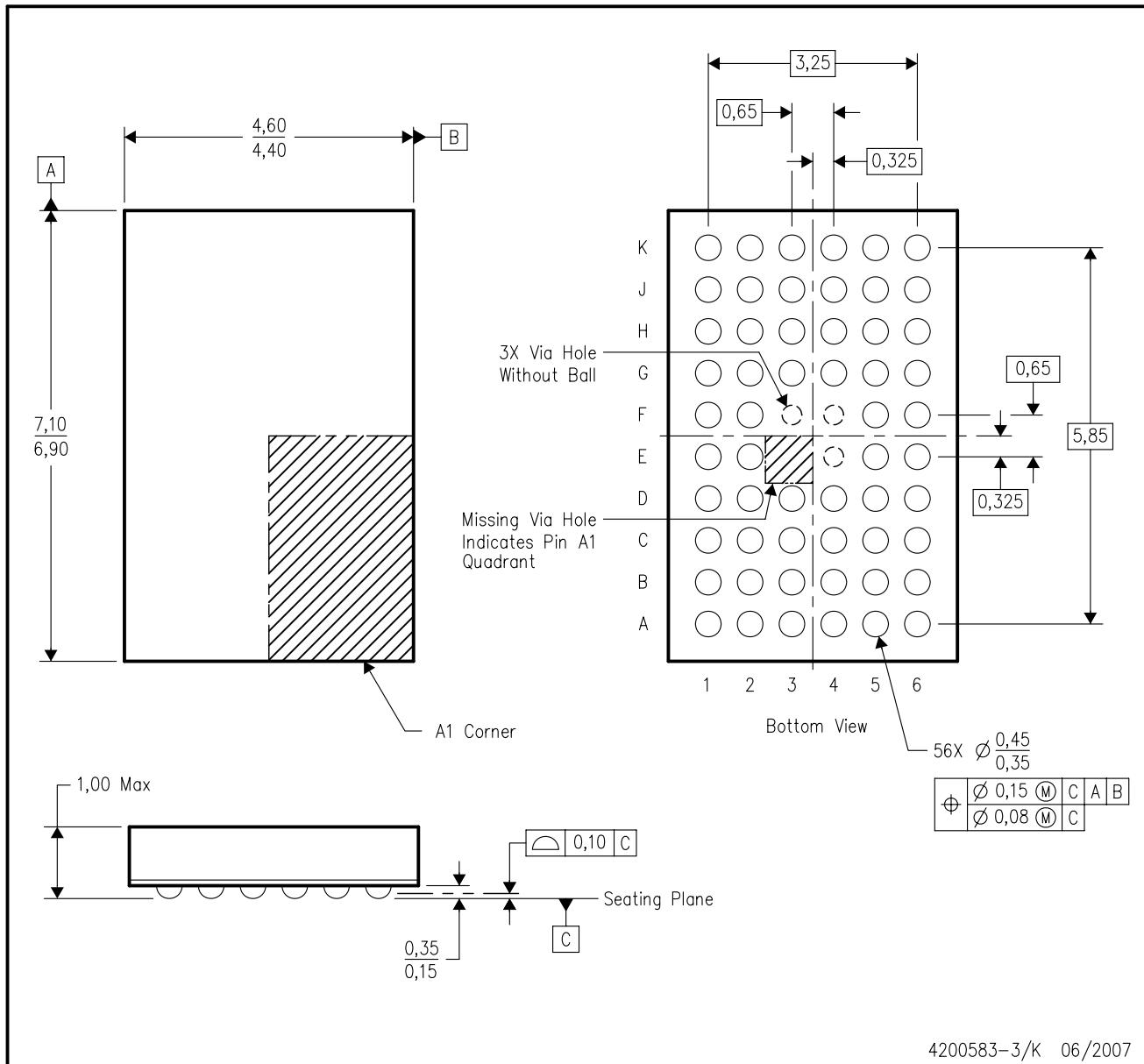
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118

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## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



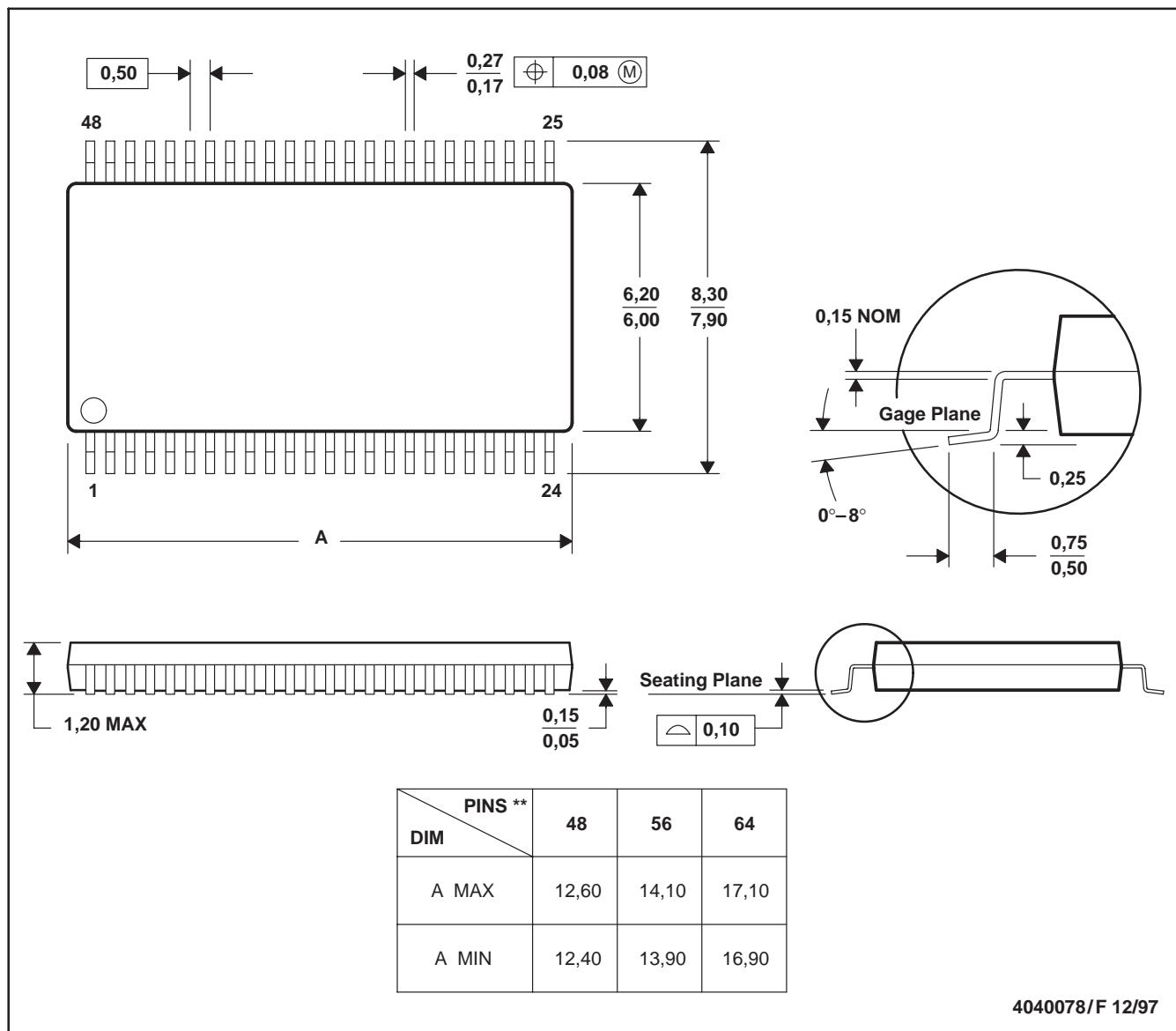
NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0.15.  
 D. Falls within JEDEC MO-153

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
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