# Switched Capacitor Regulated Voltage Inverter

## FEATURES

- **Regulated Negative Voltage from a Single Positive Supply**
- **REG Pin Indicates Output is in Regulation**
- Adjustable or Fixed Output Voltages
- Output Regulation: ±4.5%
- Supply Current: 650µA Typ
- Shutdown Mode Drops Supply Current to 5µA
- Up to 20mA Output Current
- Requires Only Three or Four External Capacitors
- Available in MS8 and SO-8 Packages

## APPLICATIONS

- GaAs FET Bias Generators
- Negative Supply Generators
- Battery-Powered Systems
- Single Supply Applications

## DESCRIPTION

The LTC®1261L is a switched-capacitor voltage inverter designed to provide a regulated negative voltage from a single positive supply. The LTC1261L operates from a single 2.7V to 5.25V supply and provides an adjustable output voltage from –1.23V to –5V. The LTC1261L-4/LTC1261L-4.5 needs a single 4.5V to 5.25V supply and provides a fixed output voltage of –4V to –4.5V respectively. Three external capacitors are required: a 0.1µF flying capacitor and an input and output bypass capacitors. An optional compensation capacitor at ADJ (COMP) can be used to reduce the output voltage ripple.

Each version of the LTC1261L will supply up to 20mA output current with guaranteed output regulation of ±4.5%. The LTC1261L includes an open-drain REG output that pulls low when the output is within 5% of the set value. Quiescent current is typically 650µA when operating and 5µA in shutdown.

The LTC1261L is available in 8-pin MSOP and SO packages.

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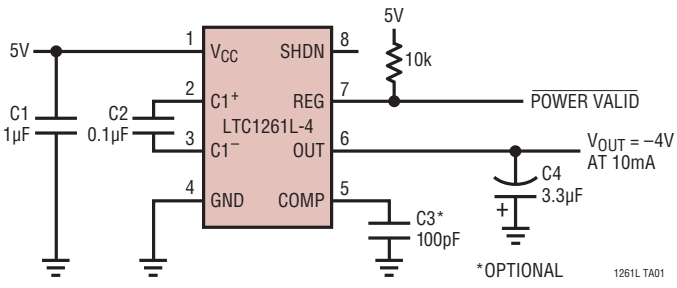
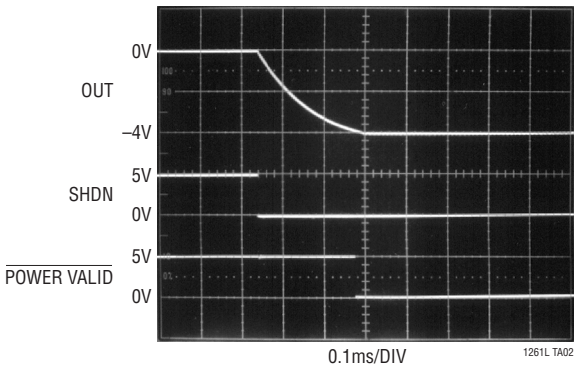
## TYPICAL APPLICATION

**–4V Generator with $\overline{\text{Power Valid}}$**




**Waveforms for –4V Generator with $\overline{\text{Power Valid}}$**

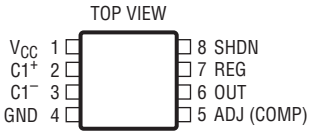


## ABSOLUTE MAXIMUM RATINGS (Note 1)

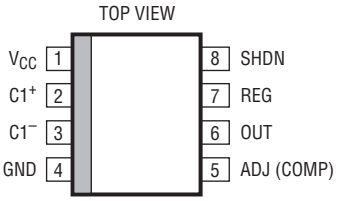
Supply Voltage (Note 2) ..... 5.5V
Output Voltage (Note 3) ..... 0.3V to –5.3V
Total Voltage, $V_{CC}$ to $V_{OUT}$ (Note 2) ..... 10.8V
SHDN Pin ..... –0.3V to ($V_{CC}$ + 0.3V)
REG Pin ..... –0.3V to 6V
ADJ Pin ..... ($V_{OUT}$ – 0.3V) to ($V_{CC}$ + 0.3V)

Output Short-Circuit Duration ..... Indefinite
Commercial Temperature Range (Note 4) .... 0°C to 70°C
Industrial Temperature Range (Note 4) ... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION




MS8 PACKAGE
8-LEAD PLASTIC MSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 200°C/W




S8 PACKAGE
8-LEAD PLASTIC SO
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 135°C/W

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC1261LCMS8#PBF | LTC1261LCMS8#TRPBF | LTFM | 8-Lead Plastic MSOP | 0°C to 70°C |
| LTC1261LIMS8#PBF | LTC1261LIMS8#TRPBF | LTFM | 8-Lead Plastic MSOP | –40°C to 85°C |
| LTC1261LCMS8-4#PBF | LTC1261LCMS8-4#TRPBF | LTFN | 8-Lead Plastic MSOP | 0°C to 70°C |
| LTC1261LIMS8-4#PBF | LTC1261LIMS8-4#TRPBF | LTFN | 8-Lead Plastic MSOP | –40°C to 85°C |
| LTC1261LCMS8-4.5#PBF | LTC1261LCMS8-4.5#TRPBF | LTFP | 8-Lead Plastic MSOP | 0°C to 70°C |
| LTC1261LIMS8-4.5#PBF | LTC1261LIMS8-4.5#TRPBF | LTFP | 8-Lead Plastic MSOP | –40°C to 85°C |
| LTC1261LCS8#PBF | LTC1261LCS8#TRPBF | 1261L | 8-Lead Plastic SO | 0°C to 70°C |
| LTC1261LIS8#PBF | LTC1261LIS8#TRPBF | 1261L | 8-Lead Plastic SO | –40°C to 85°C |
| LTC1261LCS8-4#PBF | LTC1261LCS8-4#TRPBF | 1261L4 | 8-Lead Plastic SO | 0°C to 70°C |
| LTC1261LIS8-4#PBF | LTC1261LIS8-4#TRPBF | 1261L4 | 8-Lead Plastic SO | –40°C to 85°C |
| LTC1261LCS8-4.5#PBF | LTC1261LCS8-4.5#TRPBF | 261L45 | 8-Lead Plastic SO | 0°C to 70°C |
| LTC1261LIS8-4.5#PBF | LTC1261LIS8-4.5#TRPBF | 261L45 | 8-Lead Plastic SO | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C, C1 = 0.1µF, $C_{OUT}$ = 3.3µF unless otherwise noted. (Notes 2, 4)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | | | | | |
| | LTC1261LCMS8/LTC1261LCS8 | | ● | 2.7 | | 5.25 | V |
| | LTC1261LCMS8-4/LTC1261LCS8-4 | (Note 5) | ● | 4.35 | | 5.25 | V |
| | LTC1261LCMS8-4.5/LTC1261LCS8-4.5 | (Note 5) | ● | 4.75 | | 5.25 | V |
| $V_{REF}$ | Reference Voltage | | | | 1.23 | | V |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5.25V, No Load, SHDN Floating | ● | | 650 | 1500 | µA |
| | | $V_{CC}$ = 5.25V, No Load, $V_{SHDN}$ = $V_{CC}$ | ● | | 5 | 20 | µA |
| $f_{OSC}$ | Internal Oscillator Frequency | $V_{CC}$ = 5V, $V_{OUT}$ = –4V | | | 650 | | kHz |
| $V_{OL}$ | REG Output Low Voltage | $I_{REG}$ = 1mA, $V_{CC}$ = 5V, $V_{OUT}$ = –4V | ● | | 0.1 | 0.8 | V |
| $I_{REG}$ | REG Sink Current | $V_{REG}$ = 0.8V, $V_{CC}$ = 3.3V | ● | 4 | 8 | | mA |
| | | $V_{REG}$ = 0.8V, $V_{CC}$ = 5V | ● | 5 | 12 | | mA |
| $I_{ADJ}$ | Adjust Pin Current | $V_{ADJ}$ = 1.23V | ● | | ±0.01 | ±1 | µA |
| $V_{IH}$ | SHDN Input High Voltage | $V_{CC}$ = 5V | ● | 2 | | | V |
| $V_{IL}$ | SHDN Input Low Voltage | $V_{CC}$ = 5V | ● | | | 0.8 | V |
| $I_{IN}$ | SHDN Input Current | $V_{SHDN}$ = $V_{CC}$ | ● | | 2.5 | 25 | µA |
| $t_{ON}$ | Turn-On Time | $V_{CC}$ = 5V, $I_{OUT}$ = 10mA, –1.5V ≤ $V_{OUT}$ ≤ –4V (LTC1261L) | ● | | 250 | 1500 | µs |
| | | $V_{CC}$ = 5V, $I_{OUT}$ = 5mA, $V_{OUT}$ = –4.5V (LTC1261L) | ● | | 250 | 1500 | µs |
| | | $V_{CC}$ = 5V, $I_{OUT}$ = 10mA, $V_{OUT}$ = –4V (LTC1261L-4) | ● | | 250 | 1500 | µs |
| | | $V_{CC}$ = 5V, $I_{OUT}$ = 5mA, $V_{OUT}$ = –4.5V (LTC1261L-4.5) | ● | | 250 | 1500 | µs |
| $V_{OUT}$ | Output Regulation (LTC1261L) | 2.70V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 10mA | ● | –1.552 | –1.5 | –1.448 | V |
| | | 3.25V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 20mA | ● | –1.552 | –1.5 | –1.448 | V |
| | | 2.70V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 5mA | ● | –2.070 | –2.0 | –1.930 | V |
| | | 2.95V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 10mA | ● | –2.070 | –2.0 | –1.930 | V |
| | | 3.50V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 20mA | ● | –2.070 | –2.0 | –1.91 | V |
| | | 2.95V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 5mA | ● | –2.587 | –2.5 | –2.413 | V |
| | | 3.30V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 10mA | ● | –2.587 | –2.5 | –2.413 | V |
| | | 3.85V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 20mA | ● | –2.587 | –2.5 | –2.41 | V |
| | | 3.40V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 5mA | ● | –3.105 | –3.0 | –2.895 | V |
| | | 3.70V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 10mA | ● | –3.105 | –3.0 | –2.895 | V |
| | | 4.25V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 20mA | ● | –3.105 | –3.0 | –2.885 | V |
| | | 3.85V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 5mA | ● | –3.622 | –3.5 | –3.378 | V |
| | | 4.10V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 10mA | ● | –3.622 | –3.5 | –3.378 | V |
| | | 4.60V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 20mA | ● | –3.622 | –3.5 | –3.365 | V |
| | Output Regulation (LTC1261L/LTC1261L-4) | 4.35V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 5mA | ● | –4.140 | –4.0 | –3.860 | V |
| | | 4.60V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 10mA | ● | –4.140 | –4.0 | –3.860 | V |
| | | 5.10V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 20mA | ● | –4.140 | –4.0 | –3.83 | V |
| | Output Regulation (LTC1261L/LTC1261L-4.5) | 4.75V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 5mA | ● | –4.657 | –4.5 | –4.343 | V |
| | | 5.05V ≤ $V_{CC}$ ≤ 5.25V, 0mA ≤ $I_{OUT}$ ≤ 10mA | ● | –4.657 | –4.5 | –4.343 | V |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0V, $V_{CC}$ = 5.25V | ● | | 100 | 220 | mA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

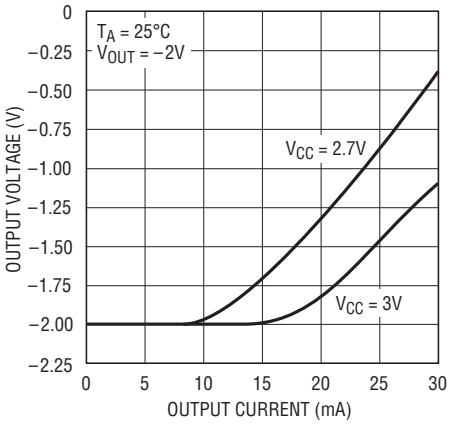
**Note 3:** The output should never be set to exceed $V_{CC}$ – 10.8V.

**Note 4:** The LTC1261LC is guaranteed to meet specifications from 0°C to 70°C and is designed, characterized and expected to meet industrial temperature limits, but is not tested at –40°C and 85°C. The LTC1261LI is guaranteed to meet specifications from –40°C and 85°C.

**Note 5:** The LTC1261L-4 and LTC1261L-4.5 will operate with less than the minimum $V_{CC}$ specified in the electrical characteristics table, but they are not guaranteed to meet the ±4.5% $V_{OUT}$ specification.

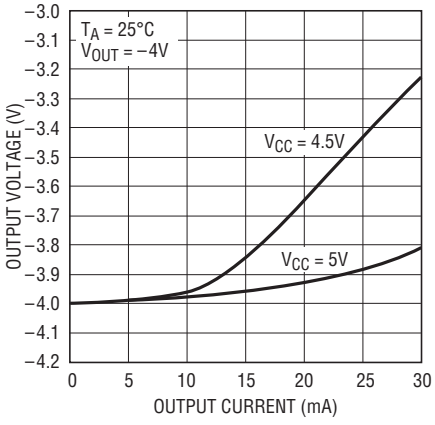
## TYPICAL PERFORMANCE CHARACTERISTICS (See Test Circuits)

### Output Voltage vs Output Current



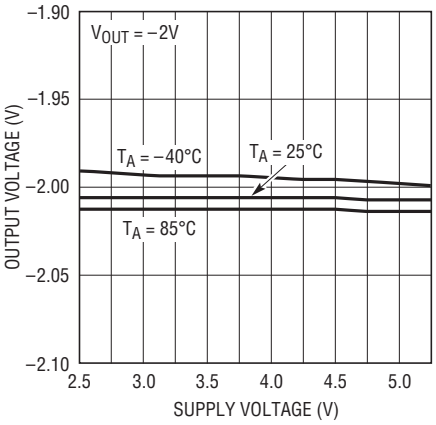

1261L G01

### Output Voltage vs Output Current



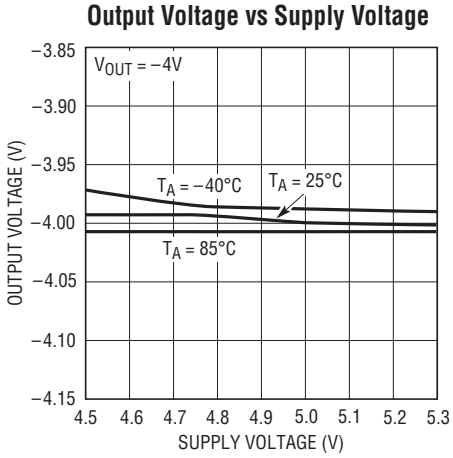

1261L G02

### Output Voltage vs Supply Voltage



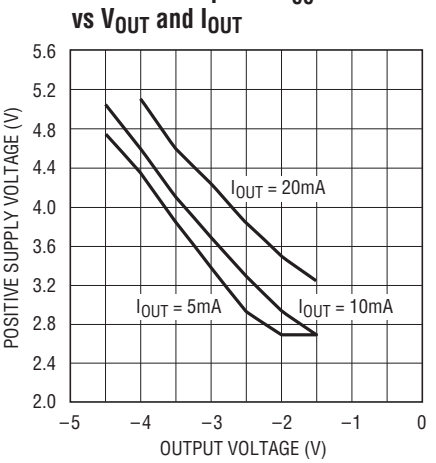

1261L G03

### Output Voltage vs Supply Voltage



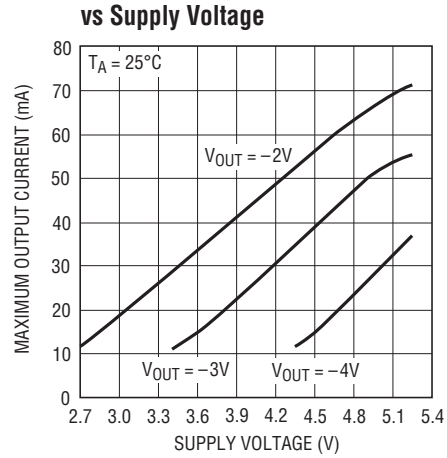

1261L G04

### Minimum Required $V_{CC}$ vs $V_{OUT}$ and $I_{OUT}$



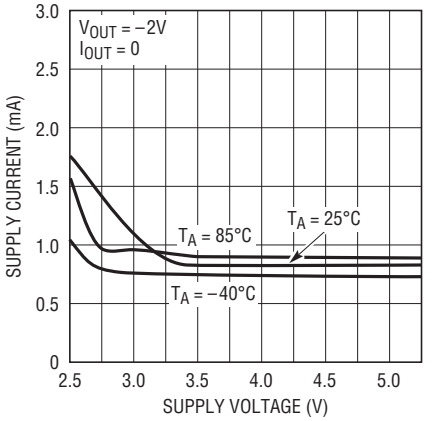

1261L G05

### Maximum Output Current vs Supply Voltage



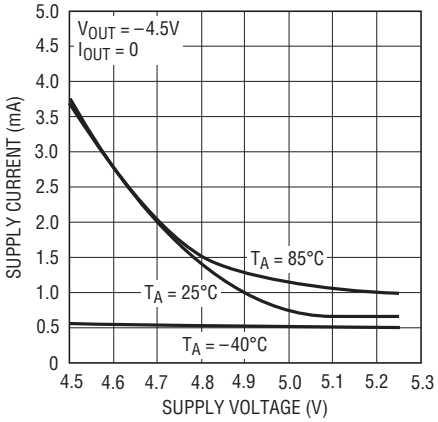

1261L G06

### Supply Current vs Supply Voltage



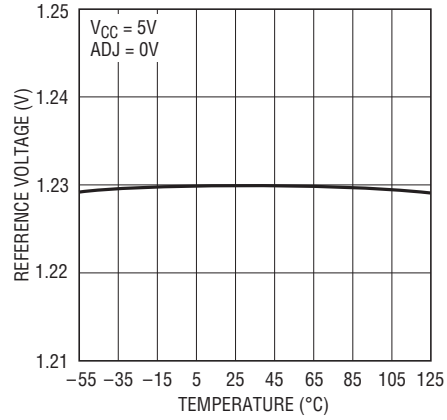

1261L G07

### Supply Current vs Supply Voltage




1261L G08

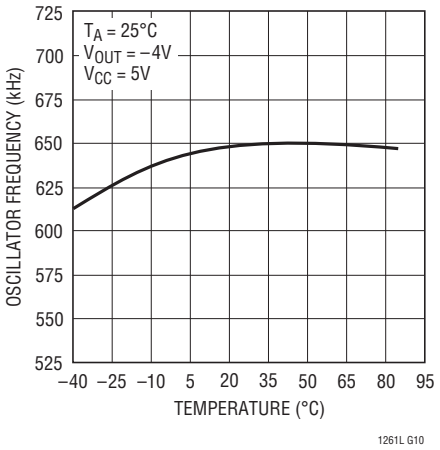
### Reference Voltage vs Temperature



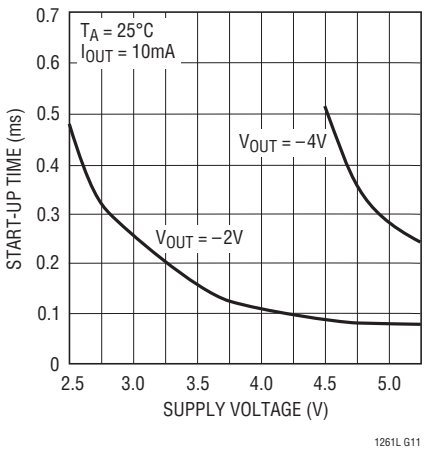

1261L G09

## TYPICAL PERFORMANCE CHARACTERISTICS

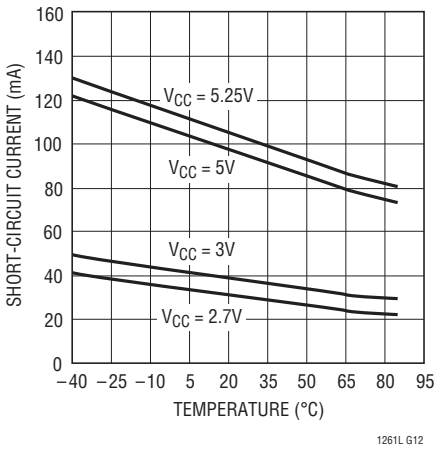
**Oscillator Frequency vs Temperature**




**Start-Up Time vs Supply Voltage**




**Output Short-Circuit Current vs Temperature**




## PIN FUNCTIONS

**$V_{CC}$ (Pin 1):** Power Supply. This requires an input voltage between 2.7V and 5.25V. $V_{CC}$ must be bypassed to ground with at least a 1µF capacitor placed in close proximity to the chip. See the Applications Information section for details.

**C1+ (Pin 2):** C1 Positive Input. Connect a 0.1µF capacitor between C1+ and C1–.

**C1– (Pin 3):** C1 Negative Input. Connect a 0.1µF capacitor from C1+ to C1–.

**GND (Pin 4):** Ground. Connect to a low impedance ground. A ground plane will help to minimize regulation errors.

**ADJ (COMP for Fixed Versions) (Pin 5):** Output Adjust/ Compensation Pin. For adjustable parts this pin is used to set the output voltage. The output voltage is divided down with an external resistor divider and fed back to this pin to set the regulated output voltage. Typically the resistor string should draw ≥10µA from the output to minimize errors due to the bias current at the adjust pin. Fixed output voltage parts have the internal resistor string connected to this pin inside the package. The pin can be used to trim the output voltage if desired. It can also be used as an optional feedback compensation pin to reduce output ripple on both the adjustable and fixed output voltage parts. See the Applications Information section for more information on compensation and output ripple.

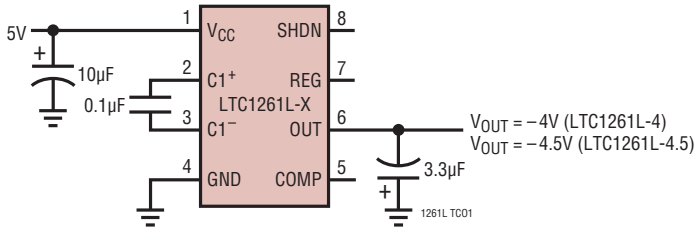
**OUT (Pin 6):** Negative Voltage Output. This pin must be bypassed to ground with a 1µF or larger capacitor. The value of the output capacitor and its ESR have a strong effect on output ripple. See the Applications Information section for more details.

**REG (Pin 7):** This is an open-drain output that pulls low when the output voltage is within 5% of the set value. It will sink 5mA to ground with a 5V supply. The external circuitry must provide a pull-up or REG will not swing high. The voltage at REG may exceed $V_{CC}$ and can be pulled up to 6V above ground without damage.

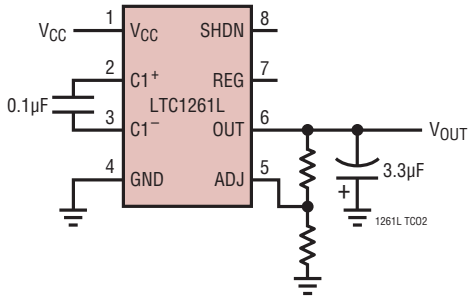
**SHDN (Pin 8):** Shutdown. When this pin is at ground the LTC1261L operates normally. An internal 5µA pull-down keeps SHDN low if it is left floating. When SHDN is pulled high, the LTC1261L enters shutdown mode. In shutdown, the charge pump is disabled, the output collapses to 0V and the quiescent current drops to 5µA typically.

## TEST CIRCUITS

**Fixed Output**




**Adjustable Output**




## APPLICATIONS INFORMATION

The LTC1261L uses an inverting charge pump to generate a regulated negative output voltage that is either equal to or less than the supply voltage. The LTC1261L needs only three external capacitors and is available in the MSOP and SO-8 packages

### THEORY OF OPERATION

A block diagram of the LTC1261L is shown in Figure 1. The heart of the LTC1261L is the charge pump core shown in the dashed box. It generates a negative output voltage by first charging the flying capacitor (C1) between $V_{CC}$ and ground. It then connects the top of the flying capacitor to ground, forcing the bottom of the flying capacitor to a negative voltage. The charge on the flying capacitor is transferred to the output bypass capacitor, leaving it charged to the negative output voltage. This process is driven by the internal 650kHz clock.

Figure 1 shows the charge pump configuration. With the clock low, C1 is charged to $V_{CC}$ by S1 and S3. At the next rising clock edge, S1 and S3 are open and S2 and S4 closed. S2 connects $C1^+$ to ground, $C1^-$ is connected to the output by S4. The charge in C1 is transferred to $C_{OUT}$, setting it to a negative voltage.

The output voltage is monitored by COMP1 which compares a divided replica of the output at ADJ (COMP for fixed output voltage parts) to the internal reference. At the beginning of a cycle the clock is low, forcing the output of the AND gate low and charging the flying capacitor. The next rising clock edge sets the RS latch, setting the charge pump to transfer charge from the flying capacitor to the output capacitor. As long as the output is below the set point, COMP1 stays low, the latch stays set and the charge pump runs at the full 50% duty cycle of the clock gated through the AND gate. As the output approaches the set voltage, COMP1 will trip whenever the divided signal exceeds the internal 1.23V reference relative to OUT. This resets the RS latch and truncates the clock pulses, reducing the amount of charge transferred to the output capacitor and regulating the output voltage. If the output exceeds the set point, COMP1 stays high, inhibiting the RS latch and disabling the charge pump.

COMP2 also monitors the divided signal at ADJ but it is connected to a 1.17V reference, 5% below the main reference voltage. When the divided output exceeds this lower reference voltage indicating that the output is within 5% of the set value, COMP2 goes high turning on the REG output transistor. This is an open-drain N-channel device capable of sinking 4mA with a 3.3V $V_{CC}$ and 5mA with a 5V $V_{CC}$. When in the "off" state (divided output is more than 5% below $V_{REF}$) the drain can be pulled above $V_{CC}$ without damage up to a maximum of 6V above ground. Note that the REG output only indicates if the magnitude of the output is *below* the magnitude of the set point by 5% (i.e., $V_{OUT} > -4.75V$ for a –5V set point). If the magnitude of the output is forced *higher* than the magnitude of the set point (i.e., to –5.25V when the output is set for –5V) the REG output will stay low.

## APPLICATIONS INFORMATION

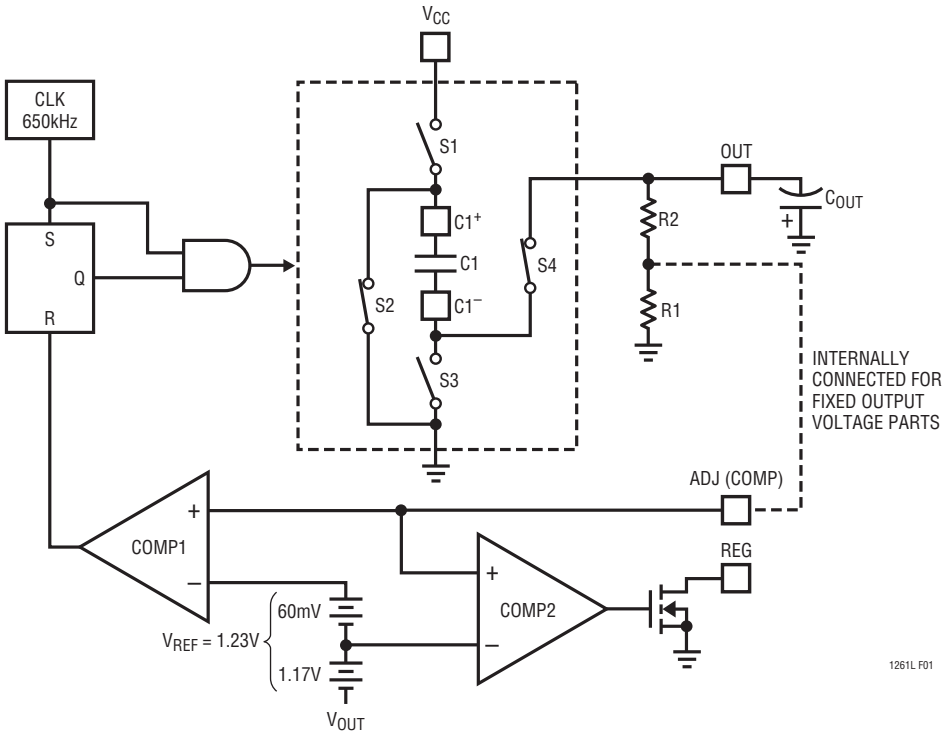



**Figure 1. Block Diagram**

### OUTPUT RIPPLE

Output ripple in the LTC1261L is present from two sources; voltage droop at the output capacitor between clocks and frequency response of the regulation loop. Voltage droop is easy to calculate. With a typical clock frequency of 650kHz, the charge on the output capacitor is refreshed once every 1.54µs. With a 15mA load and a 3.3µF output capacitor, the output will droop by:

$$I_{LOAD}\left(\frac{\Delta t}{C_{OUT}}\right) = 15mA\left(\frac{1.54\mu s}{3.3\mu F}\right) = 7mV$$

This can be a significant ripple component when the output is heavily loaded, especially if the output capacitor is small. If absolute minimum output ripple is required, a 10µF or greater output capacitor should be used.

Regulation loop frequency response is the other major contributor to output ripple. The LTC1261L regulates the output voltage by limiting the amount of charge transferred to the output capacitor on a cycle-by-cycle basis. The output voltage is sensed at the ADJ pin (COMP for fixed output voltage versions) through an internal or external resistor divider from the OUT pin to ground. As the flying capacitor is first connected to the output, the output voltage begins to change quite rapidly. As soon as it exceeds the set point COMP1 trips, switching the state of the charge pump and stopping the charge transfer. Because the RC time constant of the capacitors and the switches is quite short, the ADJ pin must have a wide AC bandwidth to be able to respond to the output in time. External parasitic capacitance at the ADJ pin can reduce the bandwidth to the point where the comparator cannot respond by the time the clock pulse finishes. When this happens the comparator will allow a few complete pulses through, then overcorrect and disable the charge pump until the output drops below the set point. Under these conditions the output will remain in regulation but the output ripple will increase as the comparator "hunts" for the correct value.

To prevent this from happening, an external capacitor can be connected from ADJ (or COMP for fixed output voltage parts) to ground to compensate for external parasitics and

## APPLICATIONS INFORMATION

increase the regulation loop bandwidth (Figure 2). This sounds counter intuitive until we remember that the internal reference is generated with respect to OUT, not ground. The feedback loop actually sees ground as its "output," thus the compensation capacitor should be connected across the "top" of the resistor divider, from ADJ (or COMP) to ground. By the same token, avoid adding capacitance between ADJ (or COMP) and $V_{OUT}$. This will slow down the feedback loop and increase output ripple. A 100pF capacitor from ADJ or COMP to ground will compensate the loop properly under most conditions for fixed voltage versions of the LTC1261L. For the adjustable LTC1261L, the capacitor value will be dependent upon the values of the external resistors in the divider network.

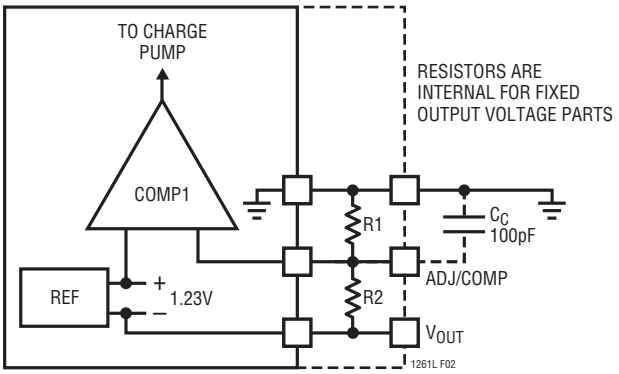



**Figure 2. Regulator Loop Compensation**

### OUTPUT FILTERING

If extremely low output ripple (<5mV) is required, additional output filtering is required. Because the LTC1261L uses a high 650kHz switching frequency, fairly low value RC or LC networks can be used at the output to effectively filter the output ripple. A 10Ω series output resistor and a 3.3µF capacitor will cut output ripple to below 3mV (Figure 3). Further reductions can be obtained with larger filter capacitors or by using an LC output filter.

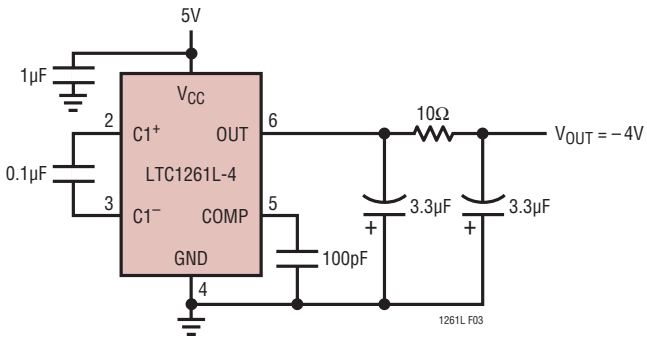



**Figure 3. Output Filter Cuts Ripple Below 3mV**

### CAPACITOR SELECTION

#### Capacitor Sizing

The performance of the LTC1261L is affected by the capacitors to which it connects. The LTC1261L requires bypass capacitors to ground for both the $V_{CC}$ and OUT pins. The input capacitor provides most of LTC1261L's supply current while it is charging the flying capacitors. This capacitor should be mounted as close to the package as possible and its value should be at least ten times larger than the flying capacitor. Ceramic capacitors generally provide adequate performance. Avoid using a tantalum capacitor as the input bypass unless there is at least a 0.1µF ceramic capacitor in parallel with it. The charge pump capacitor is somewhat less critical since its peak current is limited by the switches inside the LTC1261L. Most applications should use a 0.1µF as the flying capacitor value. Conveniently, ceramic capacitors are the most common type of 0.1µF capacitor and they work well here. Usually the easiest solution is to use the same capacitor type for both the input bypass capacitor and the flying capacitor.

In applications where the maximum load current is well-defined and output ripple is critical or input peak currents need to be minimized, the flying capacitor value can be

## APPLICATIONS INFORMATION

tailored to the application. Reducing the value of the flying capacitor reduces the amount of charge transferred with each clock cycle. This limits maximum output current, but also cuts the size of the voltage step at the output with each clock cycle. The smaller capacitor draws smaller pulses of current out of $V_{CC}$ as well, limiting peak currents and reducing the demands on the input supply. Table 1 shows recommended values of flying capacitor vs maximum load capacity.

**Table 1. Typical Max Load (mA) vs Flying Capacitor Value at $T_A$ = 25°C, $V_{OUT}$ = –4V**

| FLYING CAPACITOR VALUE (µF) | MAX LOAD (mA) $V_{CC}$ = 5V |
|---|---|
| 0.1 | 20 |
| 0.047 | 15 |
| 0.033 | 10 |
| 0.022 | 5 |
| 0.01 | 1 |

The output capacitor performs two functions: it provides output current to the load during half of the charge pump cycle and its value helps to set the output ripple voltage. For applications that are insensitive to output ripple, the output bypass capacitor can be as small as 1µF. Larger output capacitors will reduce output ripple further at the expense of turn-on time.

### Capacitor ESR

Output capacitor Equivalent Series Resistance (ESR) is another factor to consider. Excessive ESR in the output capacitor can fool the regulation loop into keeping the output artificially low by prematurely terminating the charging cycle. As the charge pump switches to recharge the output a brief surge of current flows from the flying capacitors to the output capacitor. This current surge can be as high as 100mA under full load conditions. A typical 3.3µF tantalum capacitor has 1Ω or 2Ω of ESR; 100mA × 2Ω = 200mV. If the output is within 200mV of the set point this additional 200mV surge will trip the feedback comparator and terminate the charging cycle. The pulse dissipates quickly and the comparator returns to the correct state, but the RS latch will not allow the charge pump to respond until the next clock edge. This prevents the charge pump from going into very high frequency oscillation under such conditions but it also creates an output error as the feedback loop regulates based on the top of the spike, not the average value of the output (Figure 4). The resulting output voltage behaves as if a resistor of value $C_{ESR} \times (I_{PK}/I_{AVE})\Omega$ was placed in series with the output. To avoid this nasty sequence of events, connect a 0.1µF ceramic capacitor in parallel with the larger output capacitor. The ceramic capacitor will "eat" the high frequency spike, preventing it from fooling the feedback loop, while the larger but slower tantalum or aluminum output capacitor supplies output current to the load between charge cycles.

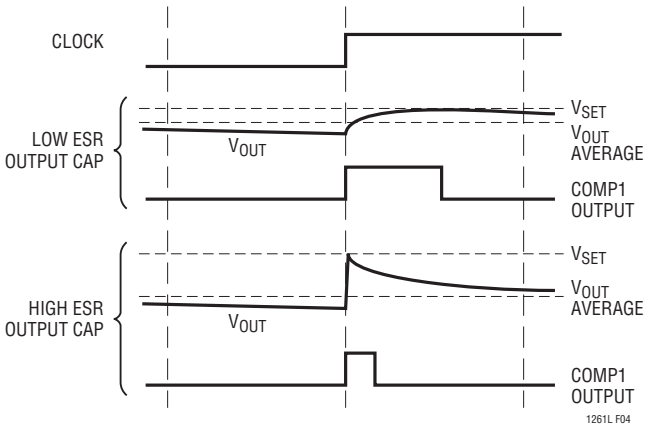



**Figure 4. Output Ripple with Low and High ESR Capacitors**

Note that ESR in the flying capacitor will not cause the same condition; in fact, it may actually improve the situation by cutting the peak current and lowering the amplitude of the spike. However, more flying capacitor ESR is not necessarily better. As soon as the RC time constant approaches half of a clock period (the time the capacitors have to share charge at full duty cycle) the output current capability of the LTC1261L starts to diminish. For a 0.1µF flying capacitor, this gives a maximum total series resistance of:

$$\frac{1}{2}\left(\frac{t_{CLK}}{C_{FLY}}\right)=\frac{1}{2}\left(\frac{1}{650kHz}\right)/0.1\mu F=7.7\Omega$$

Most of this resistance is already provided by the internal switches in the LTC1261L. More than 1Ω or 2Ω of ESR on the flying capacitors will start to affect the regulation at maximum load.

## APPLICATIONS INFORMATION

### RESISTOR SELECTION

Resistor selection is easy with the fixed output voltage versions of the LTC1261L—no resistors are needed! Selecting the right resistors for the adjustable parts is only a little more difficult. A resistor divider should be used to divide the signal at the output to give 1.23V at the ADJ pin *with respect to* $V_{OUT}$ (Figure 5). The LTC1261L uses a positive reference with respect to $V_{OUT}$, not a negative reference with respect to ground (Figure 1 shows the reference connection). Be sure to keep this in mind when connecting the resistors! If the initial output is not what you expected, try swapping the two resistors.

The LTC1261L can be internally configured for other fixed output voltages. Contact the Linear Technology Marketing department for details.

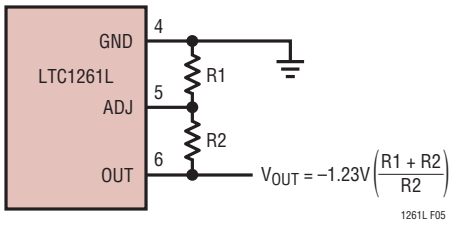
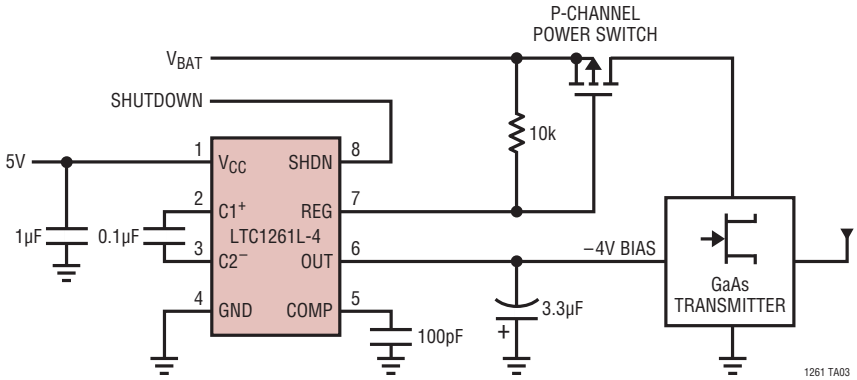


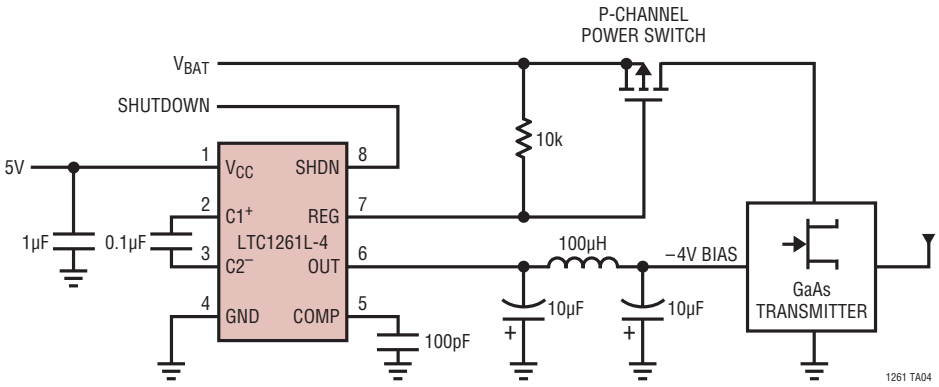

**Figure 5. External Resistor Connections**

## TYPICAL APPLICATIONS

**5V Input, –4V Output GaAs FET Bias Generator**

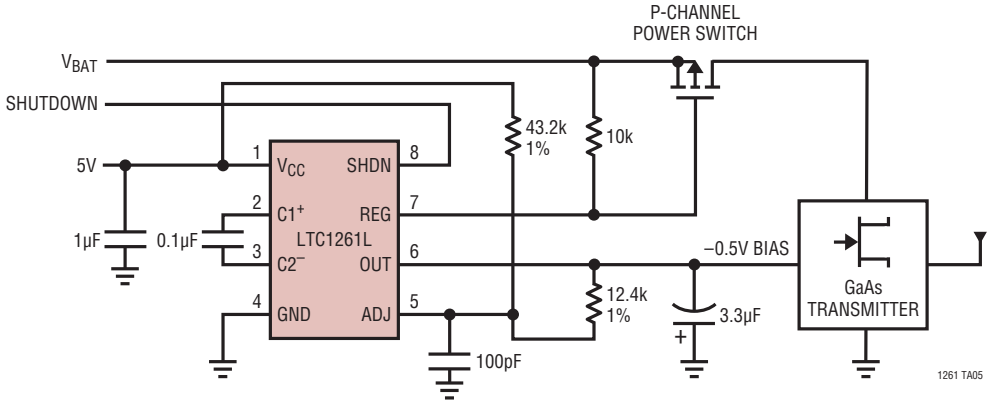



**1mV Ripple, 5V Input, –4V Output GaAs FET Bias Generator**



# TYPICAL APPLICATIONS

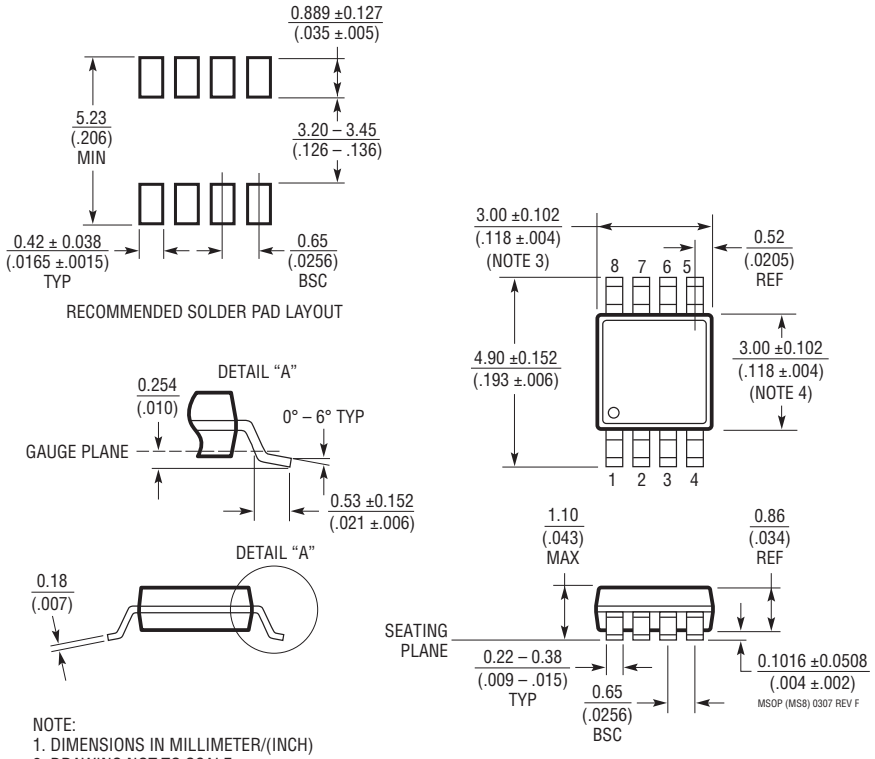
**5V Input, –0.5V Output GaAs FET Bias Generator**




# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**MS8 Package**
**8-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1660 Rev F)

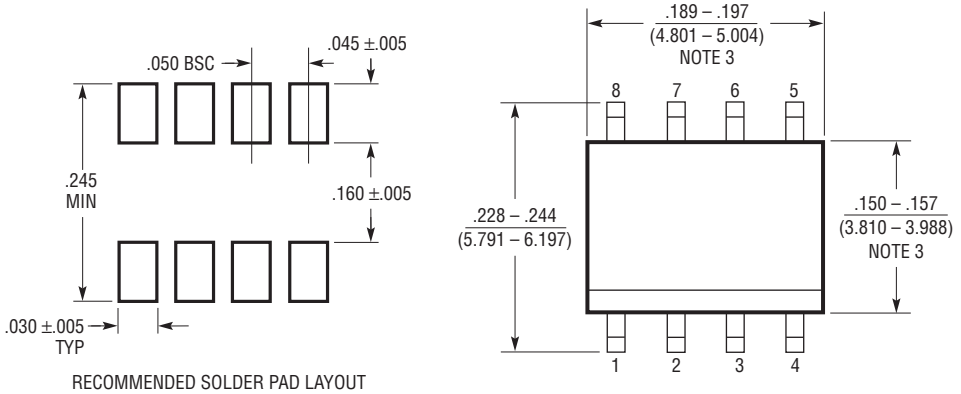



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**S8 Package**
**8-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610 Rev G)




NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 9/12 | Added I-grade option | Throughout |
| | | Modified Output Regulation specifications | 1, 3 |
| | | Modified Package/Order Information tables | 2 |
| | | Modified Notes 4 and 5 | 4 |



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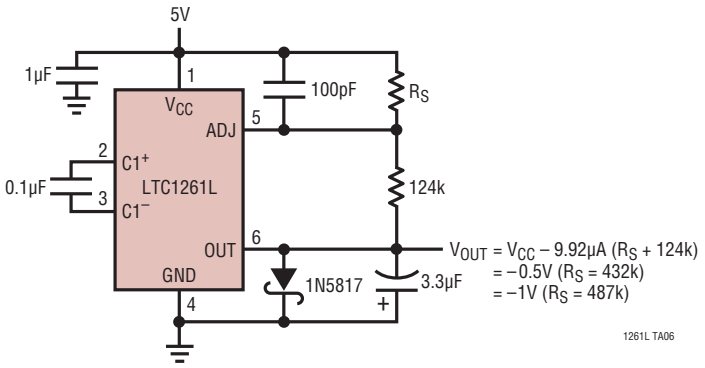
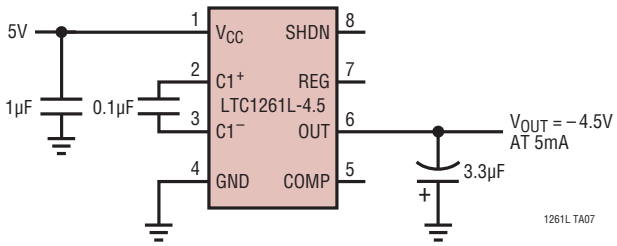
# TYPICAL APPLICATIONS

### Low Output Voltage Generator




### Minimum Parts Count –4.5V Generator




# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT1121 | Micropower Low Dropout Regulator with Shutdown | 0.4V Dropout Voltage at 150mA, Low Noise, Switched Capacitor Regulated Voltage Inverter |
| LTC1429 | Clock Synchronized Switched Capacitor Regulated Voltage Inverter | GaAs FET Bias |
| LTC1503-1.8/LTC1503-2 | High Efficiency Inductorless Step-Down DC/DC Converter | Fixed 1.8V or 2V Output from 2.4V to 6V Input, $I_{OUT}$ = 100mA |
| LTC1514/LTC1515 | Step-Up/Step-Down Switched Capacitors DC/DC Converters | $V_{IN}$: 2V to 10V, $V_{OUT}$ is Fixed or Adjustable, $I_{OUT}$ Up to 50mA |
| LTC1516 | Micropower, Regulated 5V Charge Pump DC/DC Converter | $I_{OUT}$ = 20mA ($V_{IN} \geq$ 2V), $I_{OUT}$ = 50mA ($V_{IN} \geq$ 3V) |
| LTC1517-5 | Micropower, Regulated 5V Charge Pump DC/DC Converter | LTC1522 without Shutdown and Packaged in SOT-23 |
| LTC1522 | Micropower, Regulated 5V Charge Pump DC/DC Converter | $I_{OUT}$ = 10mA ($V_{IN} \geq$ 2.7V), $I_{OUT}$ = 20mA ($V_{IN} \geq$ 3V) |
| LTC1550L/LTC1551L | Low Noise Switched Capacitor Regulated Voltage Inverter | GaAs FET Bias with Linear Regulator, <1mV Ripple, MSOP |
| LTC1555/LTC1556 | Sim Power Supply and Level Translator | Step-Up/Step-Down Sim Power Supply and Level Translators |
| LT1611 | 1.4MHz Inverting Mode Switching Regulator | –5V at 150mA from a 5V Input, 5-lead SOT-23 |
| LT1614 | Inverting 600kHz Switching Regulator with Low Battery Detector | –5V at 200mA from 5V Input in MSOP |
| LT1617/LT1617-1 | Micropower Inverting DC/DC Converters | –15V at 12mA from 2.5V Input, 5-lead SOT-23 |
| LTC1682/LTC1682-3.3/ LTC1682-5 | Low Noise Doubler Charge Pumps | Output Noise = 60µ$V_{RMS}$, 2.5V to 5.5V Output |
| LTC1754-5 | Micropower, Regulated 5V Charge Pump with Shutdown in SOT-23 | $I_{CC}$ = 13µA, $I_{OUT}$ = 50mA ($V_{IN} \geq$ 3V), $I_{OUT}$ = 25mA ($V_{IN} \geq$ 2.7V) |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