

DATA SHEET



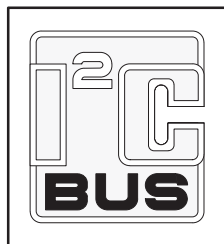
PCA9504A Glue chip 4

Product data
Supersedes data of 2003 Nov 10

2004 May 11

Glue chip 4

PCA9504A



FEATURES

- Dual, Strapping, Selectable Feature Sets
- Audio-disable Circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RMSRST# generation
- Voltage translation for DDC to VGA monitor
- HSYNCH / VSYNCH voltage translation to VGA monitor
- 3-state buffers for test
- Extra GP Logic gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit
- 5 V I²C to 3.3 V SMBus conversion to 400 kHz
- Requires both 3.3 V and 5.0 V operating voltages
- 0 to +70 °C operating temperature range
- ESD protection exceeds 1000 V HBM per JESD22-A114 and 750 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offered: TSSOP56

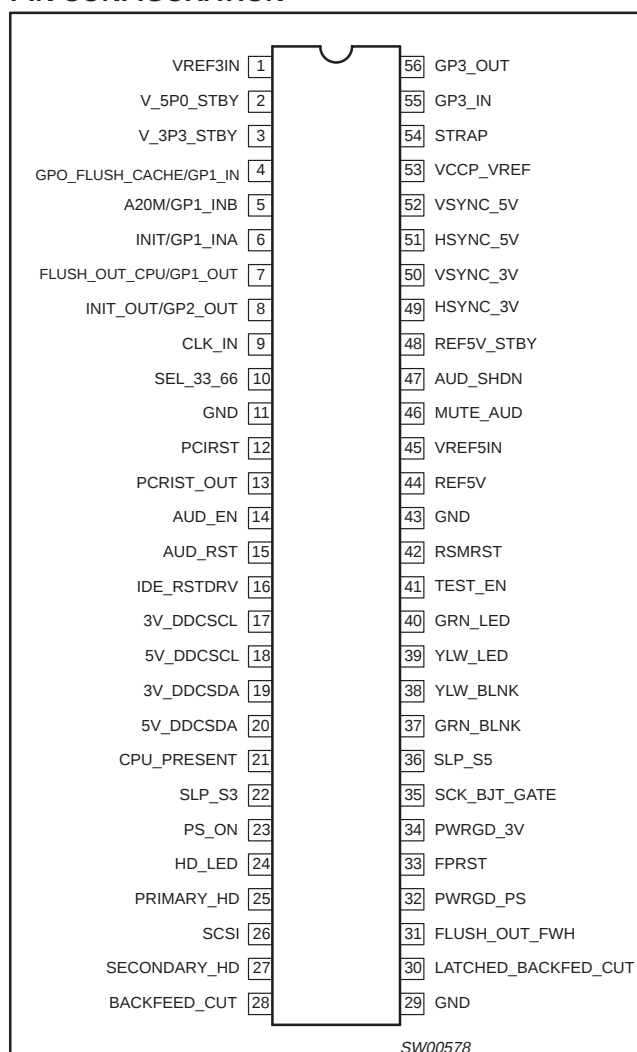
DESCRIPTION

The PCA9504A Glue Chip 4 is a highly integrated and cost-efficient custom ASIC that reduces logic part count, overall component cost, and board space requirements for PC designers and manufacturers. The Glue Chip 4 supports the latest generation of high-volume

platforms based on Intel® processors and chipsets that require additional external circuitry in order to function properly. It is used on entry servers/workstations (840 and 860 chipsets), high-end desktops (820 and 850 chipsets), as well as mid range (815, 830 and 845 chipsets) and low-end (810 chipset) motherboards. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells.

The PCA9504A Glue Chip 4 integrates miscellaneous motherboard logic and analog functions into a single, small footprint 56-pin TSSOP device. The Glue Chip 4 typically resides on the motherboard close to the I/O controller Hub (ICH) and is optimized for the Intel 82801BA I/O controller hub (ICH2).

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
56-Pin Plastic TSSOP	0 °C to +70 °C	PCA9504ADGG	PCA9504ADGG	SOT364-1

Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

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PIN DESCRIPTION

PIN(S)	SYMBOL	FUNCTION
1	3I	VREF3IN
2	P	V_5P0_STBY
3	P	V_3P3_STBY
4	3IU	GPO_FLUSH_CACHE / GP2_IN
5	REF	A20M / GP1_INB
6	REF	INIT / GP1_INA
7	5V OD	FLUSH_OUT_CPU / GP1_OUT
8	5V OD	INIT_OUT / GP2_OUT
9	3I	CLK_IN
10	3IU	SEL_33_66
11, 29, 43	G	GND
12	3I	PCRIST
13	3O	PCRIST_OUT
14	3IU	AUD_EN
15	3O	AUD_RST
16	5O	IDE_RSTDRV
17	3IOD	3V_DDCSCL
18	5IOD	5V_DDCSCL
19	3IOD	3V_DDCSDA
20	5IOD	5V_DDCSDA
21	3IU	CPU_PRESENT
22	3I	SLP_S3
23	5V OD	PS_ON
24	5V OD	HD_LED
25	5IU	PRIMARY_HD
26	5IU	SCSI
27	5IU	SECONDARY_HD
28	5V OD	BACKFEED_CUT
30	5O	LATCHED_BACKFEED_CUT
31	5V OD	FLUSH_OUT_FWH
32	5IU	PWRGD_PS
33	5IU	FPRST
34	3O	PWRGD_3V
35	5V OD	SCK_BJT_GATE
36	3I	SLP_S5
37	3IU	GRN_BLNK
38	3IU	YLW_BLNK
39	5V OD	YLW_LED
40	5V OD	GRN_LED
41	5ID	TEST_EN
42	3O	RSMRST
44	AO	REF5V
45	5I	VREF5IN
46	3IU	MUTE_AUD
47	5O	AUD_SHDN
48	AO	REF5V_STBY
49	3I	HSYNC_3V

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PIN DESCRIPTION CONTINUED

PIN(S)		SYMBOL	FUNCTION
50	3I	VSYN _C _3V	VSYNCH input from chipset video
51	5O	HSYN _C _5V	HSYNCH output to monitor
52	5O	VSYN _C _5V	VSYNCH output to monitor
53	AI	V _{CCP} _VREF	Analog voltage reference for determining INIT/A20M input thresholds
54	3IV/3O	STRAP	Strapping option for GP or FLUSH mode (internal pull-up resistor) Note 1
55	5I	GP3_IN	Generic logic gate 3 input
56	5V OD	GP3_OUT	Generic logic gate 3 output

NOTE:

1. The pin is internally pulled up to default to FLUSH mode.

TYPE	DESCRIPTION
3I	3.3 V input signal
3IU	3.3 V input signal with internal pull-up
5I	5 V input signal
5IU	5 V input signal with internal pull-up
5ID	5 V input signal with internal pull-down
P	Power (input)
G	Ground (input)
3O	3.3 V output signal
5O	5 V output signal
3V OD	3.3 V open-drain output signal
5V OD	5 v open-drain output signal
AO	Analog output
AI	Analog input
3IOD	3.3 V input/output open-drain
5IOD	5 V input/output open-drain
REFL	Input voltage levels referenced to V _{CCP} _VREF

FUNCTION TABLES

Strapping Selection Pin

STRAP (pin 54) ¹	MODE ¹	PIN NAME & (PIN NUMBER)
1 No connect	FLUSH	GPO_FLUSH_CACHE (4)
1 No connect	FLUSH	A20M (5)
1 No connect	FLUSH	INIT (6)
1 No connect	FLUSH	FLUSH_OUT_CPU (7)
1 No connect	FLUSH	INIT_OUT (8)
0 GND	GP	GP2_IN (4)
0 GND	GP	GP1_INB (5)
0 GND	GP	GP1_INA (6)
0 GND	GP	GP1_OUT (7)
0 GND	GP	GP2_OUT (8)

NOTE:

1. The pin is internally pulled up to default to FLUSH mode.

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TYPICAL APPLICATION

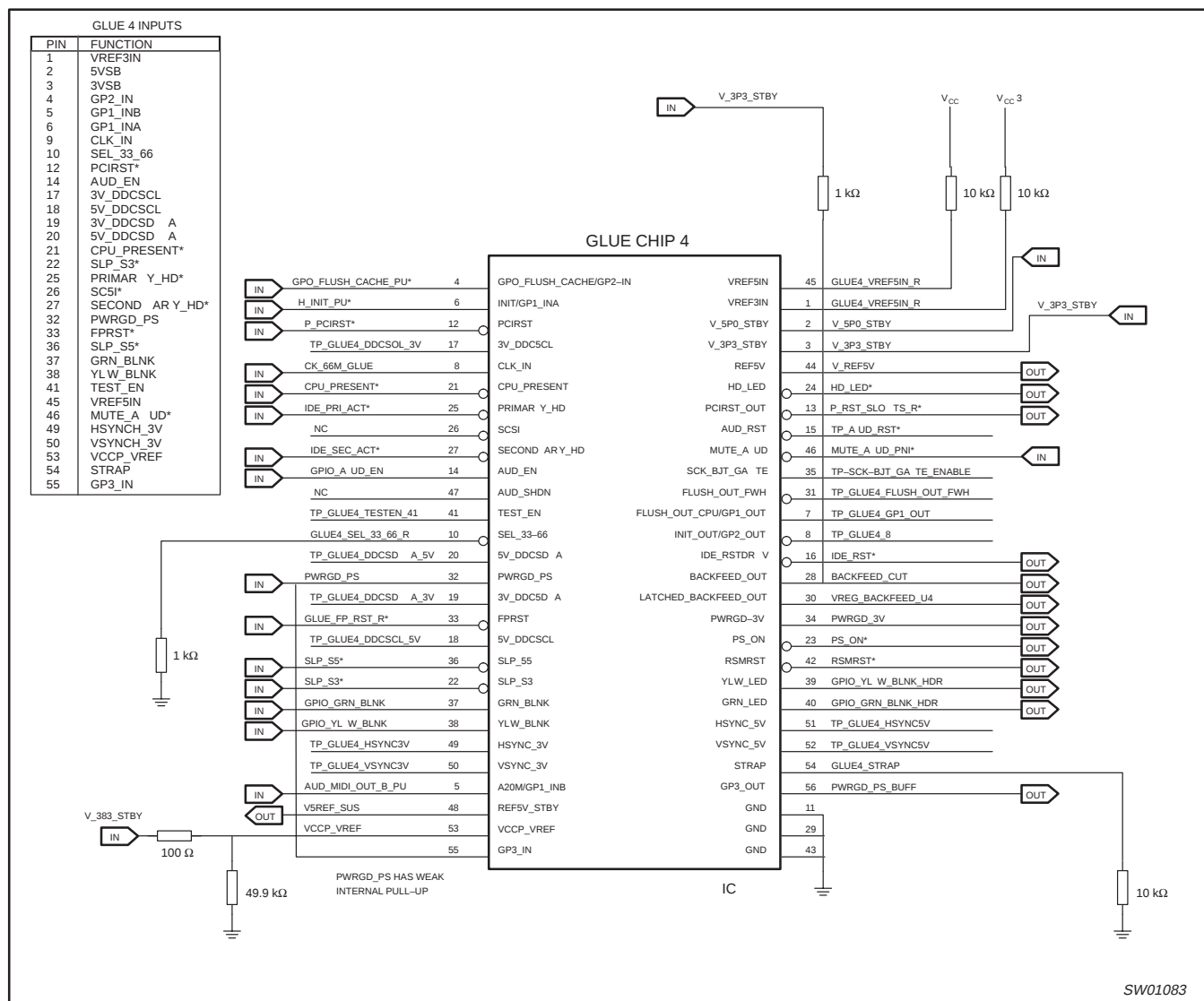


Figure 1. Typical application

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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V _{5P0_STBY}	DC 5.0V supply		−0.5	+6.0	V
V _{3P3_STBY}	DC 3.3V supply		−0.5	+6.0	V
V _{I (5V)}	DC input voltage (5 V pins)	Note 2	−0.5	V _{5P0_STBY} +0.5	V
V _{O (5V)}	Output voltage range (5 V pins)	Note 2	−0.5	V _{5P0_STBY} +0.5	V
V _{I (3.3V)}	DC input voltage (3.3 V pins)	Note 2	−0.5	V _{3P3_STBY} +0.5	V
V _{O (3.3V)}	Output voltage range (3.3 V pins)	Note 2	−0.5	V _{3P3_STBY} +0.5	V
SPD	Supply power dissipation			100	MW
ESD	Static Discharge voltage		2000		V
T _{STG}	Storage temperature range		−55	+150	°C
T _{OTR}	Operating Temperature Range		0	70	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under "recommended operating condition" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage rating may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{DD3}	DC 3.3 V supply voltage		3.0	3.6	V
V _{DDL}	DC 2.5 V supply voltage		4.75	5.25	V
V _I	DC input voltage		0	V _{DD3}	V
V _O	DC output voltage		0	V _{DDL} V _{DD3}	V
T _A	Operating ambient temperature range in free air		0	+70	°C

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DC CHARACTERISTICS

 $V_{_5P0_STBY} = 5\text{ V} \pm 5\%$; $V_{_3P3_STBY} = 3.3\text{ V} \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T _{amb} = 0 °C to +70 °C			
			MIN	TYP	MAX	
STRAP						
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
I _{IH}	Input leakage HIGH		−1		1	μA
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −3 mA	2.4			V
I _{IL}	Input leakage LOW		−88		−26	μA
AUD_EN						
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
I _{IL}	Input leakage LOW	V _{IL} = 0 V	−88		−26	μA
I _{IH}	Input leakage HIGH		−1		1	μA
PCIRST						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _L	Input leakage		−1		1	μA
Hys	Input hysteresis		400			mV
MUTE_AUD						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _{IH}	Input leakage HIGH		−1		1	μA
I _{IL}	Input leakage LOW	V _{IL} = 0 V	−88		−26	μA
VREF5IN						
V _{IH}	HIGH-level input voltage		0.85*V5P 0_STBY			V
V _{IL}	LOW-level input voltage				0.2*V5P 0_STBY	V
I _L	Input leakage		−1		1	μA
VREF3IN						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _L	Input leakage		−1		1	μA
PRIMARY_HD						
V _{IH}	HIGH-level input voltage		0.7*5VSB			V
V _{IL}	LOW-level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I _{IL}	Input leakage LOW	V _{IL} = 0 V	−88		−26	μA
I _{IH}	Input leakage HIGH	V _{IH} = 5VSB	−1		1	μA
SECONDARY_HD						
V _{IH}	HIGH-level input voltage		0.7*5VSB			V
V _{IL}	LOW-level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I _{IL}	Input leakage LOW	V _{IL} = 0 V	−88		−26	μA

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SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T _{amb} = 0 °C to +70 °C			
			MIN	TYP	MAX	
I _{IH}	Input leakage HIGH	V _{IH} = 5VSB	−1		1	μA
SCSI						
V _{IH}	HIGH-level input voltage		0.7*5VSB			V
V _{IL}	LOW-level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I _{IL}	Input leakage LOW	V _{IL} = 0 V	−88		−26	μA
I _{IH}	Input leakage HIGH	V _{IH} = 5VSB	−1		1	μA
FPRST						
V _{IH}	HIGH-level input voltage		0.7*5VSB			V
V _{IL}	LOW-level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I _{IL}	Input leakage LOW	V _{IL} = 0 V	−88		−26	μA
I _{IH}	Input leakage HIGH	V _{IH} = 5VSB	−1		1	μA
PWRGD_PS						
V _{IH}	HIGH-level input voltage		0.7*5VSB			V
V _{IL}	LOW-level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I _{IL}	Input leakage LOW	V _{IL} = 0 V	−88		−26	μA
I _{IH}	Input leakage HIGH	V _{IH} = 5VSB	−1		1	μA
GPO_FLUSH_CACHE/GP2_IN						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _L	Input leakage	V _{IL} = 0 V	−88		−26	μA
I _{IH}	Input leakage	V _{IH} = 5 V	−1		1	μA
INIT / GP1_INA (GP Mode)						
V _{IH}	HIGH-level input voltage	Part is strapped for GP mode	2.4			V
V _{IL}	LOW-level input voltage	Part is strapped for GP mode			0.8	V
I _L	Input leakage	Part is strapped for GP mode	−1		1	μA
VCCP_V _{ref}	Bias voltage	GP mode	1.95		2.1	V
INIT / GP1_INA (Flush Mode)						
V _{IH}	HIGH-level input voltage	FLUSH mode	1.5			V
V _{IL}	LOW-level input voltage	FLUSH mode			0.4	V
I _{IL}	Input leakage	FLUSH mode	−1		1	μA
VCCP_V _{ref}	Bias voltage	FLUSH mode	0.95		1.1	V

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SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T _{amb} = 0 °C to +70 °C			
			MIN	TYP	MAX	
A20M / GP1_INB						
V _{IH}	HIGH-level input voltage	FLUSH mode	1.5			V
V _{IL}	LOW-level input voltage	FLUSH mode			0.4	V
I _{IL}	Input leakage	FLUSH mode	−1		1	μA
VCCP_V _{ref}	Bias voltage	FLUSH mode	0.95		1.1	V
V _{IH}	HIGH-level input voltage	GP mode	2.4			V
V _{IL}	LOW-level input voltage	GP mode			0.8	V
I _L	Input leakage	GP mode	−1		1	μA
VCCP_V _{ref}	Bias voltage	GP mode	1.95		2.1	V
CLK_IN						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
Hys	Input hysteresis		250			mV
I _L	Input leakage		−1		1	μA
SEL_33_66						
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I _{IH}	Input leakage		−1		1	μA
I _{IL}	Input leakage	V _{IL} = 0 V	−88		−26	μA
SLP_S3						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I _L	Input leakage		−1		1	μA
SLP_S5						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I _L	Input leakage		−1		1	μA
CPU_PRESENT						
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
Hys	Input hysteresis		400			mV
I _{IH}	Input leakage	V _{IH} = 3VSB	−1		1	μA
I _{IL}	Input leakage	V _{IL} = 0 V	−88		−26	μA
TEST_EN						
V _{IH}	HIGH-level input voltage		0.7*5VSB			V
V _{IL}	LOW-level input voltage				0.2*5VSB	V
Hys	Input hysteresis		400			mV
I _{IH}	Input leakage	V _{IL} = 0 V	−1		1	μA
I _{IL}	Input leakage	V _{IH} = 5VSB	20		88	μA

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SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T _{amb} = 0 °C to +70 °C			
			MIN	TYP	MAX	
HSYNC_3V						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _L	Input leakage		−1		1	μA
VSYNC_3V						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _L	Input leakage		−1		1	μA
GRN_BLNK						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _{IH}	Input leakage		−1		1	μA
I _{IL}	Input leakage	V _{IL} = 0 V	−88		−26	μA
YLW_BLNK						
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
I _{IH}	Input leakage		−1		1	μA
I _{IL}	Input leakage	V _{IL} = 0 V	−88		−26	μA
GP3_IN						
V _{IH}	HIGH-level input voltage		2.2			V
V _{IL}	LOW-level input voltage				0.8	V
I _L	Input leakage		−1		1	μA
AUD_RST						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −3 mA	2.4			V
I _{OZ}	Off state output current		−1		1	μA
AUD_SHDN						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −6 mA	2.4			V
I _{OZ}	Off state output current		−1		1	μA
REF5V						
V _{OUT5}	LOW-level output voltage	V _{REF5in} > 1.5 V	V _{REF5in} − 0.05		V _{REF5in} + 0.05	V
V _{OUT3}	HIGH-level output voltage	V _{REF3in} > 1.5 V	V _{REF3in} − 0.05		V _{REF3in} + 0.05	V
I _{OUTL}	Off state output current		−20		20	μA
REF5V_STBY						
V _{OUT5}	LOW-level output voltage	V_5P0_STBY > 1.5 V	V_5P0_STBY − 0.05		V_5P0_STBY + 0.05	V
V _{OUT3}	HIGH-level output voltage	V_5P0_STBY > 1.5 V	V_5P0_STBY − 0.05		V_5P0_STBY + 0.05	V
I _{OUTL}	Off state output current		−20		20	μA
HD_LED						
V _{OL}	LOW-level output voltage	I _{OL} = 12 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA

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SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T _{amb} = 0 °C to +70 °C			
			MIN	TYP	MAX	
IDE_RSTDRV						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −6 mA	2.4			V
I _{OZ}	Off state output current		−1		1	μA
PCIRST_OUT						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −3 mA	2.4			V
I _{OZ}	Off state output current		−1		1	μA
PRWGD_3V						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −3 mA	2.4			V
I _{OZ}	Off state output current		−1		1	μA
INIT_OUT / GP2_OUT						
V _{OL}	LOW-level output voltage	I _{OL} = 12 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA
FLUSH_OUT_CPU / GP1_OUT						
V _{OL}	LOW-level output voltage	I _{OL} = 12 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA
BACKFEED_CUT						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA
FLUSH_OUT_FWH						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA
LATCHED_BACKFEED_CUT						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −6 mA	2.4			V
I _{OZ}	Off state output current		−1		1	μA
PS_ON						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA
RSMRST						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −3 mA	2.4			V
I _{OZ}	Off state output current		−1		1	μA
VTRIP	5VSB LOW trip voltage		1.8		3.5	V
SCK_BJT_GATE						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA

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SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			T _{amb} = 0 °C to +70 °C			
			MIN	TYP	MAX	
3V_DDCSDA						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _H	Input leakage	5V_DDCSDA = V _{DD}	−1		2.5	μA
I _{OZ}	Off state output current		−1		1	μA
5V_DDCSDA						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _H	Input leakage	3V_DDCSDA = V _{DD}	−1		2.5	μA
I _{OZ}	Off state output current		−1		1	μA
3V_DDCSCL						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _H	Input leakage	5V_DDCSCL = V _{DD}	−1		2.5	μA
I _{OZ}	Off state output current		−1		1	μA
5V_DDCSCL						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
I _H	Input leakage	3V_DDCSCL = V _{DD}	−1		2.5	μA
I _{OZ}	Off state output current		−1		1	μA
HSYNC_5V						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −6 mA	3.8			V
I _{OZ}	Off state output current		−1		1	μA
VSYNC_5V						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA			0.4	V
V _{OH}	HIGH-level output voltage	I _{OH} = −6 mA	3.8			V
I _{OZ}	Off state output current		−1		1	μA
GRN_LED / YLW_LED						
V _{OL}	LOW-level output voltage	I _{OL} = 24 mA			0.4	V
I _{OZ}	Off state output current		−1		1	μA
GP3_OUT						
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA				
I _{OZ}	Off state output current		−1		1	μA

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AC CHARACTERISTICS

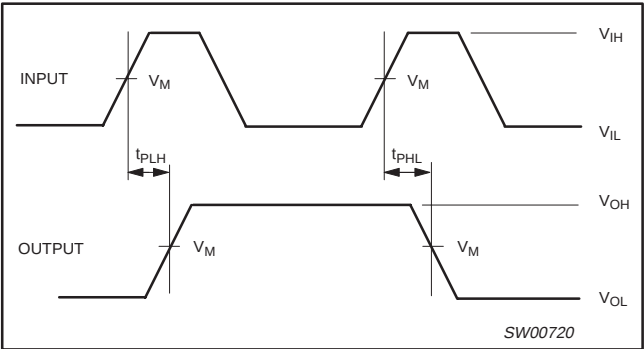
 $V_{CC1} = 3.3\text{ V}$; $V_{CC} = 5.0\text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	NOTES
		T _{amb} = 0 °C to +70 °C				
		MIN	TYP	MAX		
t _{RESET}	RSMRST	4.0		100	ms	
t _{RESET_FALL}	RSMRST			100	ns	
t _{PHL} /t _{PLH}	Propagation Delay AUD_EN to AUD_RST PCIRST to AUD_RST PCIRST to IDE_RSTDRV PCIRST to PCIRST_OUT	1.0		11.0	ns	
t _{PLH} /t _{PHL}	Propagation Delay MUTE_AUD to MUTE_SHDN	2.5		6.0	ns	
t _{PLH} /t _{PHL}	Propagation Delay PWRGD_PS to PWRGD_3V FPRST to PWRGD_3V	4.5		11.0	ns	
t _{PLH} /t _{PHL}	Propagation Delay HSYNC_3V to HSYNC_5V VSYNC_3V to VSYNC_5V	2.0		5.0	ns	
t _{PLH} /t _{PHL}	Propagation Delay PWRGD_PS to SCK_BJT_GATE FPRST to SCK_BJT_GATE	1.0		6.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay PRIMARY_HD to HD_LED PRIMARY_HD to HD_LED PRIMARY_HD to HD_LED	1.0		5.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay GP1_INA to GP1_OUT GP2_INA to GP1_OUT	3.0		25.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay GP2_IN to GP2_OUT	3.0		7.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay GP3_IN to GP3_OUT	1.0		4.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay SLP_S3 to BACKFEED_OUT PRWGD_PS to BACKFEED_OUT	1.0		6.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay CPU_PRESENT to PS_ON	2.0		10.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay SLP_S3 to PS_ON	2.0		10.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay BACKFEED_OUT to LATCHED_BACKFEED_OUT	2.0		11.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay SLP_S5 to YLW_LED SLP_S5 to GRN_LED YLW_BLNK to YLW_LED GRN_BLNK to GRN_LED	1.0		5.0	ns	
t _{PLZ} /t _{PZL}	Open Drain Prop Delay 3V_DDOSDA to 5V_DDOSDA 3V_DDOSDA to 5V_DDOSDA	1.0		5.0	ns	
t _r , t _f	Rise and Fall Times HSYNC_5V VSYNC_5V	3.5			ns	
t _r , t _f	Rise and Fall Times LATCHED_BACKFEED_OUT			1.0	μs	

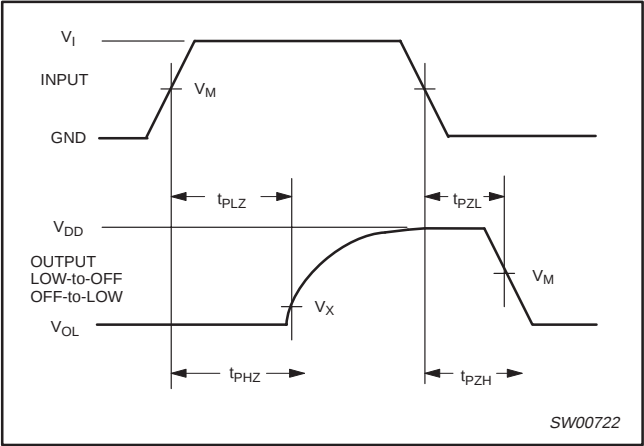
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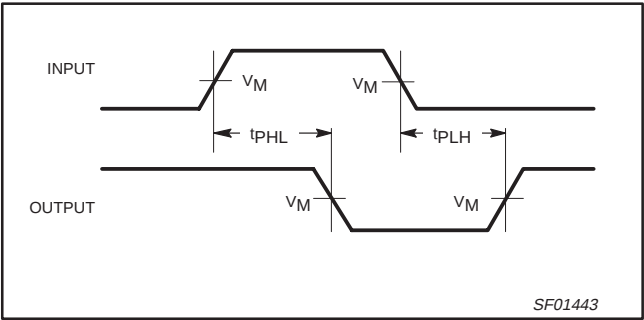
WAVEFORMS



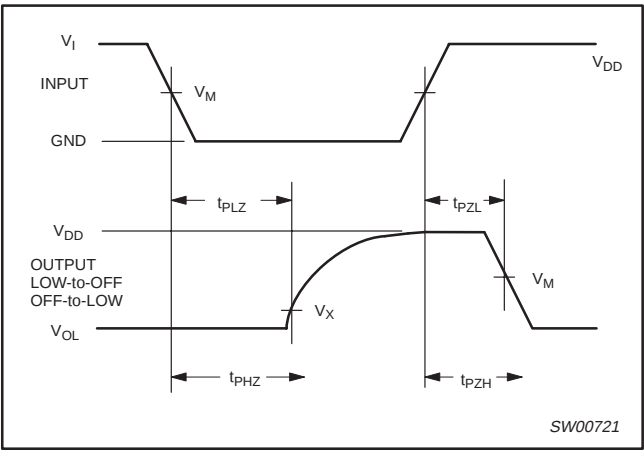
Waveform 1.



Waveform 2.



Waveform 3.



Waveform 4.

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5V REFERENCE GENERATION

Supply	REF5V
$V_{REF5IN} < V_{REF3IN}$	V_{REF3IN}
$V_{REF5IN} > V_{REF3IN}$	V_{REF5IN}

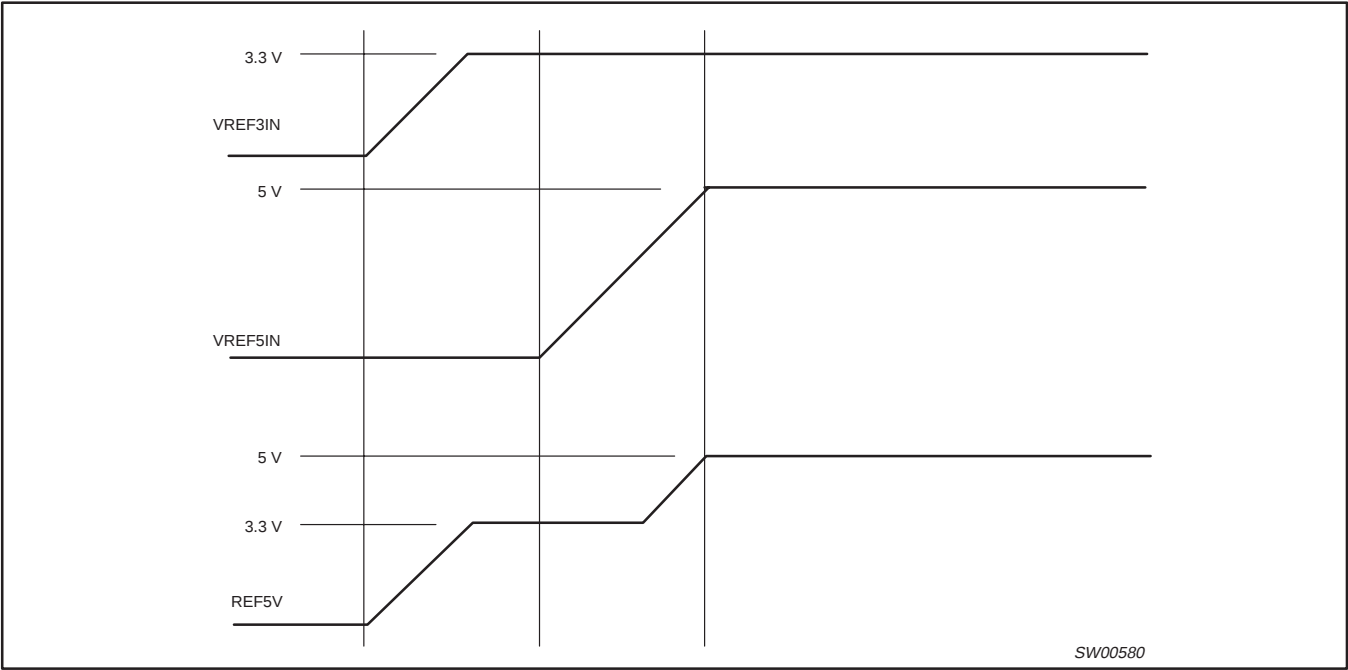


Figure 1. REF5V when VREF3IN ramps before VREF5IN

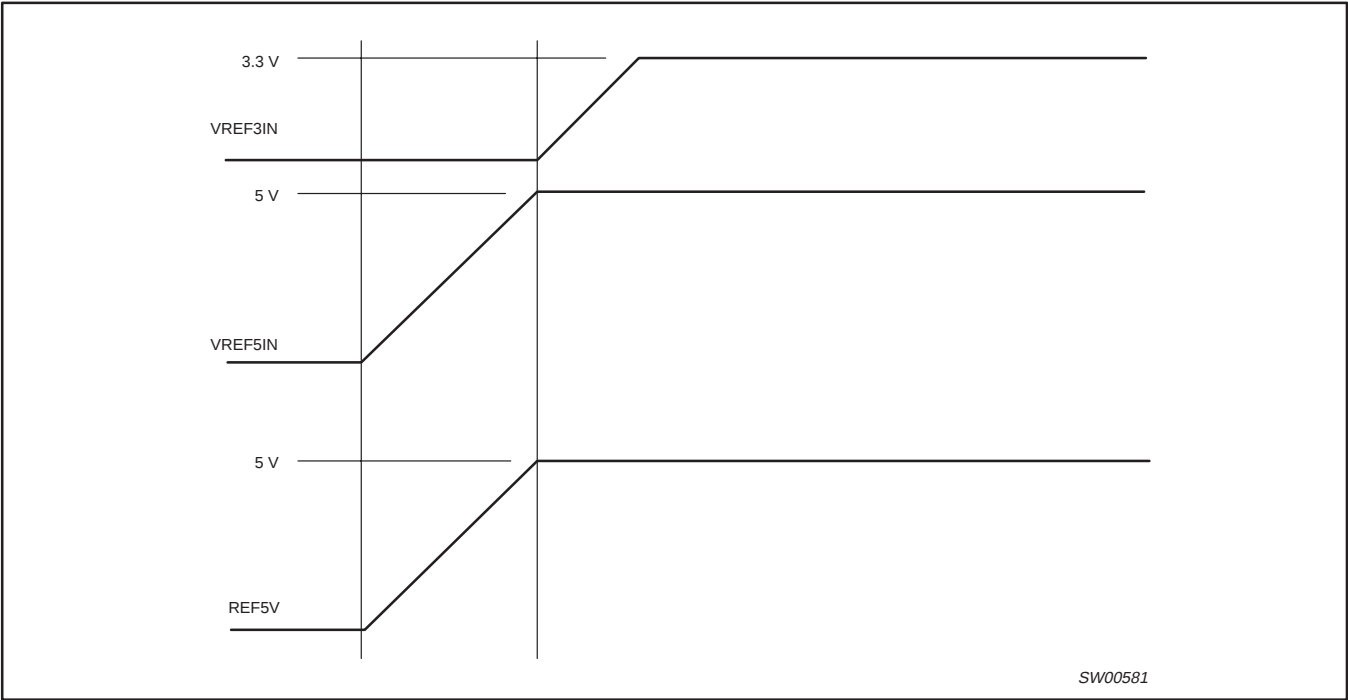


Figure 2. REF5V when VREF5IN ramps before VREF3IN

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5V STANDBY REFERENCE GENERATION

Standby Supply	REF5V_STBY
$V_{5PO_STBY} < V_{3P3_STBY}$	V_{3P3_STBY}
$V_{5PO_STBY} > V_{3P3_STBY}$	V_{5PO_STBY}

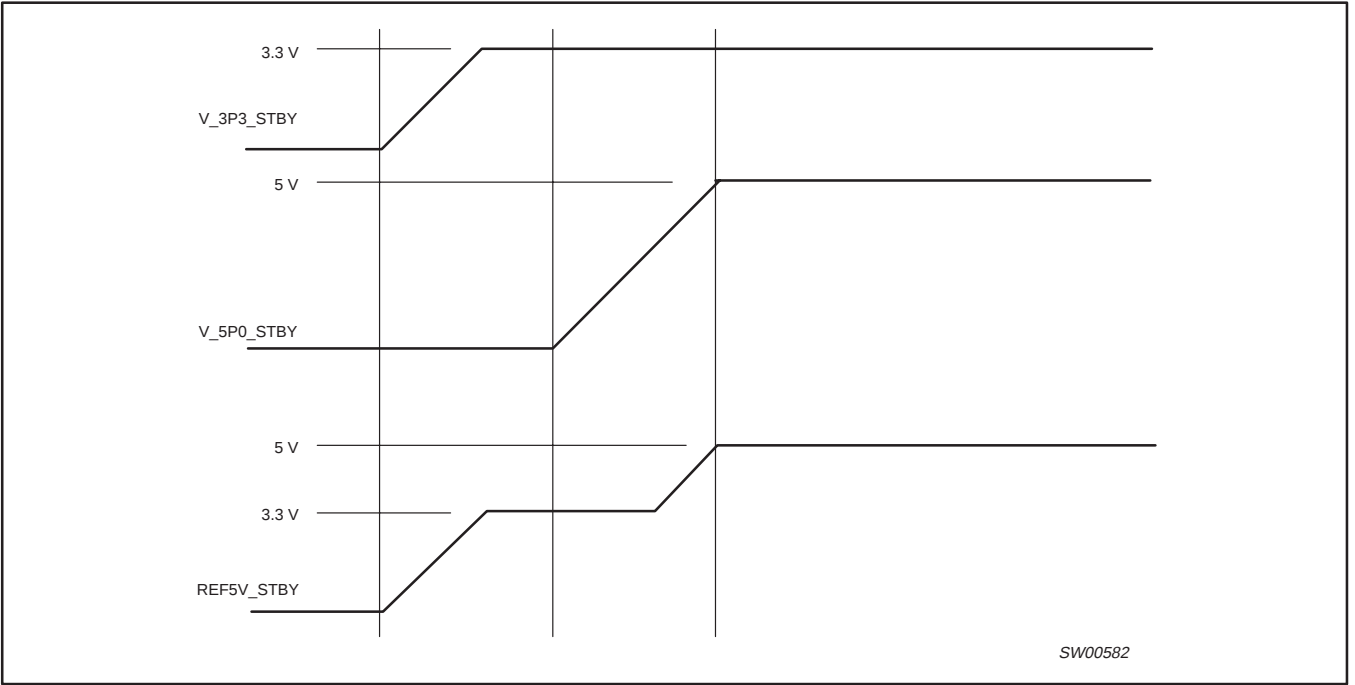


Figure 3. REF5V_STBY when V_3P3_STBY ramps before V_5PO_STBY

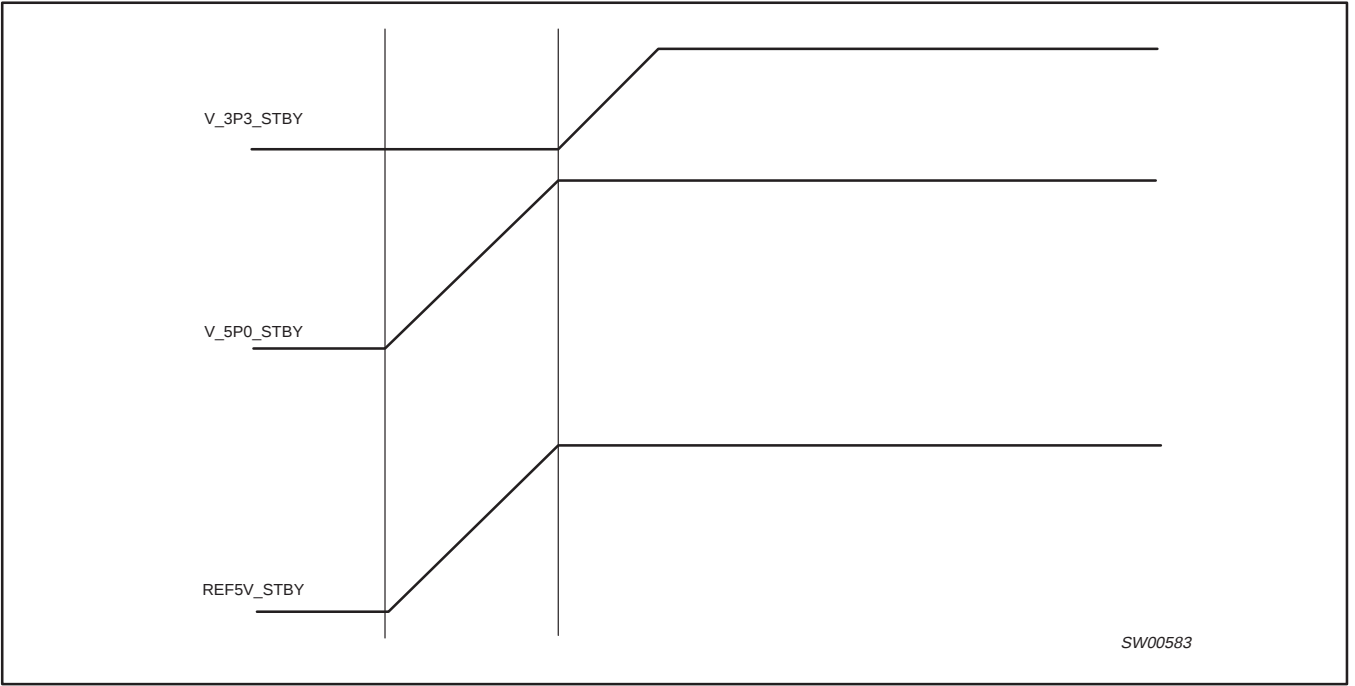


Figure 4. REF5V_STBY when V_5PO_STBY ramps before V_3P3_STBY

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FLUSH OUT* / INIT OUT* CIRCUIT

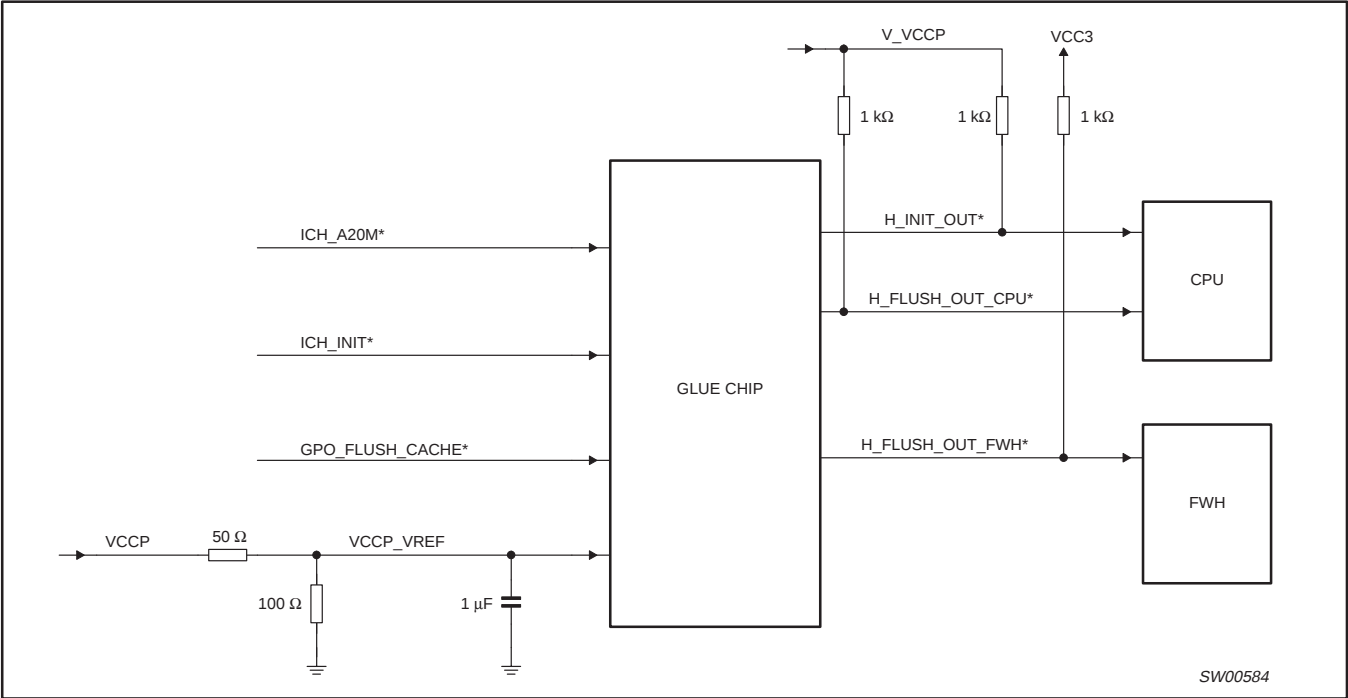


Figure 5. Block diagram for FLUSH_OUT*/INIT_OUT* circuit

Case	A20M*	GPO FLUSH CACHE*	INIT*	FLUSH OUT CPU*	FLUSH OUT FWH*	INIT OUT*
1	1	falling edge	0	0 (for t1)	0 (for t1)	0, Hi-Z, then 0 (delayed by t1-t, then active for 2*t)
2	1	falling edge	1	0 (for t1)	0 (for t1)	Hi-Z, 0 (delayed by t1-t, then active for 2*t)
3	X	1	0	Hi-Z	Hi-Z	0
4	X	1	1	Hi-Z	Hi-Z	Hi-Z
5	0	falling edge	1	Hi-Z	Hi-Z	Hi-Z
6	0	falling edge	0	Hi-Z	Hi-Z	0

NOTE:
1. Nominal value timings with tolerances are listed in the DC Characteristics table for t and t1. All Hi-Z outputs are shown as 1's or HIGH in the following diagrams.

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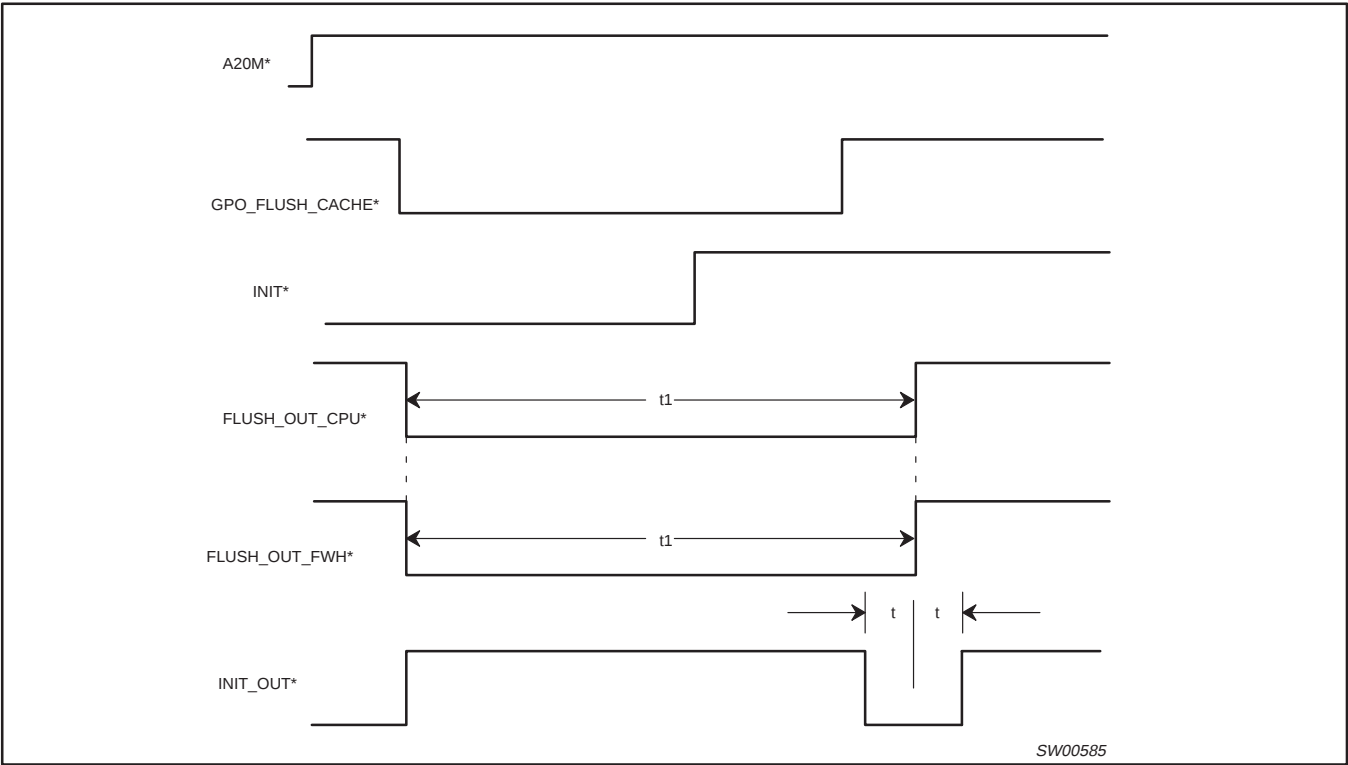


Figure 6. Waveforms for Case 1

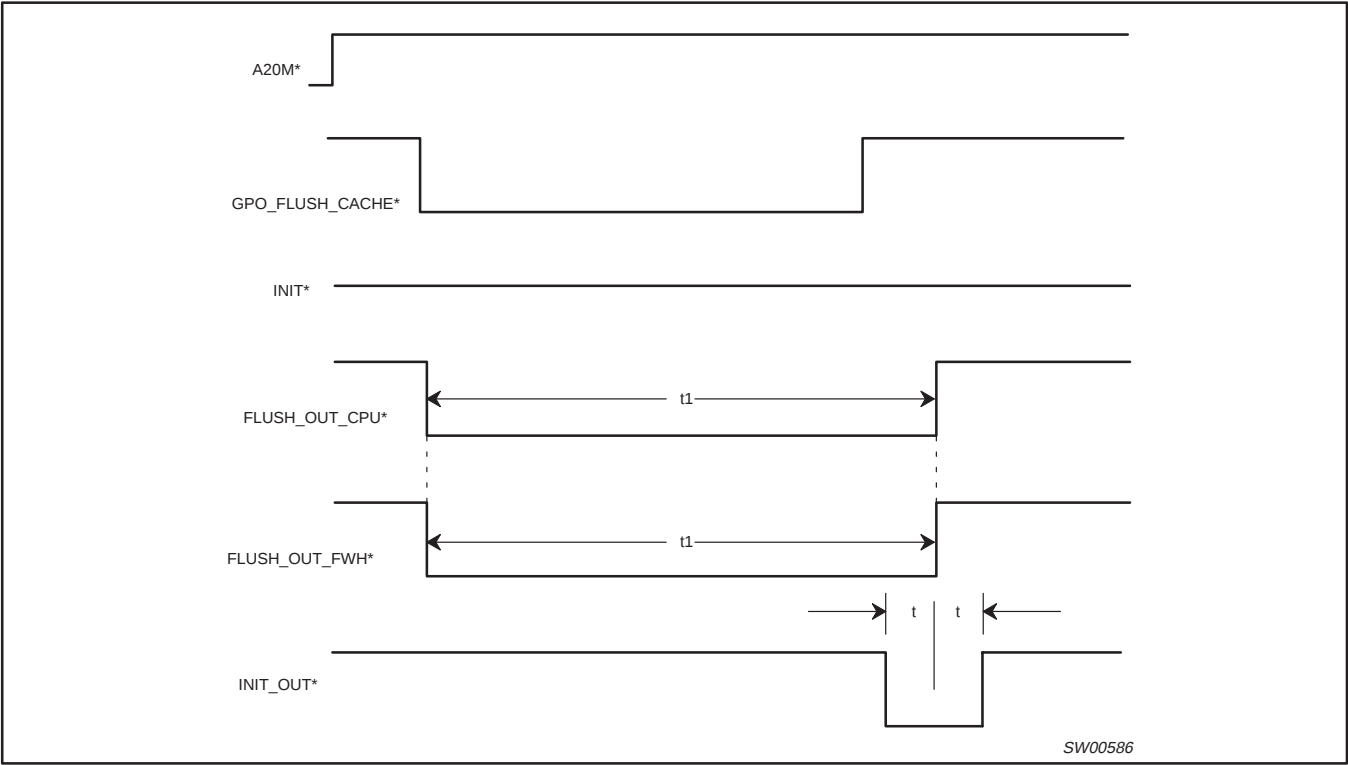


Figure 7. Waveforms for Case 2

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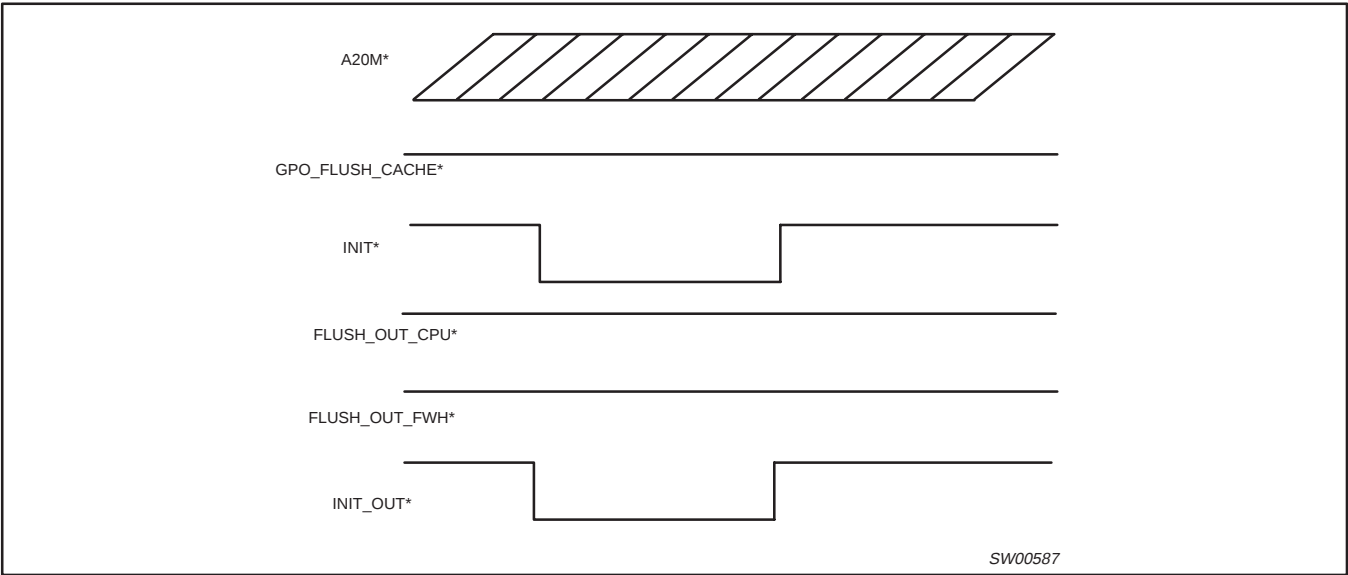


Figure 8. Waveforms for Case 3

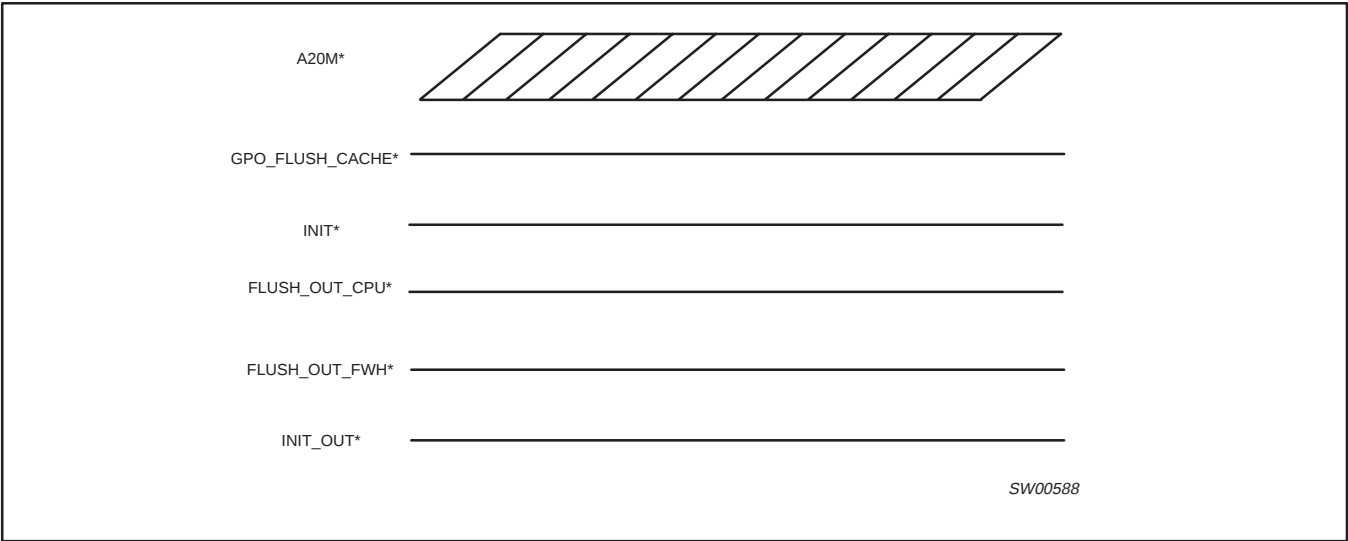


Figure 9. Waveforms for Case 4

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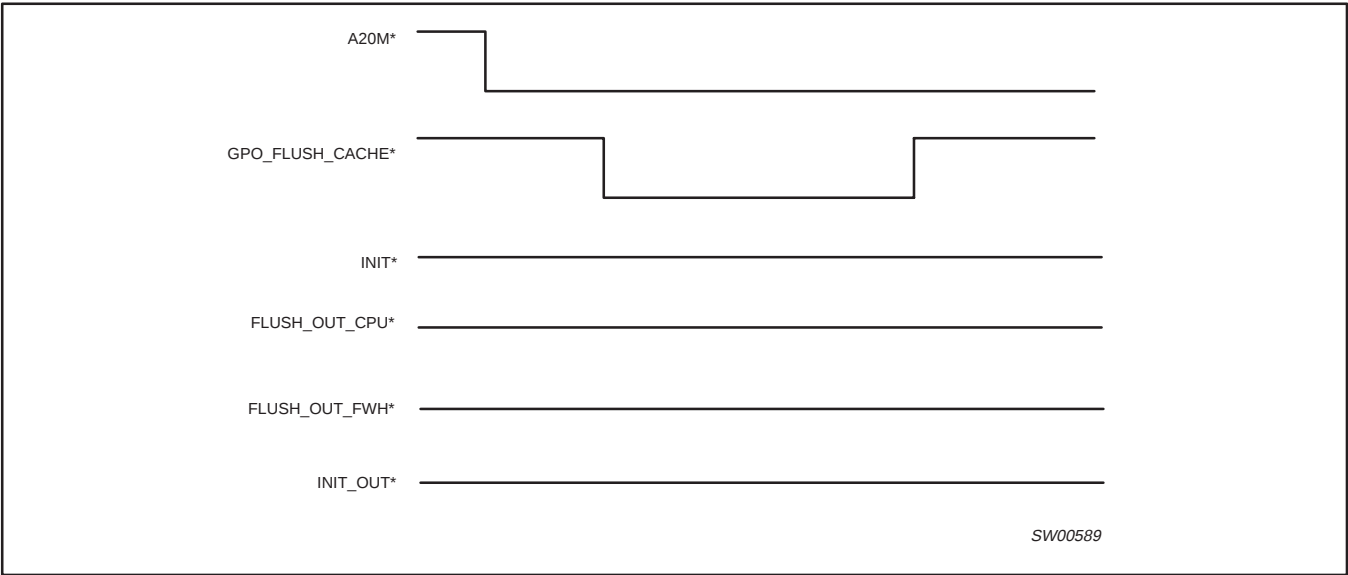


Figure 10. Waveforms for Case 5

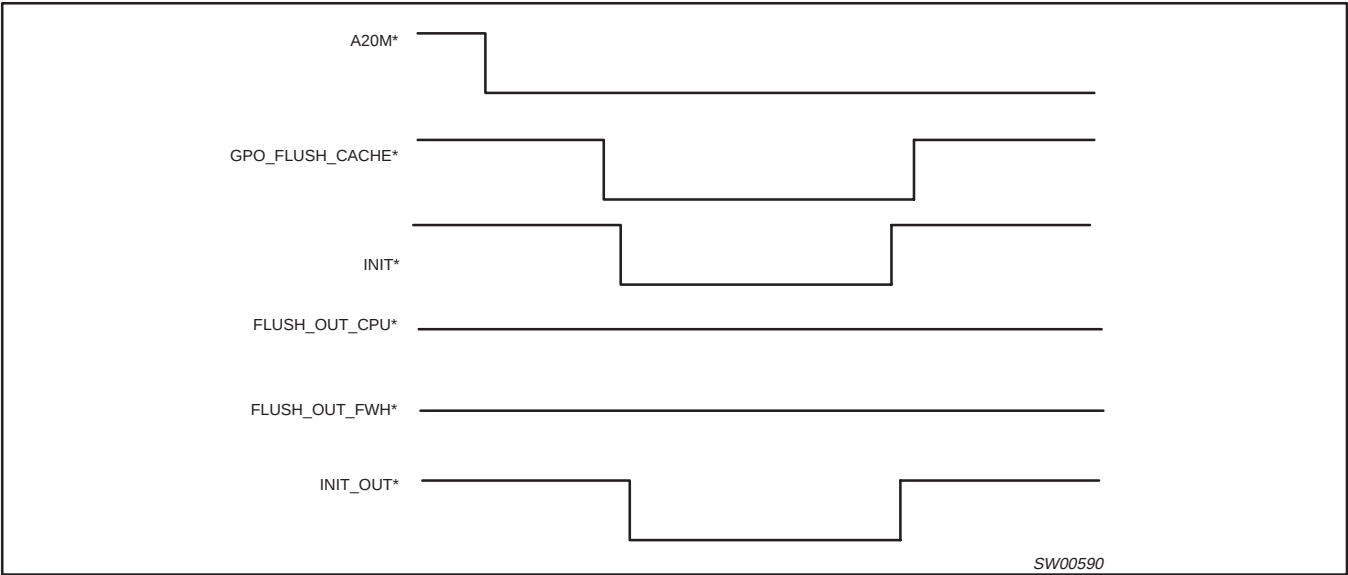


Figure 11. Waveforms for Case 6

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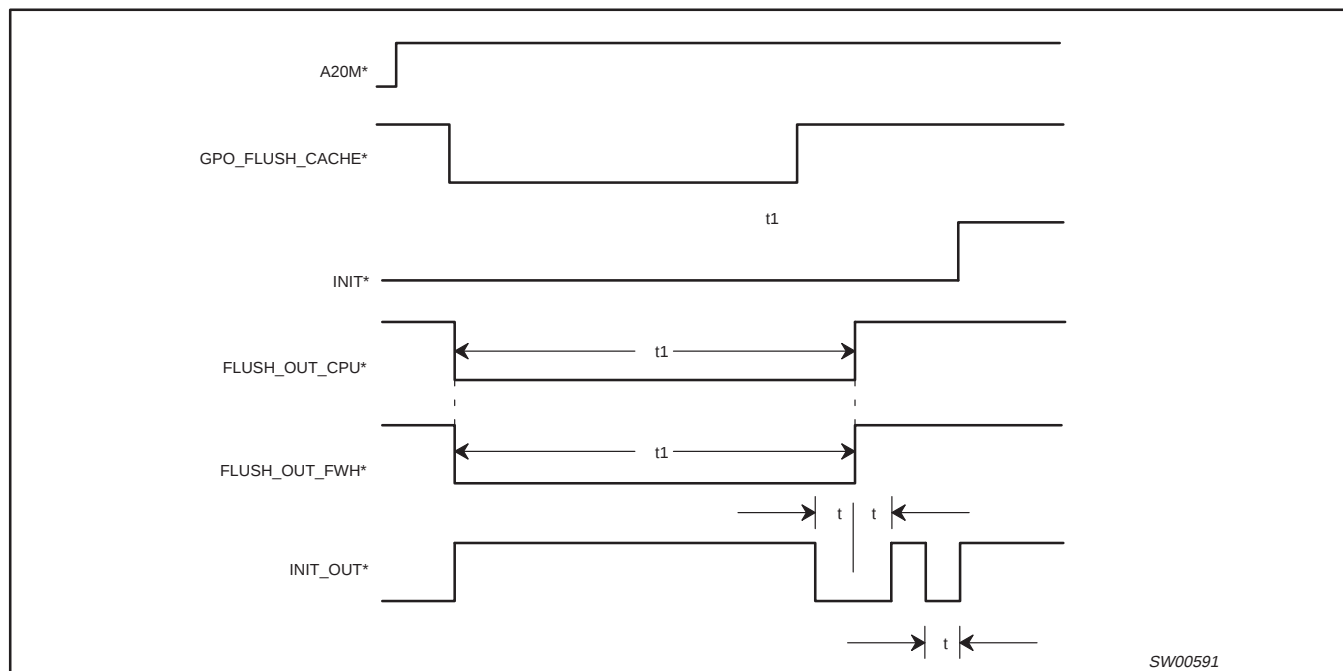


Figure 12. Waveforms for Case 7

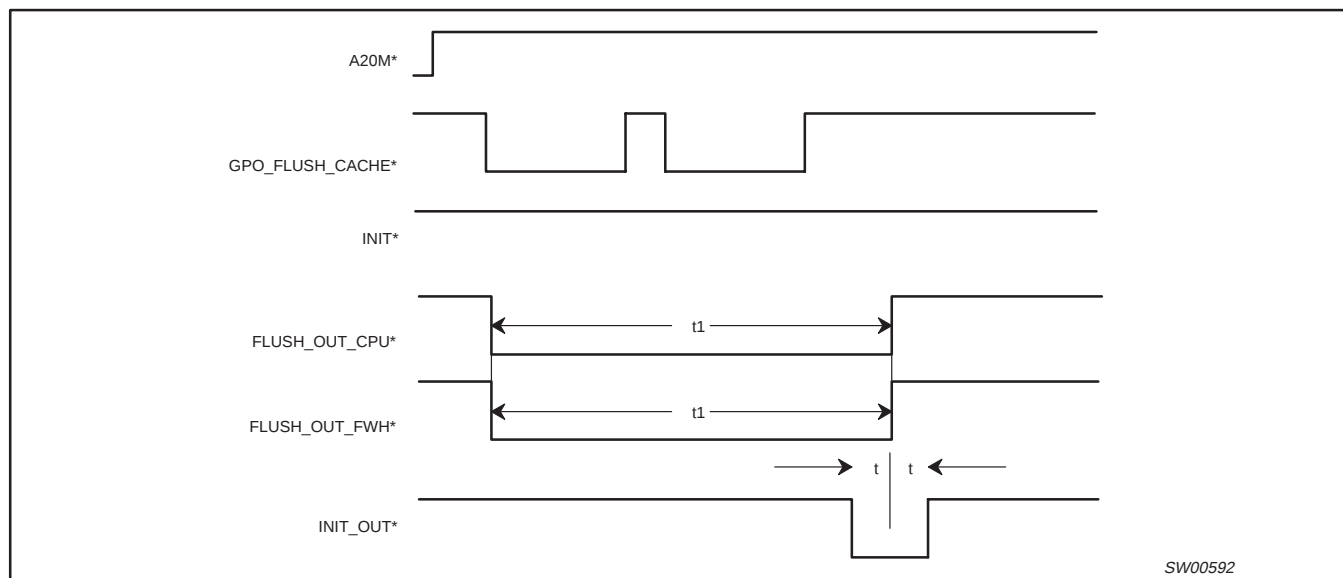


Figure 13. Waveforms for boundary GPO_FLUSH_CACHE* Case

- Timings should remain the same for both a 66 MHz or 33 MHz CLK_IN input.
- The boundary condition for INIT listed above, is a special case where immediately following the FLUSH_OUT*, INIT_OUT* cycle, the ICH2 asserts INIT* into the Glue Chip.
- The boundary condition for GPO_FLUSH_CACHE* listed above, is a special case where immediately following the first assertion of GPO_FLUSH_CACHE*, the GPO is de-asserted, then re-asserted again before the timings have had a chance to complete.

NOTE:

1. Nominal timing values with tolerances are listed in the DC Characteristics table.

GPO_FLUSH_CACHE* – input to logic, GPO from the ICH2, programmed active LOW.

INIT* – input to logic, INIT* signal from the ICH2.

A20M* – input to logic, A20M* signal from the ICH2.

FLUSH_OUT_CPU* – output of logic, route to CPU FLUSH* pin.

FLUSH_OUT_FWH* – output of logic, routed to FWH INIT* pin.

INIT_OUT* – output of logic, routed to CPU INIT* pin.

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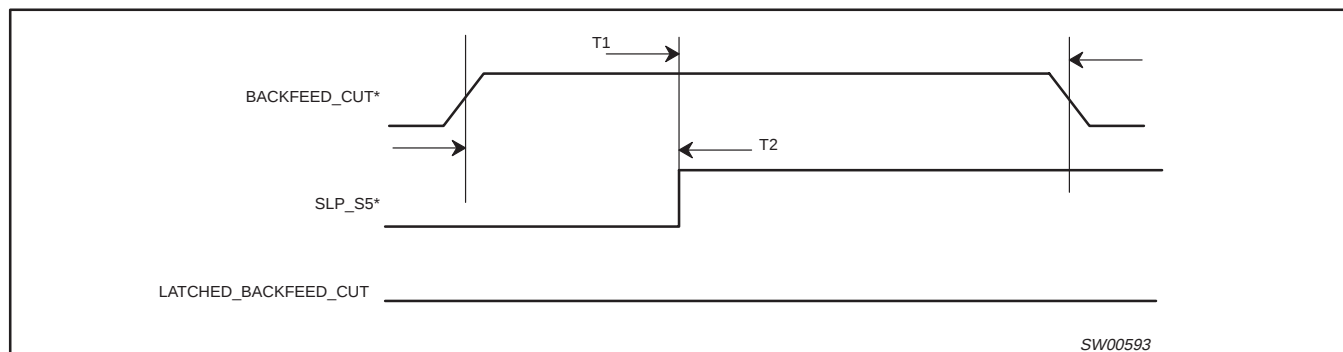


Figure 14. Power up signal sequencing

Power up signal sequencing is shown in Figure 14. BACKFEED_CUT* is following the power rail up to its final value. LATCHED_BACKFEED_CUT should stay LOW, never turning on. SLP_S5* goes to its HIGH value when the power rails have stabilized, ~25 msec after power on. BACKFEED_CUT* is pulled LOW a period T1 after SLP_S5* goes HIGH. T1 can be as short as 1msec. Typical measured values are ~200 msec. T1 and T2 are guaranteed by the inherent design of the system and are not controlled by Glue Chip.

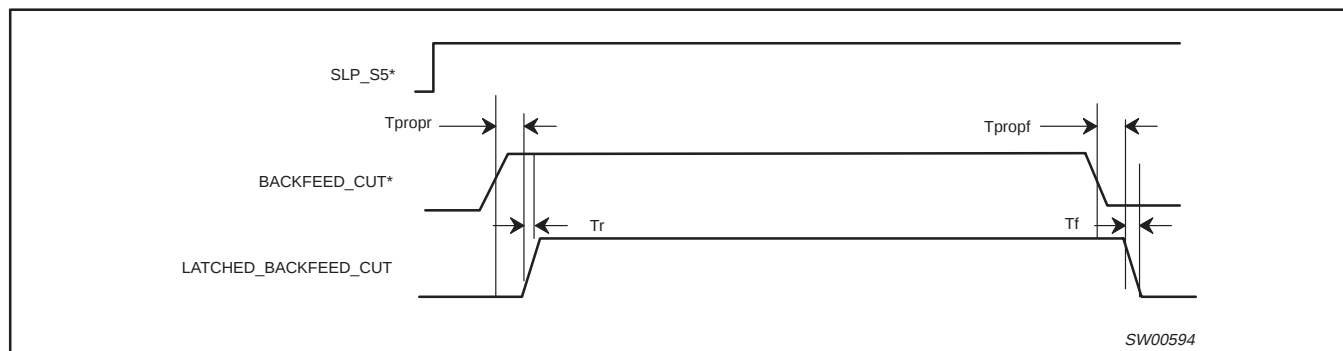


Figure 15. 1st sequence timing

The first possible sequence is with SLP_S5* staying HIGH and BACKFEED_CUT* transitioning from LOW to HIGH, remaining HIGH for an undetermined period and then going back to LOW and the system is back at the end of the power-up sequence. The power-up sequence is shown in Figure 15. During these BACKFEED_CUT* transitions, the propagation delays, rise and fall times, and going into regulation times LATCHED_BACKFEED_CUT are as described in Figure 16. The first sequence starts can start at the end of the power-up sequence at any time.

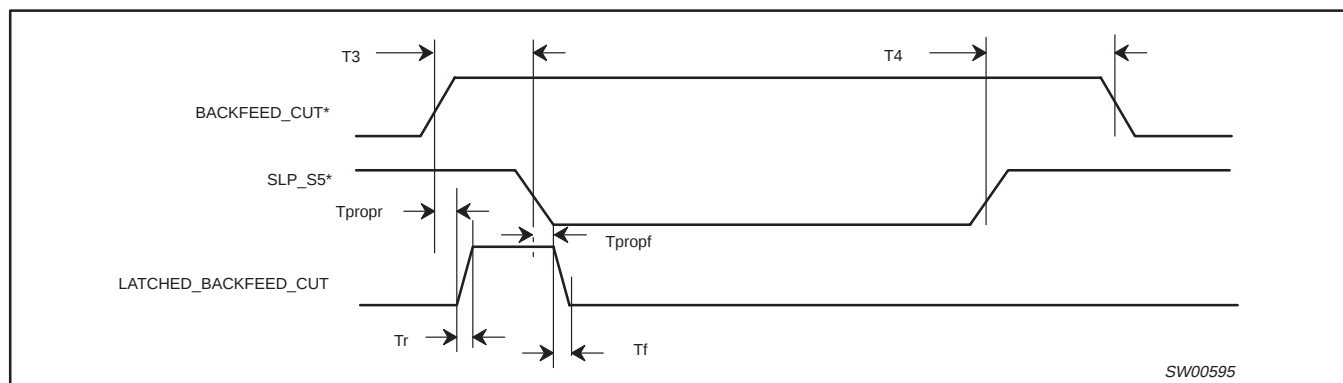


Figure 16. 2nd sequence timing

Signal sequencing for the second possible sequence is shown in Figure 16. BACKFEED_CUT* goes from LOW to HIGH and SLP_S5* goes from HIGH to LOW, 30 μ sec to 65 μ sec (T3) later. LATCHED_BACKFEED_CUT goes HIGH when BACKFEED_CUT* goes HIGH and then LATCHED_BACKFEED_CUT returns to LOW when SLP_S5* goes LOW. BACKFEED_CUT* stays HIGH and SLP_S5* stays LOW for an indeterminate time and then SLP_S5* will go HIGH. A minimum of 1msec (T4) later, BACKFEED_CUT* will go LOW and the system is back at the end of the power-up sequence. Typical measured values of T4 are ~250 msec. During all transitions, the propagation delays, rise and fall times, and going into regulation times for LATCHED_BACKFEED_CUT are as described in Figure 16. The first sequence starts can start at the end of the power-up sequence at any time.

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RSMRST* GENERATION

RSMRST* is a delayed 3.3 V hysteresis copy of V_5PO_STBY. RSMRST* is delayed going inactive from the rising edge of V_5PO_STBY by 32 ms, nominal. This delay starts when V_5PO_STBY hits the trip point. There is minimal delay on the falling edge.

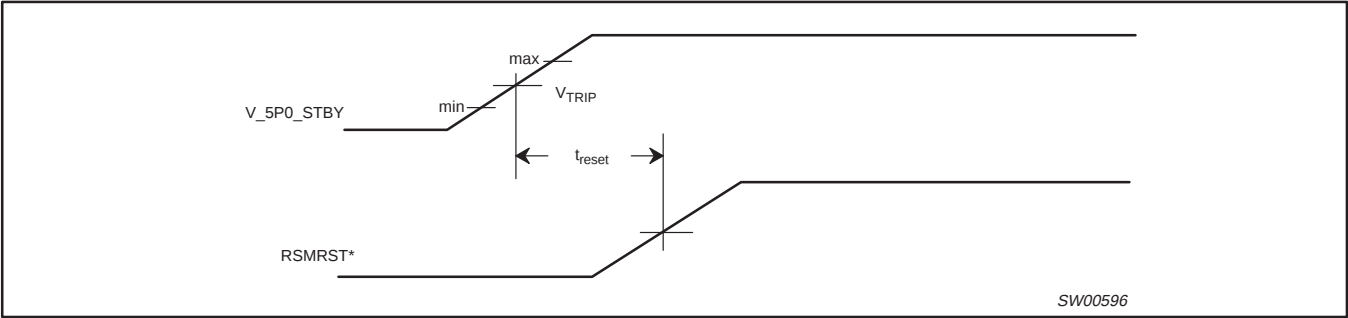


Figure 17. Resume reset functionality

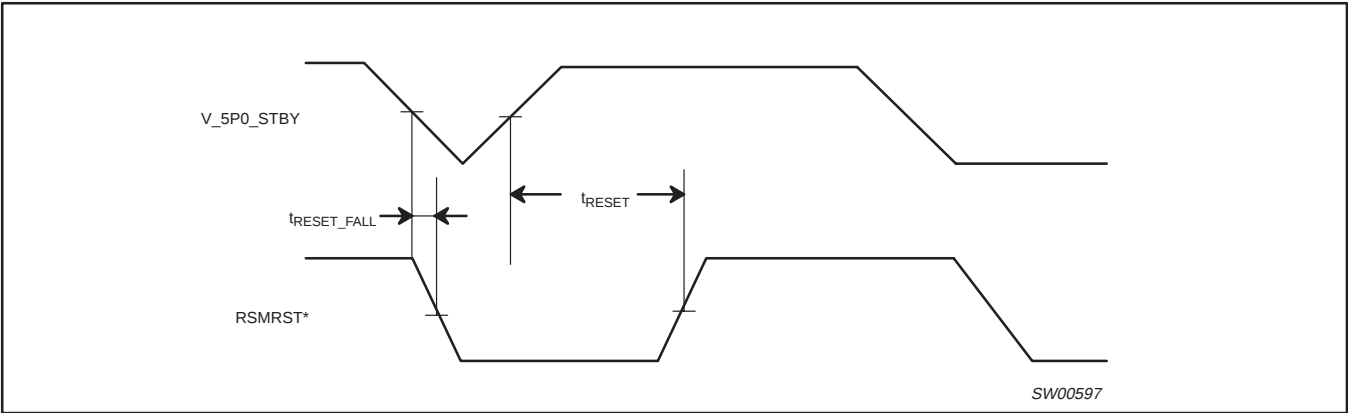


Figure 18. Resume reset functionality during brown out

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AUDIO-DISABLE

AUD_EN	PCIRST	AUD_RST
0	0	0
0	1	0
1	0	0
1	1	1

MUTE AUDIO CIRCUIT

MUTE_AUD	AUD_SHDN
0	1
1	0

HD SINGLE COLOR LED DRIVER

PRIMARY_HD	SECONDARY_HD	SCSI	HD_LED
0	0	0	0
0	X	X	0
X	0	X	0
X	X	0	0
1	1	1	HI-Z

IDE RESET SIGNAL GENERATION AND PCIRST DRIVE STRENGTH

PCIRST	IDE_RSTDRV ¹	PCIRST_OUT
0	0	0
1	1	1

NOTE:

1. IDE_RSTDRV is a 5 V copy of PCIRST. PCIRST_OUT is a 3.3 V copy of PCIRST.

PWRGD SIGNAL GENERATION

FPRST	PWRGD_PS	PWRGD_3V
0	0	0
0	1	0
1	0	0
1	1	1

FLUSH_OUT / INIT_OUT CIRCUIT

CASE	A20M	GPO_FLUSH_CACHE	INIT	FLUSH_OUT_CPU	FLUSH_OUT_FWH	INIT_OUT
1	1	Falling edge	0	0(for t1)	0(for t1)	0, HI-Z, then 0 (delayed by t1-t, then active for 2*t)
2	1	Falling edge	1	0(for t1)	0(for t1)	HI-Z, 0 (delayed by t1-t, then active for 2*t)
3	X	1	0	HI-Z	HI-Z	0
4	X	1	1	HI-Z	HI-Z	HI-Z
5	0	Falling edge	1	HI-Z	HI-Z	HI-Z
6	0	Falling edge	0	HI-Z	HI-Z	0

CLK_IN AND SEL_33_66

SEL_33_66	CLK_IN RATE
0	66 MHz
1	33 MHz

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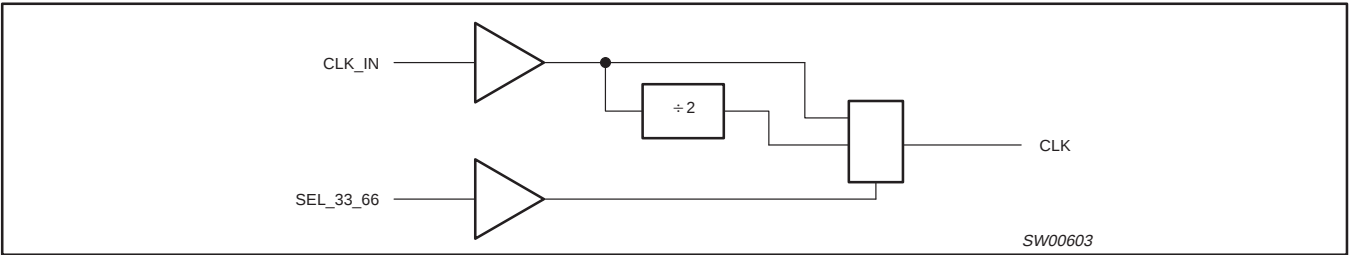


Figure 19.

GP_IN/GP_OUT GENERAL PURPOSE GATES

GP1_INA	GP1_INB	GP1_OUT
0	0	1
0	1	1
1	0	1
1	1	0

GP_IN/GP_OUT GENERAL PURPOSE GATES (continued)

GP2_IN	GP2_OUT
0	1
1	0

GP_IN/GP_OUT GENERAL PURPOSE GATES (continued)

GP3_IN	GP3_OUT
0	0
1	1

POWER SEQUENCING / BACKFEED_CUT

PWRGD_PS	SLP_S3	BACKFEED_CUT
0	0	Hi-Z
0	1	Hi-Z
1	0	Hi-Z
1	1	0

POWER SUPPLY TURN-ON CIRCUIT

SLOT0CC	SLP_S3	SLP_S3A
0	0	Hi-Z
0	1	0
1	0	Hi-Z
1	1	Hi-Z

RAMBUS_SCK_BJT

PWRGD_3V	SCK_BJT_GATE
0	Hi-Z
1	0

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VGA DCC VOLTAGE TRANSLATION

3V_DDCSDA	3V_DDCSCL	5V_DDCSDA	5V_DDCSCL
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

HSYNC / VSYNC VOLTAGE TRANSLATION

HSYNC_3V	HSYNC_5V	VSYNC_3V	VSYNC_5V
0	0	0	0
1	1	1	1

POWER LED DRIVER

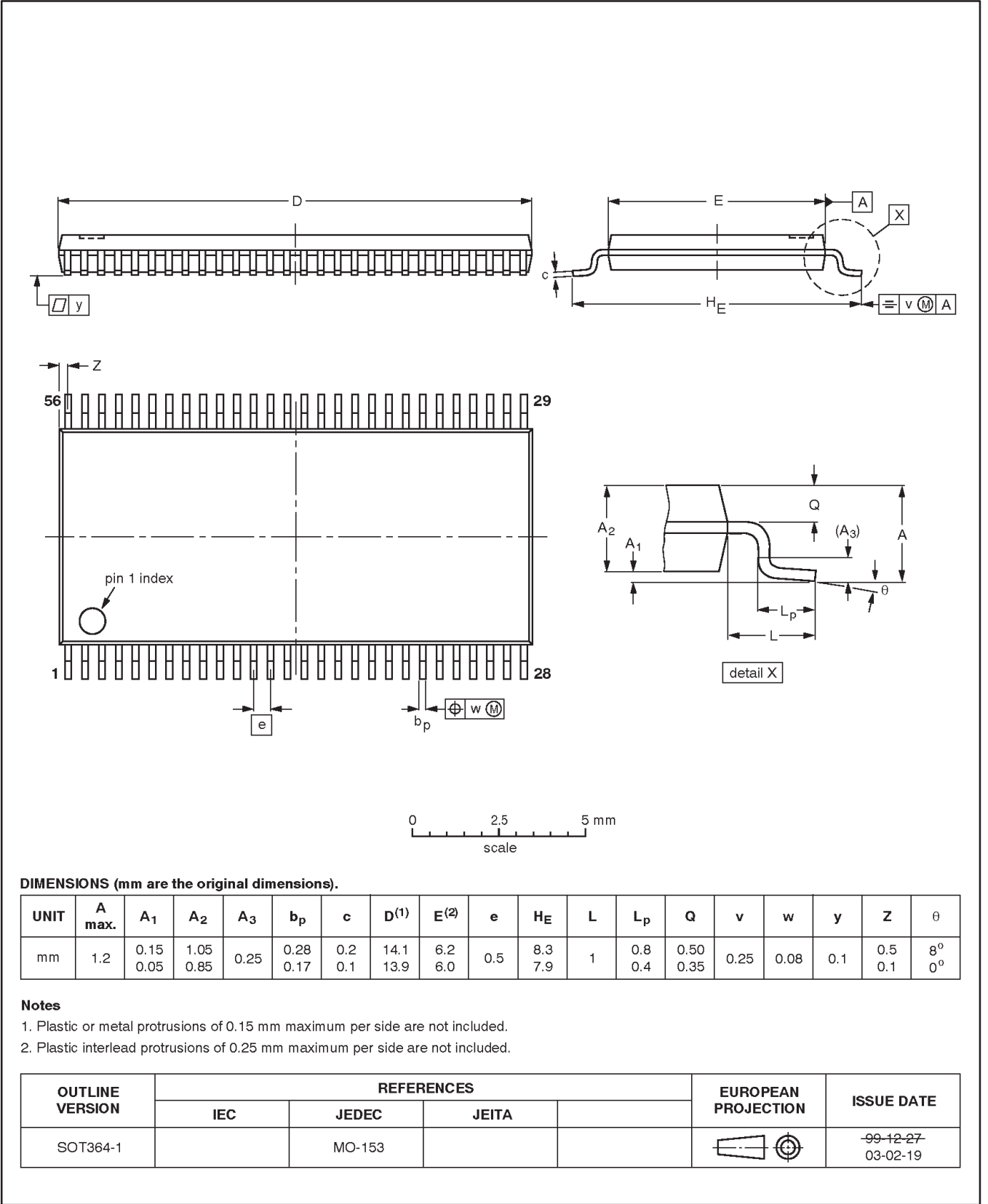
YLW_BLNK	SLP_S5	YLW_LED	GRN_BLNK	SLP_S5	GRN_LED
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	Hi-Z	1	1	Hi-Z

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



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REVISION HISTORY

Rev	Date	Description
_5	20040511	Product data (9397 750 13279). Supersedes data of 2003 Nov 10 (9397 750 12288). Modifications: ● Page 24, Audio-disable table: AUD_EN column (reading vertically) changed from '0000' to '0011'.
_4	20031110	Product data (9397 750 12288); ECN 853-2206 30409 dated 10 October 2003. Supersedes data of 28 March 2003 (9397 750 09602).
_3	20030328	Product data (9397 750 09602); ECN: 853-2206 27930 (2003 Mar 28)

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