

74AVC2T45-Q100

**Dual-bit, dual-supply voltage level translator/transceiver;
3-state**

Rev. 2 — 15 February 2013

Product data sheet

1. General description

The 74AVC2T45-Q100 is a dual-bit, dual-supply transceiver that enables bidirectional level translation. It features two data input-output ports (nA and nB), a direction control input (DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied with any voltage between 0.8 V and 3.6 V. This flexibility makes the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins nA and DIR are referenced to $V_{CC(A)}$ and pins nB are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from nA to nB and a LOW on DIR allows transmission from nB to nA.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In Suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A and B are in the high-impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40°C to $+85^{\circ}\text{C}$ and from -40°C to $+125^{\circ}\text{C}$
- Wide supply voltage range:
 - ◆ $V_{CC(A)}$: 0.8 V to 3.6 V
 - ◆ $V_{CC(B)}$: 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - ◆ JESD8-12 (0.8 V to 1.3 V)
 - ◆ JESD8-11 (0.9 V to 1.65 V)
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - ◆ MIL-STD-883, method 3015 Class 3B exceeds 8000 V
 - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200 \text{ pF}$, $R = 0 \Omega$)



- Maximum data rates:
 - ◆ 500 Mbit/s (1.8 V to 3.3 V translation)
 - ◆ 320 Mbit/s (<1.8 V to 3.3 V translation)
 - ◆ 320 Mbit/s (translate to 2.5 V or 1.8 V)
 - ◆ 280 Mbit/s (translate to 1.5 V)
 - ◆ 240 Mbit/s (translate to 1.2 V)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC2T45DP-Q100	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AVC2T45DC-Q100	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AVC2T45GD-Q100	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74AVC2T45DP-Q100	B45
74AVC2T45DC-Q100	B45
74AVC2T45GD-Q100	B45

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

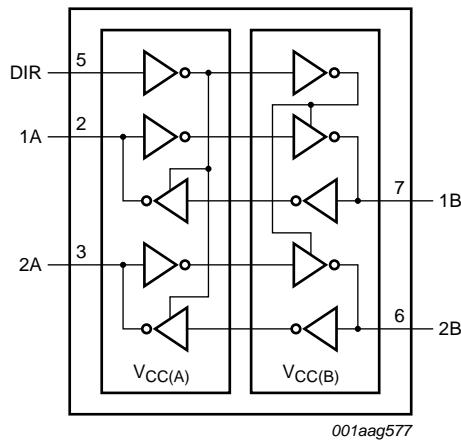


Fig 1. Logic symbol

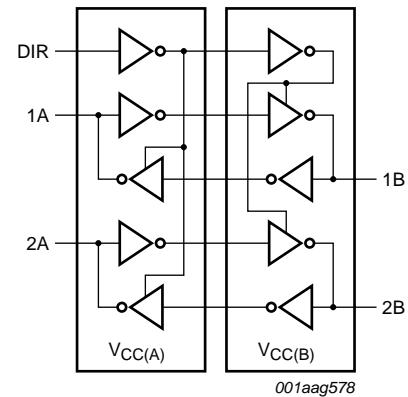


Fig 2. Logic diagram

6. Pinning information

6.1 Pinning

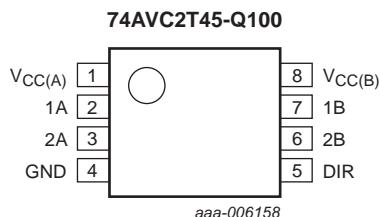


Fig 3. Pin configuration SOT505-2 and SOT765-1

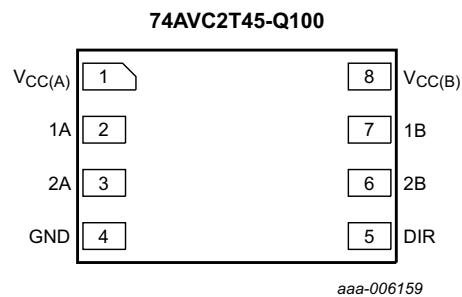


Fig 4. Pin configuration SOT996-2

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A (referenced to pins 1A, 2A and DIR)
1A	2	data input or output
2A	3	data input or output
GND	4	ground (0 V)
DIR	5	direction control
2B	6	data input or output
1B	7	data input or output
$V_{CC(B)}$	8	supply voltage B (referenced to pins 1B and 2B)

7. Functional description

Table 4. Function table^[1]

Supply voltage	Input	Input/output ^[2]	
$V_{CC(A)}, V_{CC(B)}$	DIR ^[3]	nA	nB
0.8 V to 3.6 V	L	$nA = nB$	input
0.8 V to 3.6 V	H	input	$nB = nA$
GND ^[4]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The input circuit of the data I/O is always active.

[3] The DIR input circuit is referenced to $V_{CC(A)}$.

[4] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into Suspend mode.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V	
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V	
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA	
V_I	input voltage		[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA	
V_O	output voltage	Active mode	[1][2][3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	[1]	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CCO}	-	± 50	mA	
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA	
I_{GND}	ground current		-100	-	mA	
T_{stg}	storage temperature		-65	+150	°C	
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[4]	-	250	mW

[1] The minimum input voltage rating and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] $V_{CCO} + 0.5$ V should not exceed 4.6 V.

[4] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly at 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For XSON8 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC(A)}$	supply voltage A		0.8	3.6	V	
$V_{CC(B)}$	supply voltage B		0.8	3.6	V	
V_I	input voltage		0	3.6	V	
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode	0	3.6	V	
T_{amb}	ambient temperature		-40	+125	°C	
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8$ V to 3.6 V	[2]	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

10. Static characteristics

Table 7. Typical static characteristics at $T_{amb} = 25^{\circ}\text{C}$ ^{[1][2]}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} $I_O = -1.5 \text{ mA}$; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.69	-	V	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} $I_O = 1.5 \text{ mA}$; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.07	-	V	
I_I	input leakage current	DIR input; $V_I = 0 \text{ V}$ or 3.6 V ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$ to 3.6 V	-	± 0.025	± 0.25	μA	
I_{OZ}	OFF-state output current	A or B port; $V_O = 0 \text{ V}$ or V_{CCO} ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$ to 3.6 V	^[3]	-	± 0.5	± 2.5	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0 \text{ V}$ to 3.6 V ; $V_{CC(A)} = 0 \text{ V}$; $V_{CC(B)} = 0.8 \text{ V}$ to 3.6 V	-	± 0.1	± 1	μA	
		B port; V_I or $V_O = 0 \text{ V}$ to 3.6 V ; $V_{CC(B)} = 0 \text{ V}$; $V_{CC(A)} = 0.8 \text{ V}$ to 3.6 V	-	± 0.1	± 1	μA	
C_I	input capacitance	DIR input; $V_I = 0 \text{ V}$ or 3.3 V ; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	1.0	-	pF	
$C_{I/O}$	input/output capacitance	A and B port; Suspend mode; $V_O = V_{CCO}$ or GND; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	4.0	-	pF	

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. Static characteristics^{[1][2]}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input					
		$V_{CCI} = 0.8 \text{ V}$	0.70 V_{CCI}	-	0.70 V_{CCI}	-	V
		$V_{CCI} = 1.1 \text{ V}$ to 1.95 V	0.65 V_{CCI}	-	0.65 V_{CCI}	-	V
		$V_{CCI} = 2.3 \text{ V}$ to 2.7 V	1.6	-	1.6	-	V
		$V_{CCI} = 3.0 \text{ V}$ to 3.6 V	2	-	2	-	V
	DIR input						
		$V_{CC(A)} = 0.8 \text{ V}$	0.70 $V_{CC(A)}$	-	0.70 $V_{CC(A)}$	-	V
		$V_{CC(A)} = 1.1 \text{ V}$ to 1.95 V	0.65 $V_{CC(A)}$	-	0.65 $V_{CC(A)}$	-	V
		$V_{CC(A)} = 2.3 \text{ V}$ to 2.7 V	1.6	-	1.6	-	V
		$V_{CC(A)} = 3.0 \text{ V}$ to 3.6 V	2	-	2	-	V

Table 8. Static characteristics ...continued^{[1][2]}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IL}	LOW-level input voltage	data input					
		V _{CCI} = 0.8 V	-	0.30V _{CCI}	-	0.30V _{CCI}	V
		V _{CCI} = 1.1 V to 1.95 V	-	0.35V _{CCI}	-	0.35V _{CCI}	V
		V _{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	0.9	-	0.9	V
		DIR input					
		V _{CC(A)} = 0.8 V	-	0.30V _{CC(A)}	-	0.30V _{CC(A)}	V
		V _{CC(A)} = 1.1 V to 1.95 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = -100 μ A; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	0.85	-	0.85	-	V
		I _O = -6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	1.05	-	1.05	-	V
		I _O = -8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	1.2	-	1.2	-	V
		I _O = -9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	1.75	-	1.75	-	V
		I _O = -12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	2.3	-	2.3	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100 μ A; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I _O = 3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	-	0.25	-	0.25	V
		I _O = 6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	-	0.35	-	0.35	V
		I _O = 8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	-	0.45	-	0.45	V
		I _O = 9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	-	0.55	-	0.55	V
		I _O = 12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	-	0.7	-	0.7	V
I _I	input leakage current	DIR input; V _I = 0 V or 3.6 V; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	\pm 1	-	\pm 1.5	μ A
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 3.6 V	[3]	-	\pm 5	-	\pm 7.5 μ A
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 3.6 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.8 V to 3.6 V	-	\pm 5	-	\pm 35	μ A
		B port; V _I or V _O = 0 V to 3.6 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0.8 V to 3.6 V	-	\pm 5	-	\pm 35	μ A

Table 8. Static characteristics ...continued^{[1][2]}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{CC}	supply current	A port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	8	-	11.5	µA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	8	-	11.5	µA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-2	-	-8	-	µA
		B port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	8	-	11.5	µA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-2	-	-8	-	µA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-	8	-	11.5	µA
		A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI} ; V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	16	-	23	µA

[1] V_{CCO} is the supply voltage associated with the output port.[2] V_{CCI} is the supply voltage associated with the data input port.[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

11. Dynamic characteristics

Table 9. Typical dynamic characteristics at $V_{CC(A)} = 0.8$ V and $T_{amb} = 25$ °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	A to B	15.5	8.1	7.6	7.7	8.4	9.2	ns
		B to A	15.5	12.7	12.3	12.2	12.0	11.8	ns
t_{dis}	disable time	DIR to A	12.2	12.2	12.2	12.2	12.2	12.2	ns
		DIR to B	11.7	7.9	7.6	8.2	8.7	10.2	ns
t_{en}	enable time	DIR to A	27.2	20.6	19.9	20.4	20.7	22.0	ns
		DIR to B	27.7	20.3	19.8	19.9	20.6	21.4	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{en} is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

Table 10. Typical dynamic characteristics at $V_{CC(B)} = 0.8$ V and $T_{amb} = 25$ °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	A to B	15.5	12.7	12.3	12.2	12.0	11.8	ns
		B to A	15.5	8.1	7.6	7.7	8.4	9.2	ns
t_{dis}	disable time	DIR to A	12.2	4.9	3.8	3.7	2.8	3.4	ns
		DIR to B	11.7	9.2	9.0	8.8	8.7	8.6	ns
t_{en}	enable time	DIR to A	27.2	17.3	16.6	16.5	17.1	17.8	ns
		DIR to B	27.7	17.6	16.1	15.9	14.8	15.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{en} is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

Table 11. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25$ °C [1][2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction A to B); B port: (direction B to A)	1	2	2	2	2	2	pF
		A port: (direction B to A); B port: (direction A to B)	9	11	11	12	14	17	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 10$ MHz; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1$ ns; $C_L = 0$ pF; $R_L = \infty$ Ω .

Table 12. Dynamic characteristics for temperature range -40°C to $+85^{\circ}\text{C}$ [1]Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V _{CC(B)}										Unit	
			1.2 V \pm 0.1 V		1.5 V \pm 0.1 V		1.8 V \pm 0.15 V		2.5 V \pm 0.2 V		3.3 V \pm 0.3 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
V_{CC(A)} = 1.1 V to 1.3 V														
t _{pd}	propagation delay	A to B	1.0	9.0	0.7	6.8	0.6	6.1	0.5	5.7	0.5	6.1	ns	
		B to A	1.0	9.0	0.8	8.0	0.7	7.7	0.6	7.2	0.5	7.1	ns	
t _{dis}	disable time	DIR to A	2.2	8.8	2.2	8.8	2.2	8.8	2.2	8.8	2.2	8.8	ns	
		DIR to B	2.2	8.4	1.8	6.7	2.0	6.9	1.7	6.2	2.4	7.2	ns	
t _{en}	enable time	DIR to A	-	17.4	-	14.7	-	14.6	-	13.4	-	14.3	ns	
		DIR to B	-	17.8	-	15.6	-	14.9	-	14.5	-	14.9	ns	
V_{CC(A)} = 1.4 V to 1.6 V														
t _{pd}	propagation delay	A to B	1.0	8.0	0.7	5.4	0.6	4.6	0.5	3.7	0.5	3.5	ns	
		B to A	1.0	6.8	0.8	5.4	0.7	5.1	0.6	4.7	0.5	4.5	ns	
t _{dis}	disable time	DIR to A	1.6	6.3	1.6	6.3	1.6	6.3	1.6	6.3	1.6	6.3	ns	
		DIR to B	2.0	7.6	1.8	5.9	1.6	6.0	1.2	4.8	1.7	5.5	ns	
t _{en}	enable time	DIR to A	-	14.4	-	11.3	-	11.1	-	9.5	-	10.0	ns	
		DIR to B	-	14.3	-	11.7	-	10.9	-	10.0	-	9.8	ns	
V_{CC(A)} = 1.65 V to 1.95 V														
t _{pd}	propagation delay	A to B	1.0	7.7	0.6	5.1	0.5	4.3	0.5	3.4	0.5	3.1	ns	
		B to A	1.0	6.1	0.7	4.6	0.5	4.4	0.5	3.9	0.5	3.7	ns	
t _{dis}	disable time	DIR to A	1.6	5.5	1.6	5.5	1.6	5.5	1.6	5.5	1.6	5.5	ns	
		DIR to B	1.8	7.7	1.8	5.7	1.4	5.8	1.0	4.5	1.5	5.2	ns	
t _{en}	enable time	DIR to A	-	13.8	-	10.3	-	10.2	-	8.4	-	8.9	ns	
		DIR to B	-	13.2	-	10.6	-	9.8	-	8.9	-	8.6	ns	
V_{CC(A)} = 2.3 V to 2.7 V														
t _{pd}	propagation delay	A to B	1.0	7.2	0.5	4.7	0.5	3.9	0.5	3.0	0.5	2.6	ns	
		B to A	1.0	5.7	0.6	3.8	0.5	3.4	0.5	3.0	0.5	2.8	ns	
t _{dis}	disable time	DIR to A	1.5	4.2	1.5	4.2	1.5	4.2	1.5	4.2	1.5	4.2	ns	
		DIR to B	1.7	7.3	2.0	5.2	1.5	5.1	0.6	4.2	1.1	4.8	ns	
t _{en}	enable time	DIR to A	-	13.0	-	9.0	-	8.5	-	7.2	-	7.6	ns	
		DIR to B	-	11.4	-	8.9	-	8.1	-	7.2	-	6.8	ns	
V_{CC(A)} = 3.0 V to 3.6 V														
t _{pd}	propagation delay	A to B	1.0	7.1	0.5	4.5	0.5	3.7	0.5	2.8	0.5	2.4	ns	
		B to A	1.0	6.1	0.6	3.6	0.5	3.1	0.5	2.6	0.5	2.4	ns	
t _{dis}	disable time	DIR to A	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	ns	
		DIR to B	1.7	7.2	0.7	5.5	0.6	5.5	0.7	4.1	1.7	4.7	ns	
t _{en}	enable time	DIR to A	-	13.3	-	9.1	-	8.6	-	6.7	-	7.1	ns	
		DIR to B	-	11.8	-	9.2	-	8.4	-	7.5	-	7.1	ns	

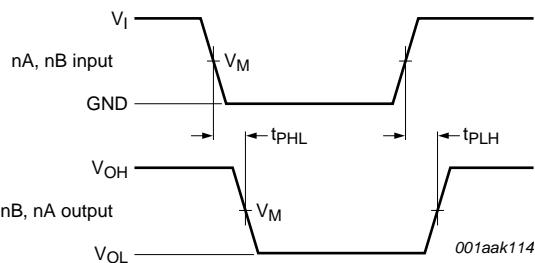
[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.
t_{en} is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

Table 13. Dynamic characteristics for temperature range -40°C to $+125^{\circ}\text{C}$ [1]Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	V _{CC(B)}										Unit	
			1.2 V \pm 0.1 V		1.5 V \pm 0.1 V		1.8 V \pm 0.15 V		2.5 V \pm 0.2 V		3.3 V \pm 0.3 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
V_{CC(A)} = 1.1 V to 1.3 V														
t _{pd}	propagation delay	A to B	1.0	9.9	0.7	7.5	0.6	6.8	0.5	6.3	0.5	6.8	ns	
		B to A	1.0	9.9	0.8	8.8	0.7	8.5	0.6	8.0	0.5	7.9	ns	
t _{dis}	disable time	DIR to A	2.2	9.7	2.2	9.7	2.2	9.7	2.2	9.7	2.2	9.7	ns	
		DIR to B	2.2	9.2	1.8	7.4	2.0	7.6	1.7	6.9	2.4	8.0	ns	
t _{en}	enable time	DIR to A	-	19.1	-	16.2	-	16.1	-	14.9	-	15.9	ns	
		DIR to B	-	19.6	-	17.2	-	16.5	-	16.0	-	16.5	ns	
V_{CC(A)} = 1.4 V to 1.6 V														
t _{pd}	propagation delay	A to B	1.0	8.8	0.7	6.0	0.6	5.1	0.5	4.1	0.5	3.9	ns	
		B to A	1.0	7.5	0.8	6.0	0.7	5.7	0.6	5.2	0.5	5.0	ns	
t _{dis}	disable time	DIR to A	1.6	7.0	1.6	7.0	1.6	7.0	1.6	7.0	1.6	7.0	ns	
		DIR to B	2.0	8.3	1.8	6.5	1.6	6.6	1.2	5.3	1.7	6.1	ns	
t _{en}	enable time	DIR to A	-	15.8	-	12.5	-	12.3	-	10.5	-	11.1	ns	
		DIR to B	-	15.8	-	13.0	-	12.1	-	11.1	-	10.9	ns	
V_{CC(A)} = 1.65 V to 1.95 V														
t _{pd}	propagation delay	A to B	1.0	8.5	0.6	5.7	0.5	4.8	0.5	3.8	0.5	3.5	ns	
		B to A	1.0	6.8	0.7	5.1	0.5	4.9	0.5	4.3	0.5	4.1	ns	
t _{dis}	disable time	DIR to A	1.6	6.1	1.6	6.1	1.6	6.1	1.6	6.1	1.6	6.1	ns	
		DIR to B	1.8	8.5	1.8	6.3	1.4	6.4	1.0	5.0	1.5	5.8	ns	
t _{en}	enable time	DIR to A	-	15.3	-	11.4	-	11.3	-	9.3	-	9.9	ns	
		DIR to B	-	14.6	-	11.8	-	10.9	-	9.9	-	9.6	ns	
V_{CC(A)} = 2.3 V to 2.7 V														
t _{pd}	propagation delay	A to B	1.0	8.0	0.5	5.2	0.5	4.3	0.5	3.3	0.5	2.9	ns	
		B to A	1.0	6.3	0.6	4.2	0.5	3.8	0.5	3.3	0.5	3.1	ns	
t _{dis}	disable time	DIR to A	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	ns	
		DIR to B	1.7	8.0	2.0	5.8	1.5	5.7	0.6	4.7	1.1	5.3	ns	
t _{en}	enable time	DIR to A	-	14.3	-	10.0	-	9.5	-	8.0	-	8.4	ns	
		DIR to B	-	12.7	-	9.9	-	9.0	-	8.0	-	7.6	ns	
V_{CC(A)} = 3.0 V to 3.6 V														
t _{pd}	propagation delay	A to B	1.0	7.9	0.5	5.0	0.5	4.1	0.5	3.1	0.5	2.7	ns	
		B to A	1.0	6.8	0.6	4.0	0.5	3.5	0.5	2.9	0.5	2.7	ns	
t _{dis}	disable time	DIR to A	1.5	5.2	1.5	5.2	1.5	5.2	1.5	5.2	1.5	5.2	ns	
		DIR to B	1.7	7.9	0.7	6.1	0.6	6.1	0.7	4.6	1.7	5.2	ns	
t _{en}	enable time	DIR to A	-	14.7	-	10.1	-	9.6	-	7.5	-	7.9	ns	
		DIR to B	-	13.1	-	10.2	-	9.3	-	8.3	-	7.9	ns	

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.
t_{en} is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

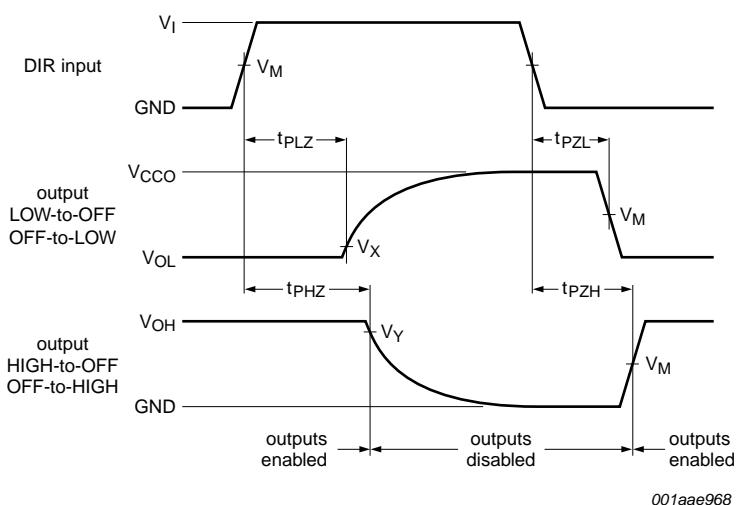
12. Waveforms



Measurement points are given in [Table 14](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. The data input (nA, nB) to output (nB, nA) propagation delay times



Measurement points are given in [Table 14](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

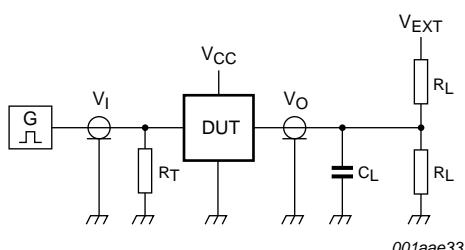
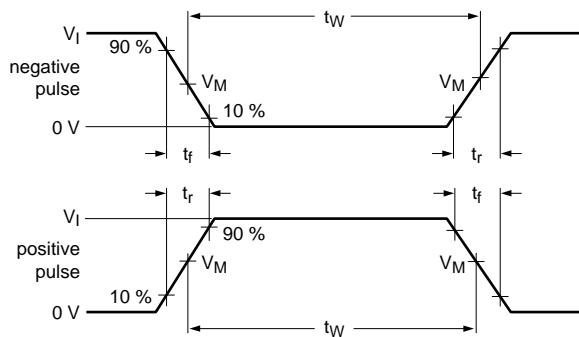
Fig 6. Enable and disable times

Table 14. Measurement points

Supply voltage	Input ^[1]	Output ^[2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.1 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1$ V	$V_{OH} - 0.1$ V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.



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Test data is given in [Table 15](#). R_L = Load resistance. C_L = Load capacitance including jig and probe capacitance. R_T = Termination resistance. V_{EXT} = External voltage for measuring switching times.**Fig 7. Test circuit for measuring switching times****Table 15. Test data**

Supply voltage	Input	Load		V _{EXT}			
V _{CC(A)} , V _{CC(B)}	V _I ^[1]	$\Delta t/\Delta V$ ^[2]	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	
1.1 V to 1.6 V	V _{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	2V _{CC0}
1.65 V to 2.7 V	V _{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	2V _{CC0}
3.0 V to 3.6 V	V _{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	2V _{CC0}

[1] V_{CCI} is the supply voltage associated with the data input port.[2] $dV/dt \geq 1.0 \text{ V/ns}$ [3] V_{CC0} is the supply voltage associated with the output port.

13. Application information

13.1 Unidirectional logic level-shifting application

The circuit given in [Figure 8](#) is an example of the 74AVC2T45-Q100 being used in a unidirectional logic level-shifting application.

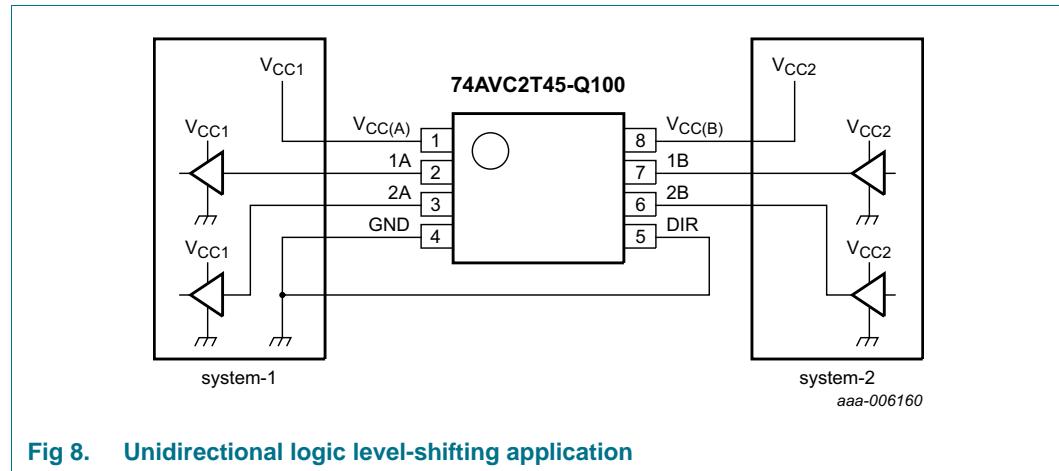


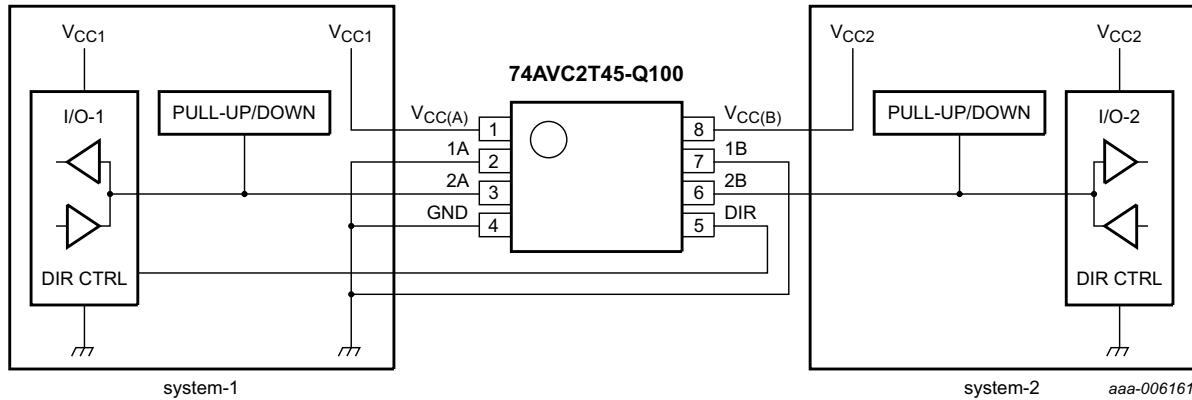
Fig 8. Unidirectional logic level-shifting application

Table 16. Unidirectional logic level-shifting application

Pin	Name	Function	Description
1	V _{CC(A)}	V _{CC1}	supply voltage of system-1 (0.8 V to 3.6 V)
2	1A	OUT1	output level depends on V _{CC1} voltage
3	2A	OUT2	output level depends on V _{CC1} voltage
4	GND	GND	device GND
5	DIR	DIR	the GND (LOW level) determines B port to A port direction
6	2B	IN2	input threshold value depends on V _{CC2} voltage
7	1B	IN1	input threshold value depends on V _{CC2} voltage
8	V _{CC(B)}	V _{CC2}	supply voltage of system-2 (0.8 V to 3.6 V)

13.2 Bidirectional logic level-shifting application

Figure 9 shows the 74AVC2T45-Q100 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable (OE) pin, the system designer must take precautions to avoid bus contention between system-1 and system-2 when changing directions.



System-1 and system-2 must use the same conditions, i.e., both pull-up or both pull-down.

Fig 9. Bidirectional logic level-shifting application

Table 17 gives a sequence that illustrates data transmission from system-1 to system-2 and then from system-2 to system-1.

Table 17. Bidirectional logic level-shifting application^{[1][2]}

State	DIR CTRL	I/O-1	I/O-2	Description
1	H	output	input	system-1 data to system-2
2	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on the pull-up or pull-down.
3	L	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 are still disabled. The bus-line state depends on the pull-up or pull-down.
4	L	input	output	system-2 data to system-1

[1] System-1 and system-2 must use the same conditions, i.e., both pull-up or both pull-down.

[2] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

13.3 Power-up considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

Table 18. Typical total supply current ($I_{CC(A)} + I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.7	2.3	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.3	1.4	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.9	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.5	μA
2.5 V	0.1	0.7	0.3	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	2.3	1.4	0.9	0.5	0.1	0.1	μA

13.4 Enable times

The enable times for the 74AVC2T45-Q100 are calculated from the following formulas:

- t_{en} (DIR to nA) = t_{dis} (DIR to nB) + t_{pd} (nB to nA)
- t_{en} (DIR to nB) = t_{dis} (DIR to nA) + t_{pd} (nA to nB)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, the 74AVC2T45-Q100 is initially transmitting from A to B, then the DIR bit is switched. Disable the B port of the device before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

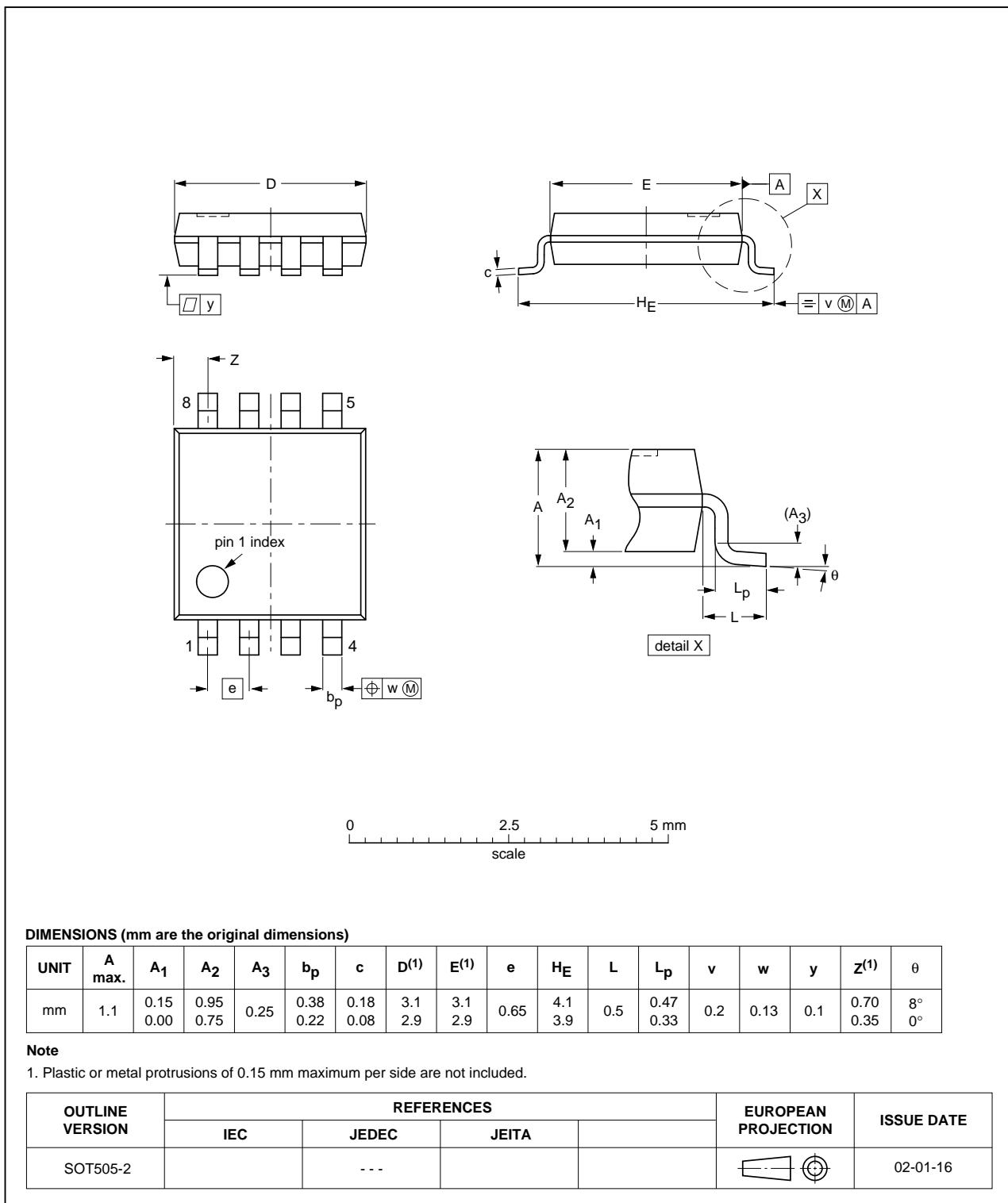


Fig 10. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

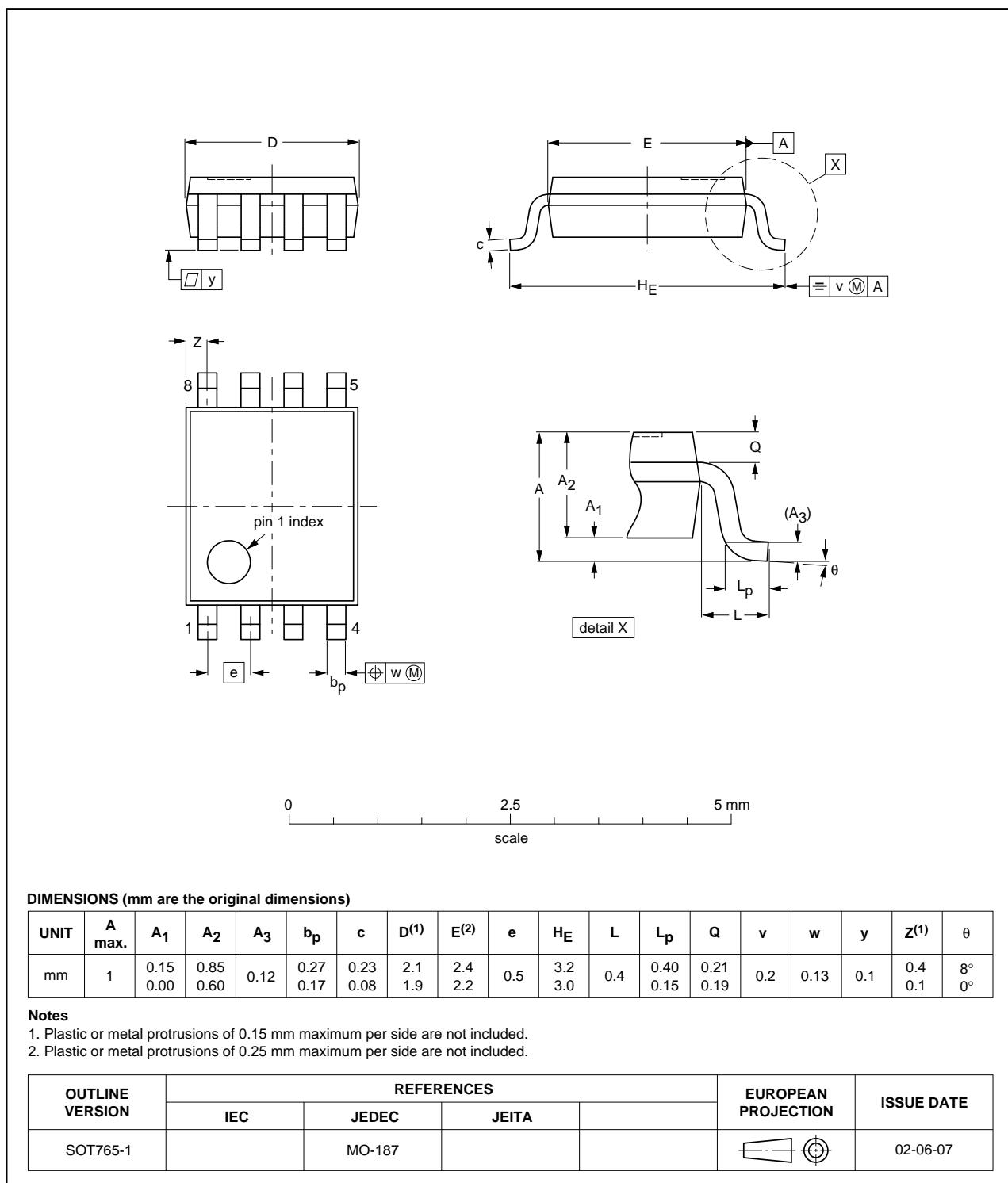


Fig 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

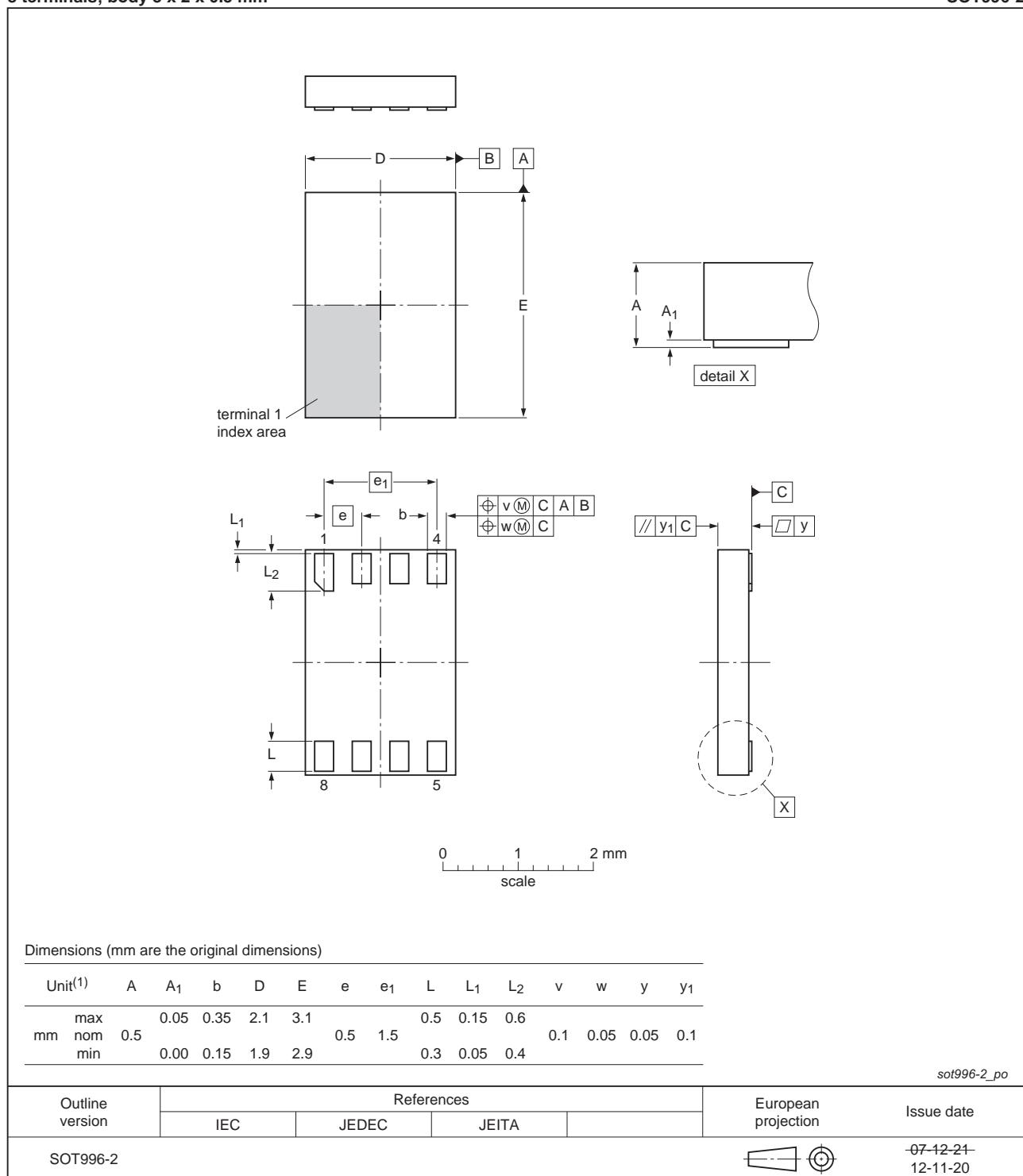


Fig 12. Package outline SOT996-2 (XSON8)

15. Abbreviations

Table 19. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

16. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC2T45_Q100 v.2	20130215	Product data sheet	-	74AVC2T45_Q100 v.1
Modifications:	• For type number 74AVC2T45GD-Q100 XSON8U has changed to XSON8.			
74AVC2T45_Q100 v.1	20130131	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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