

MC74HC4051A, MC74HC4052A, MC74HC4053A

Analog Multiplexers / Demultiplexers High-Performance Silicon-Gate CMOS

The MC74HC4051A, MC74HC4052A and MC74HC4053A utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051A, HC4052A and HC4053A are identical in pinout to the metal-gate MC14051AB, MC14052AB and MC14053AB. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{ON}) is more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

For a multiplexer/demultiplexer with injection current protection, see HC4851A and HC4852A.

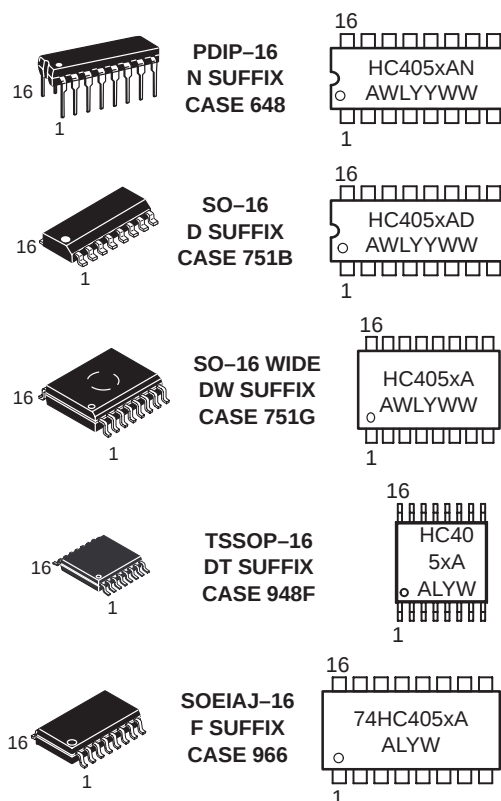
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051A — 184 FETs or 46 Equivalent Gates
HC4052A — 168 FETs or 42 Equivalent Gates
HC4053A — 156 FETs or 39 Equivalent Gates



ON Semiconductor

<http://onsemi.com>

MARKING DIAGRAMS



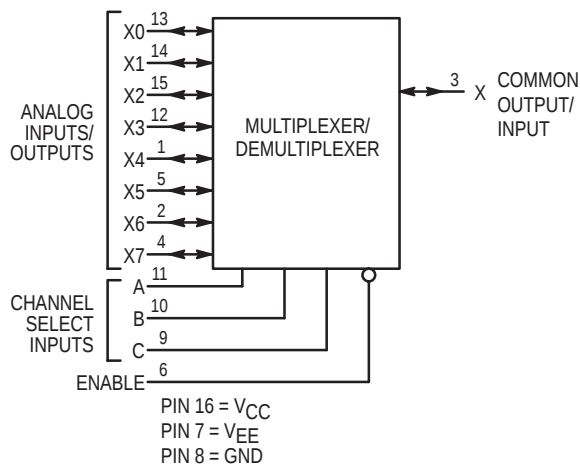
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

MC74HC4051A, MC74HC4052A, MC74HC4053A

LOGIC DIAGRAM
MC74HC4051A
Single-Pole, 8-Position Plus Common Off

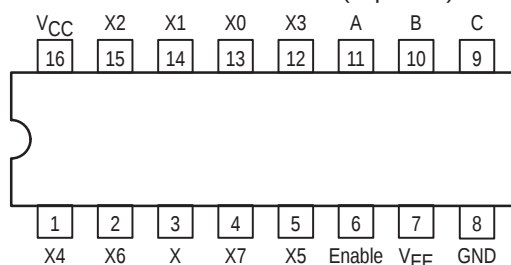


FUNCTION TABLE – MC74HC4051A

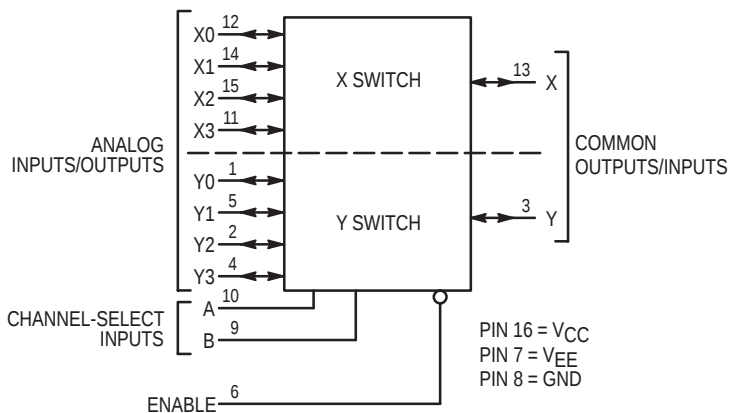
Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

Pinout: MC74HC4051A (Top View)



LOGIC DIAGRAM
MC74HC4052A
Double-Pole, 4-Position Plus Common Off

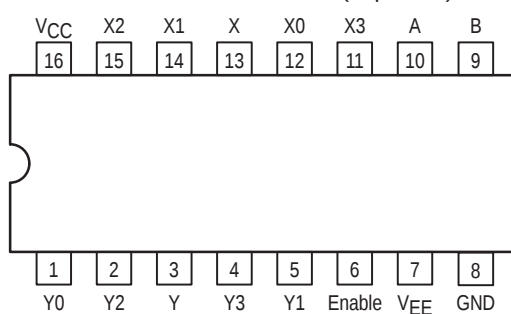


FUNCTION TABLE – MC74HC4052A

Control Inputs				
Enable	Select			
	B	A	ON Channels	
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

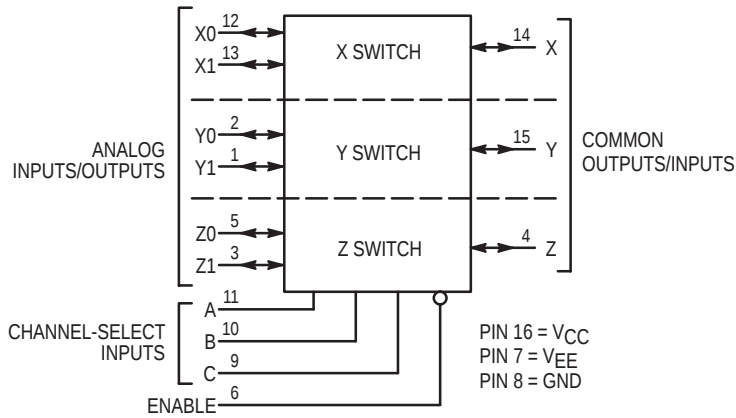
Pinout: MC74HC4052A (Top View)



MC74HC4051A, MC74HC4052A, MC74HC4053A

LOGIC DIAGRAM MC74HC4053A

Triple Single-Pole, Double-Position Plus Common Off



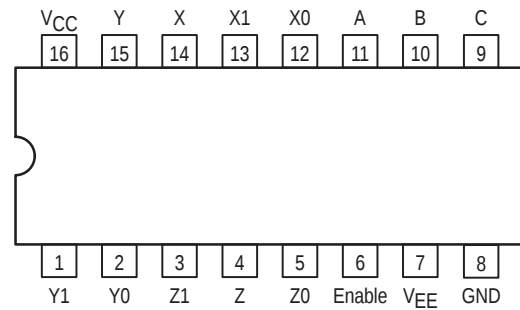
NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

FUNCTION TABLE – MC74HC4053A

Control Inputs				ON Channels		
Enable	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

Pinout: MC74HC4053A (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{IS}	Analog Input Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C

EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C

TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74HC4051A, MC74HC4052A, MC74HC4053A

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V _{EE})	2.0 2.0	6.0 12.0	V
V _{EE}	Negative DC Supply Voltage, Output (Referenced to GND)	− 6.0	GND	V
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V
V _{in}	Digital Input Voltage (Referenced to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch		1.2	V
T _A	Operating Temperature Range, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise/Fall Time (Channel Select or Enable Inputs) V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = \text{GND}$, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{ON} = \text{Per Spec}$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{ON} = \text{Per Spec}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0\text{ V}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{EE} = \text{GND}$ $V_{IO} = 0\text{ V}$ $V_{EE} = -6.0$	6.0 6.0	1 4	10 40	20 80	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

MC74HC4051A, MC74HC4052A, MC74HC4053A

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V _{CC}	V _{EE}	Guaranteed Limit			Unit
					–55 to 25°C	≤85°C	≤125°C	
R _{ON}	Maximum “ON” Resistance	V _{IN} = V _{IL} or V _{IH} ; V _{IS} = V _{CC} to V _{EE} ; I _S ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	190	240	280	Ω
			4.5	– 4.5	120	150	170	
			6.0	– 6.0	100	125	140	
		V _{IN} = V _{IL} or V _{IH} ; V _{IS} = V _{CC} or V _{EE} (Endpoints); I _S ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	150	190	230	
			4.5	– 4.5	100	125	140	
			6.0	– 6.0	80	100	115	
ΔR _{ON}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V _{IN} = V _{IL} or V _{IH} ; V _{IS} = 1/2 (V _{CC} – V _{EE}); I _S ≤ 2.0 mA	4.5	0.0	30	35	40	Ω
			4.5	– 4.5	12	15	18	
			6.0	– 6.0	10	12	14	
I _{off}	Maximum Off–Channel Leakage Current, Any One Channel	V _{IN} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} – V _{EE} ; Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
			6.0	– 6.0	0.2	2.0	4.0	
			6.0	– 6.0	0.1	1.0	2.0	
I _{on}	Maximum On–Channel HC4051A Leakage Current, HC4052A Common Channel HC4053A	V _{IN} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} – V _{EE} ; Switch Off (Figure 4)	6.0	– 6.0	0.2	2.0	4.0	μA
			6.0	– 6.0	0.1	1.0	2.0	
			6.0	– 6.0	0.1	1.0	2.0	
	Maximum On–Channel HC4051A Leakage Current, HC4052A Channel–to–Channel HC4053A	V _{IN} = V _{IL} or V _{IH} ; Switch–to–Switch = V _{CC} – V _{EE} ; (Figure 5)	6.0	– 6.0	0.2	2.0	4.0	μA
			6.0	– 6.0	0.1	1.0	2.0	
			6.0	– 6.0	0.1	1.0	2.0	

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0	270	320	350	ns
		3.0	90	110	125	
		4.5	59	79	85	
		6.0	45	65	75	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	40	60	70	ns
		3.0	25	30	32	
		4.5	12	15	18	
		6.0	10	13	15	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	160	200	220	ns
		3.0	70	95	110	
		4.5	48	63	76	
		6.0	39	55	63	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	245	315	345	ns
		3.0	115	145	155	
		4.5	49	69	83	
		6.0	39	58	67	
C _{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
C _{I/O}	Maximum Capacitance (All Switches Off)	Analog I/O	35	35	35	pF
		Common O/I: HC4051A	130	130	130	
		HC4052A	80	80	80	
		HC4053A	50	50	50	
	Feedthrough		1.0	1.0	1.0	

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D)

C _{PD}	Power Dissipation Capacitance (Figure 13)*	HC4051A HC4052A HC4053A	Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V	pF
			45 80 45	

* Used to determine the no–load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

MC74HC4051A, MC74HC4052A, MC74HC4053A

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V _{CC} V	V _{EE} V	Limit*			Unit
					25°C			
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f _{in} = 1MHz Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{OS} ; Increase f _{in} Frequency Until dB Meter Reads –3dB; R _L = 50Ω, C _L = 10pF			'51	'52	'53	MHz
			2.25	–2.25	80	95	120	
			4.50	–4.50	80	95	120	
			6.00	–6.00	80	95	120	
—	Off–Channel Feedthrough Isolation (Figure 7)	f _{in} = Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{IS} f _{in} = 10kHz, R _L = 600Ω, C _L = 50pF	2.25	–2.25	–50			dB
			4.50	–4.50	–50			
			6.00	–6.00	–50			
		f _{in} = 1.0MHz, R _L = 50Ω, C _L = 10pF	2.25	–2.25	–40			
			4.50	–4.50	–40			
			6.00	–6.00	–40			
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V _{in} ≤ 1MHz Square Wave (t _r = t _f = 6ns); Adjust R _L at Setup so that I _S = 0A; Enable = GND R _L = 600Ω, C _L = 50pF	2.25	–2.25	25			mV _{pp}
			4.50	–4.50	105			
			6.00	–6.00	135			
		R _L = 10kΩ, C _L = 10pF	2.25	–2.25	35			
			4.50	–4.50	145			
			6.00	–6.00	190			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A)	f _{in} = Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{IS} f _{in} = 10kHz, R _L = 600Ω, C _L = 50pF	2.25	–2.25	–50			dB
			4.50	–4.50	–50			
			6.00	–6.00	–50			
		f _{in} = 1.0MHz, R _L = 50Ω, C _L = 10pF	2.25	–2.25	–60			
			4.50	–4.50	–60			
			6.00	–6.00	–60			
THD	Total Harmonic Distortion (Figure 14)	f _{in} = 1kHz, R _L = 10kΩ, C _L = 50pF THD = THD _{measured} – THD _{source} V _{IS} = 4.0V _{pp} sine wave V _{IS} = 8.0V _{pp} sine wave V _{IS} = 11.0V _{pp} sine wave						%
			2.25	–2.25	0.10			
			4.50	–4.50	0.08			
			6.00	–6.00	0.05			

*Limits not tested. Determined by design and verified by qualification.

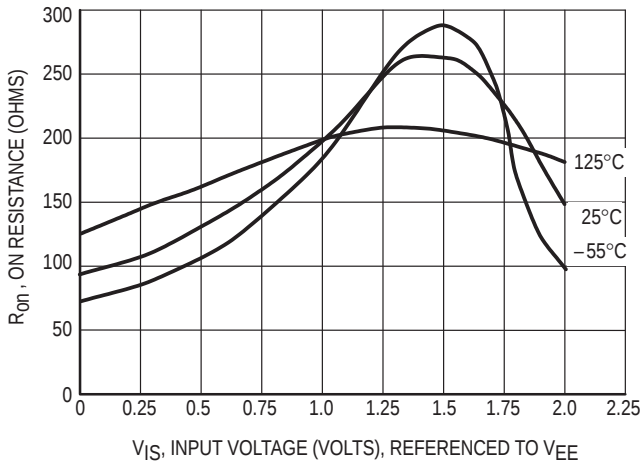


Figure 1a. Typical On Resistance, V_{CC} - V_{EE} = 2.0 V

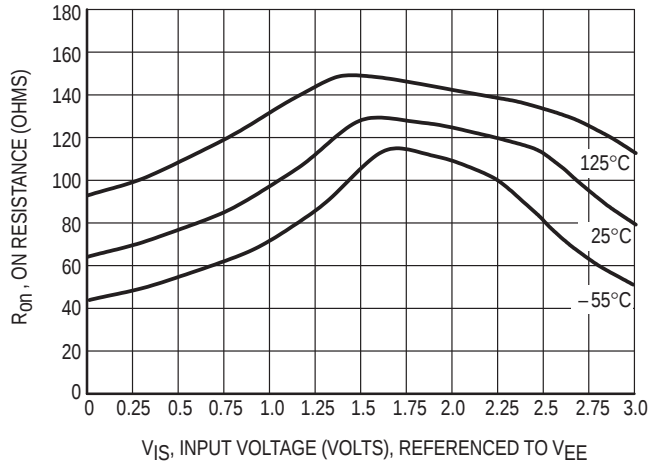


Figure 1b. Typical On Resistance, V_{CC} - V_{EE} = 3.0 V

MC74HC4051A, MC74HC4052A, MC74HC4053A

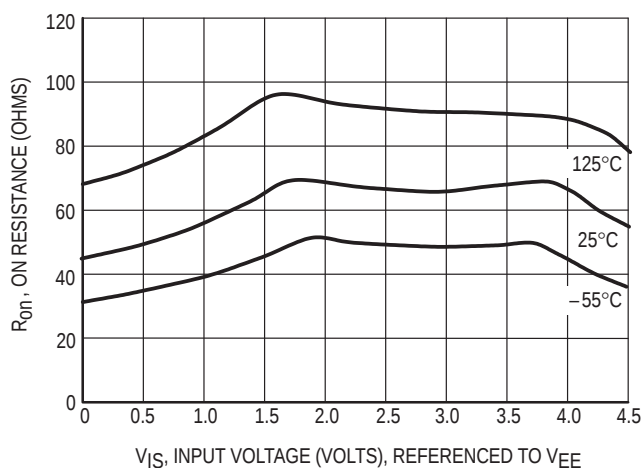


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V

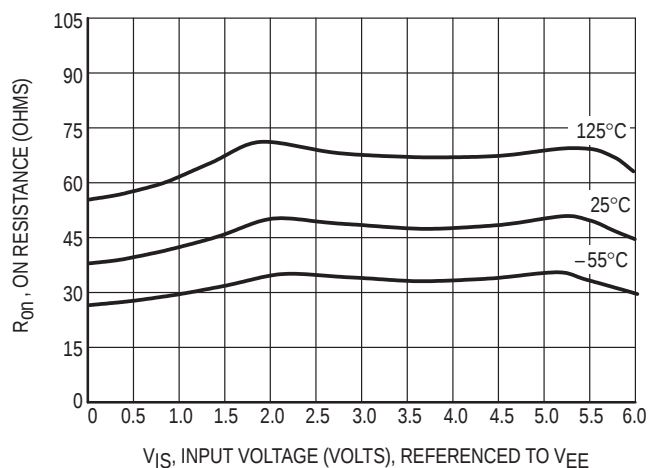


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V

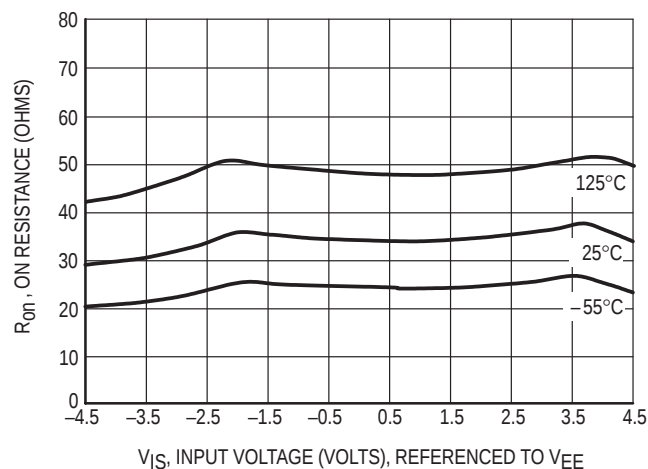


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V

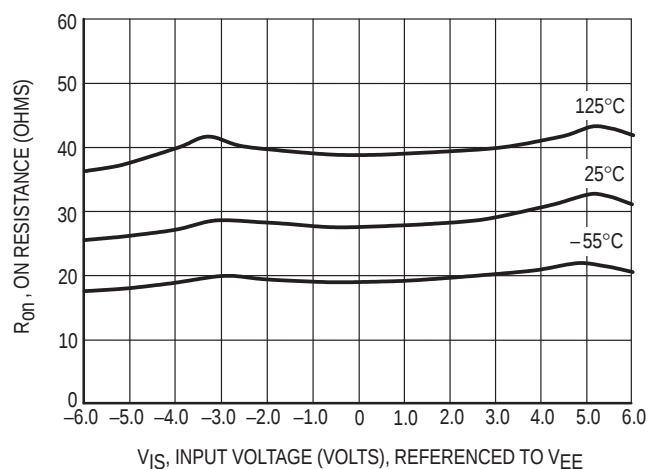


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE} = 12.0$ V

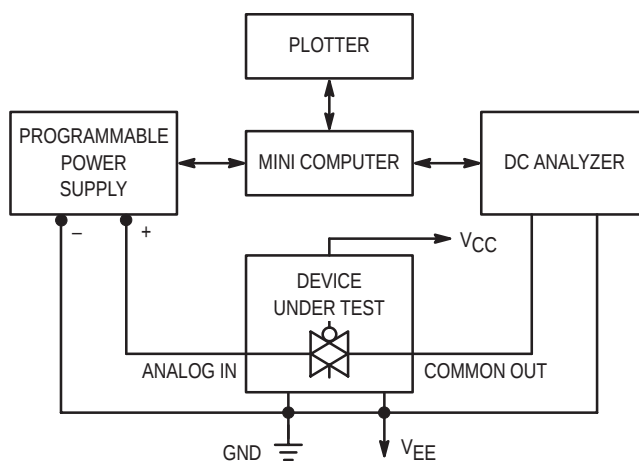


Figure 2. On Resistance Test Set-Up

MC74HC4051A, MC74HC4052A, MC74HC4053A

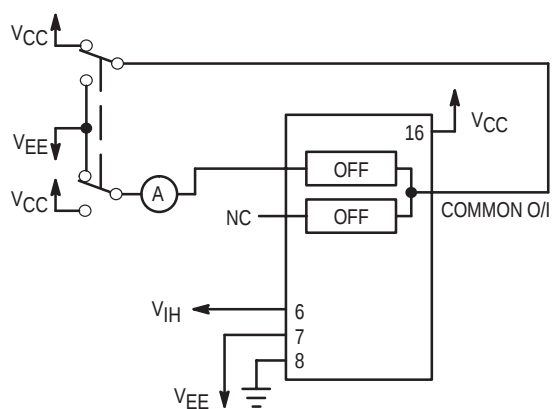


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

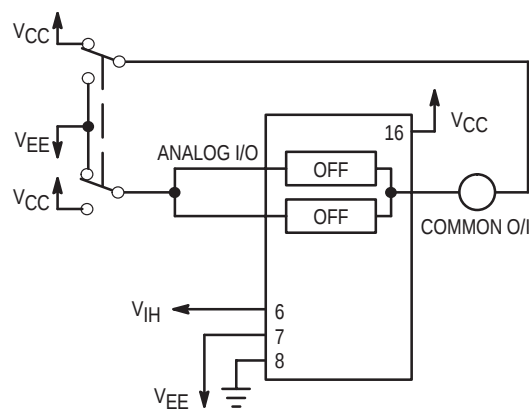


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

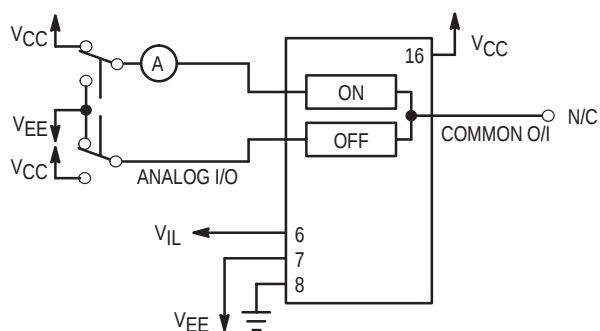
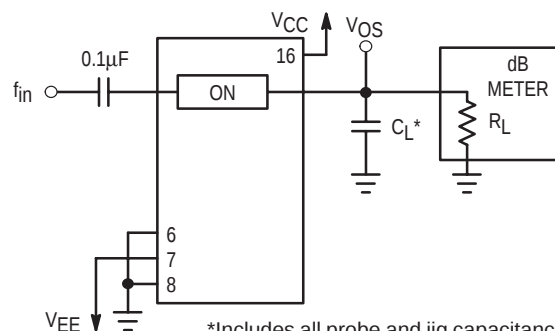
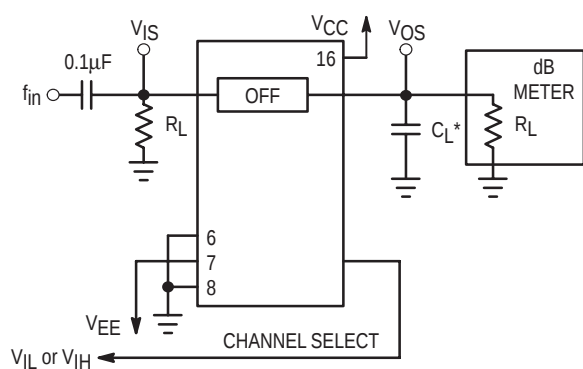


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



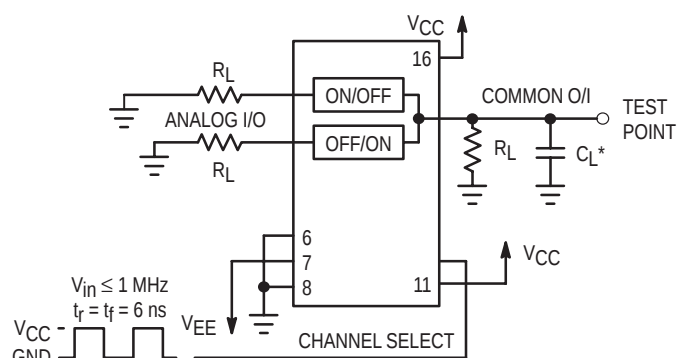
*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set-Up



*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

MC74HC4051A, MC74HC4052A, MC74HC4053A

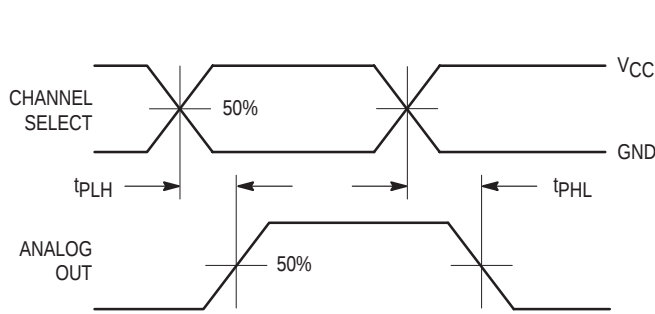
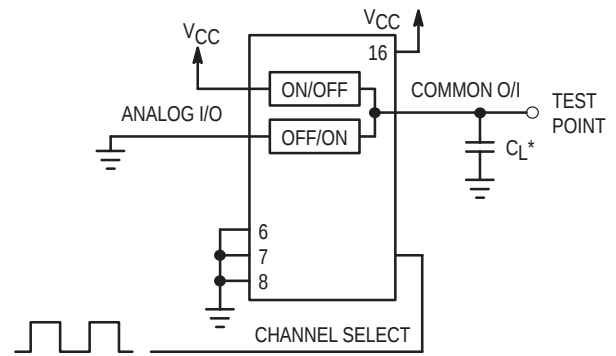


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

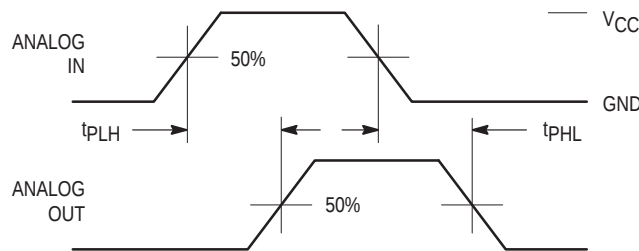
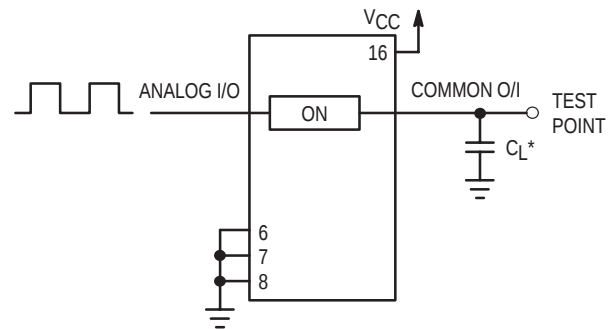


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

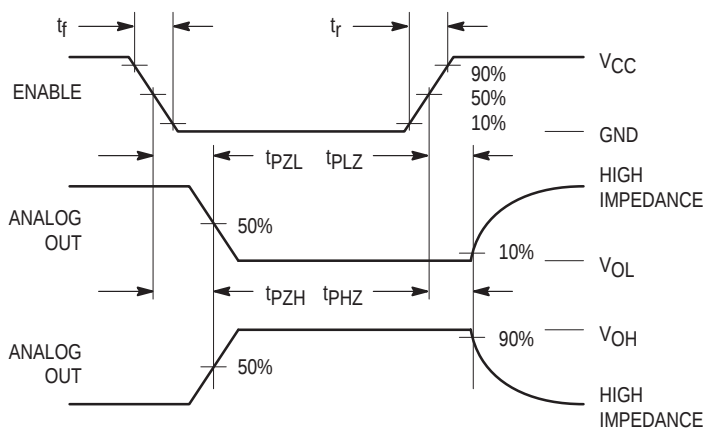


Figure 11a. Propagation Delays, Enable to Analog Out

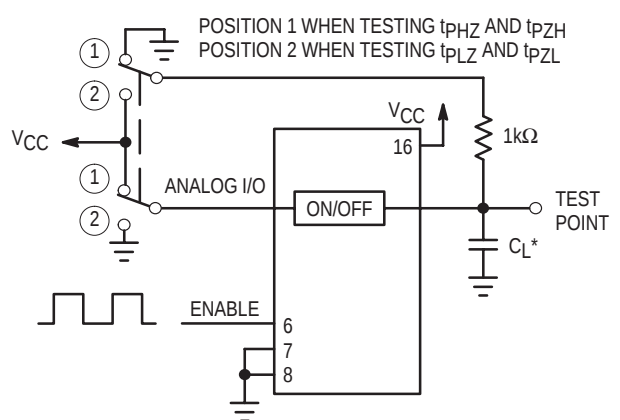
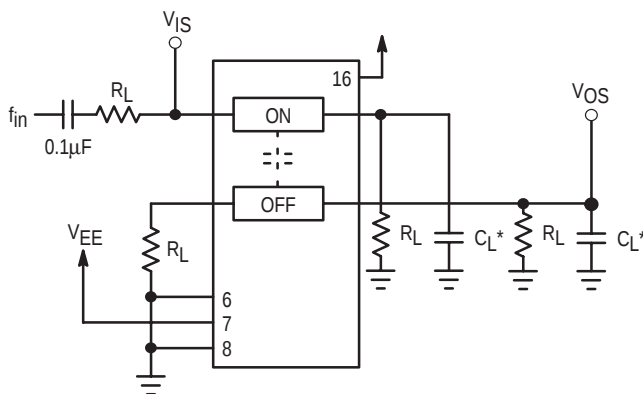


Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out



*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

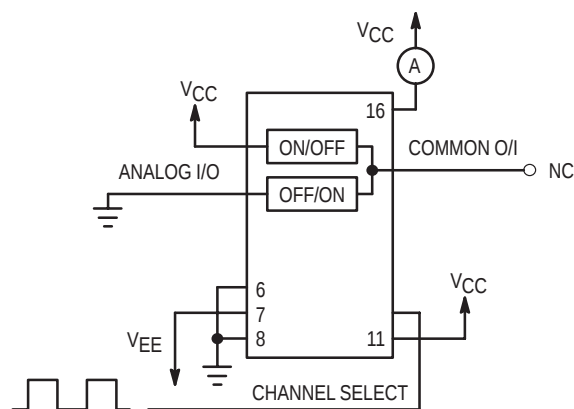
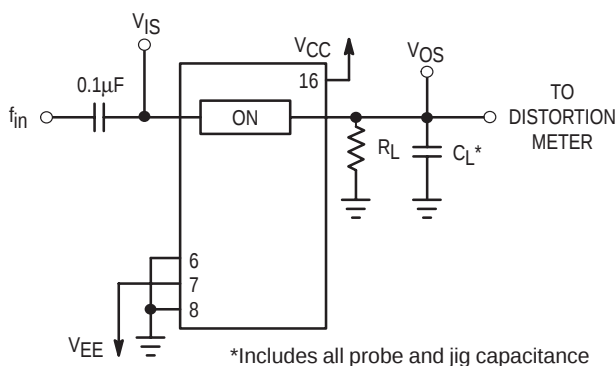


Figure 13. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance

Figure 14a. Total Harmonic Distortion, Test Set-Up

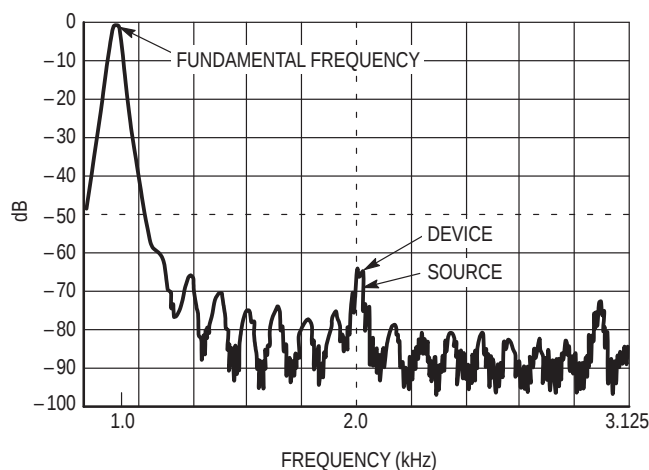


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5V = \text{logic high} \\ \text{GND} &= 0V = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ &\text{and } V_{EE} \leq \text{GND} \end{aligned}$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

MC74HC4051A, MC74HC4052A, MC74HC4053A

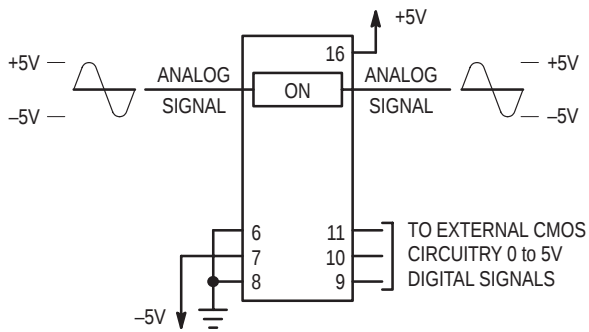


Figure 15. Application Example

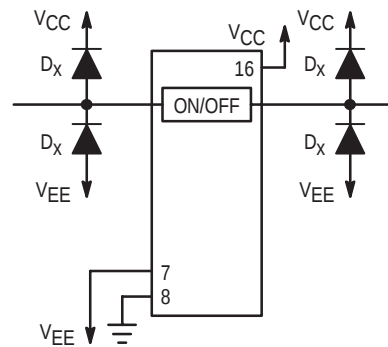
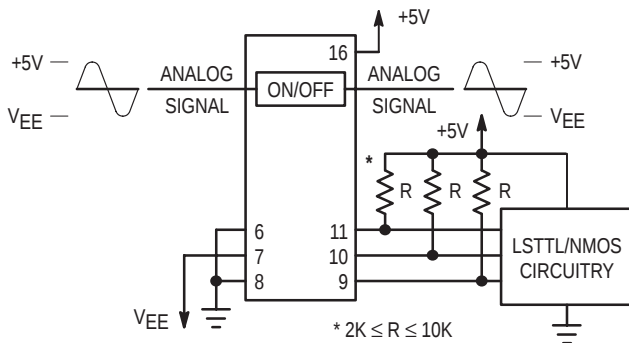
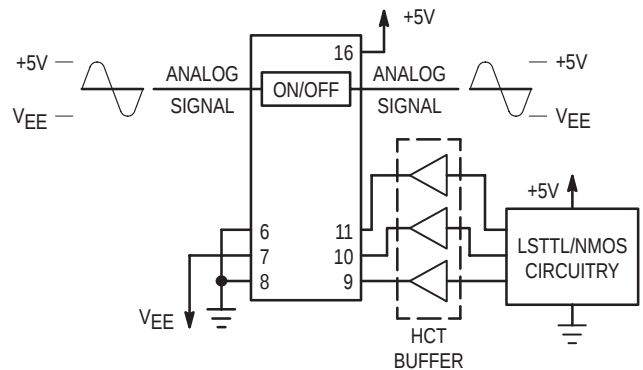


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

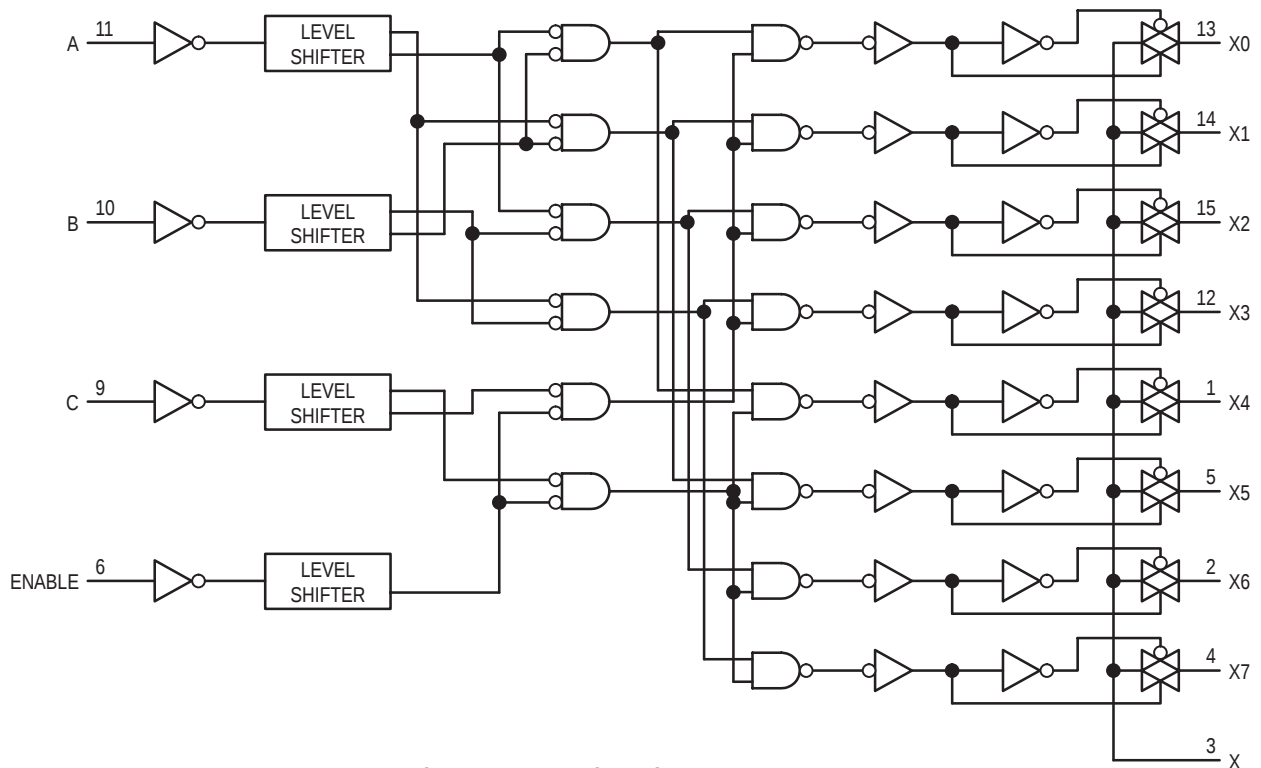


Figure 18. Function Diagram, HC4051A

MC74HC4051A, MC74HC4052A, MC74HC4053A

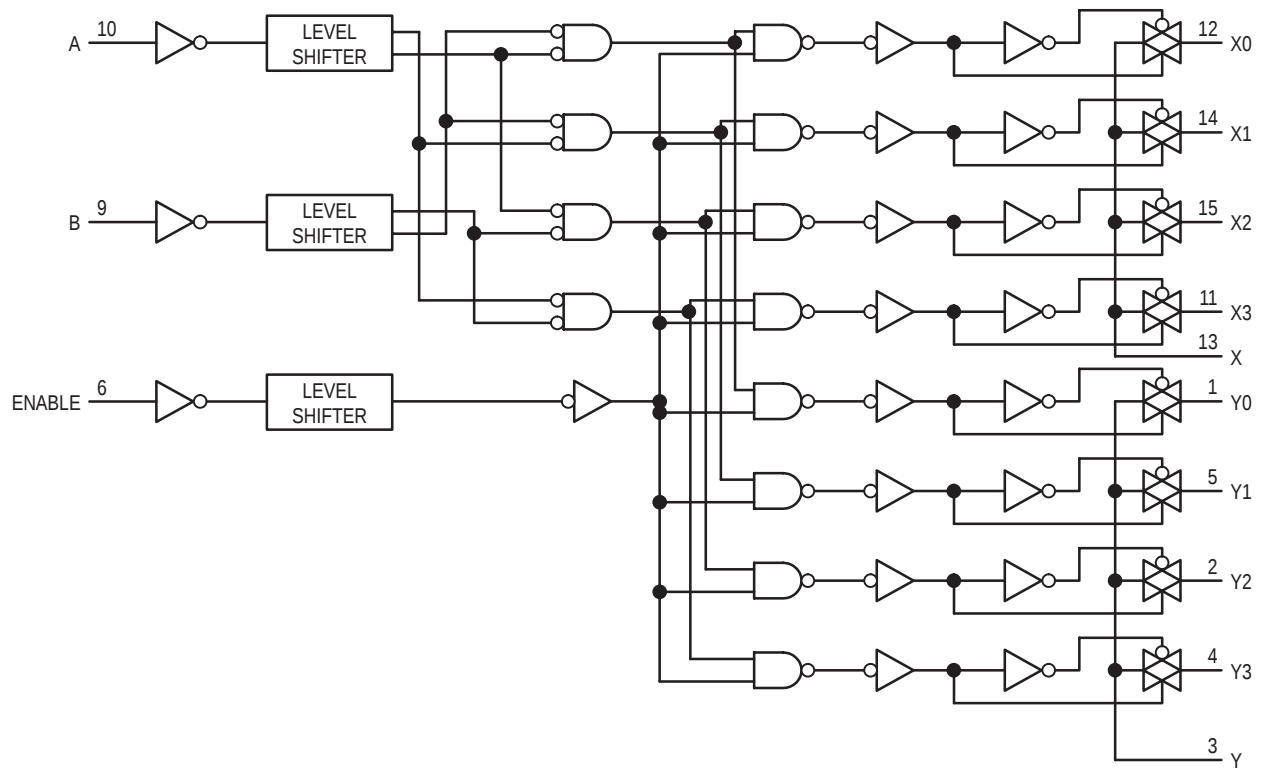


Figure 19. Function Diagram, HC4052A

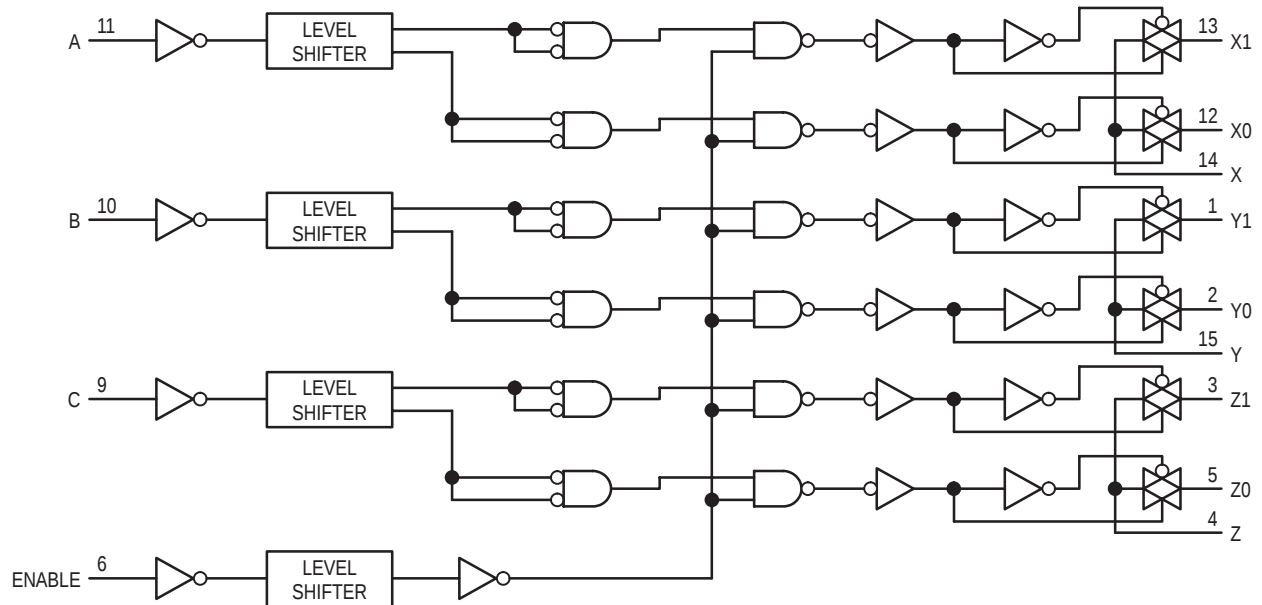


Figure 20. Function Diagram, HC4053A

MC74HC4051A, MC74HC4052A, MC74HC4053A

ORDERING & SHIPPING INFORMATION

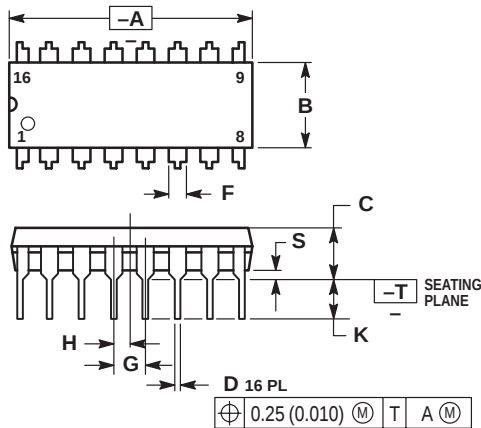
Device	Package	Shipping
MC74HC4051AN	PDIP–16	500 Units / Unit Pak
MC74HC4051AD	SOIC–16	48 Units / Rail
MC74HC4051ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4051ADT	TSSOP–16	96 Units / Rail
MC74HC4051ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4051ADW	SOIC WIDE	48 Units / Rail
MC74HC4051ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4051AF	SOEIAJ–16	See Note 1.
MC74HC4051AFEL	SOEIAJ–16	See Note 1.
MC74HC4052AN	PDIP–16	500 Units / Unit Pak
MC74HC4052AD	SOIC–16	48 Units / Rail
MC74HC4052ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4052ADT	TSSOP–16	96 Units / Rail
MC74HC4052ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4052ADW	SOIC WIDE	48 Units / Rail
MC74HC4052ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4052AF	SOEIAJ–16	See Note 1.
MC74HC4052AFEL	SOEIAJ–16	See Note 1.
MC74HC4053AN	PDIP–16	500 Units / Unit Pak
MC74HC4053AD	SOIC–16	48 Units / Rail
MC74HC4053ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4053ADT	TSSOP–16	96 Units / Rail
MC74HC4053ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4053ADW	SOIC WIDE	48 Units / Rail
MC74HC4053ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4053AF	SOEIAJ–16	See Note 1.
MC74HC4053AFEL	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC74HC4051A, MC74HC4052A, MC74HC4053A

PACKAGE DIMENSIONS

PDIP-16
N SUFFIX
CASE 648-08
ISSUE R

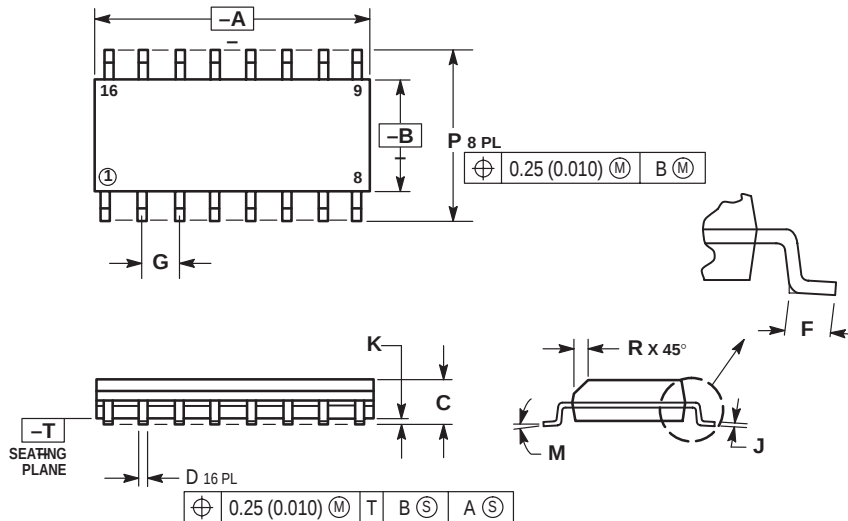


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



NOTES:

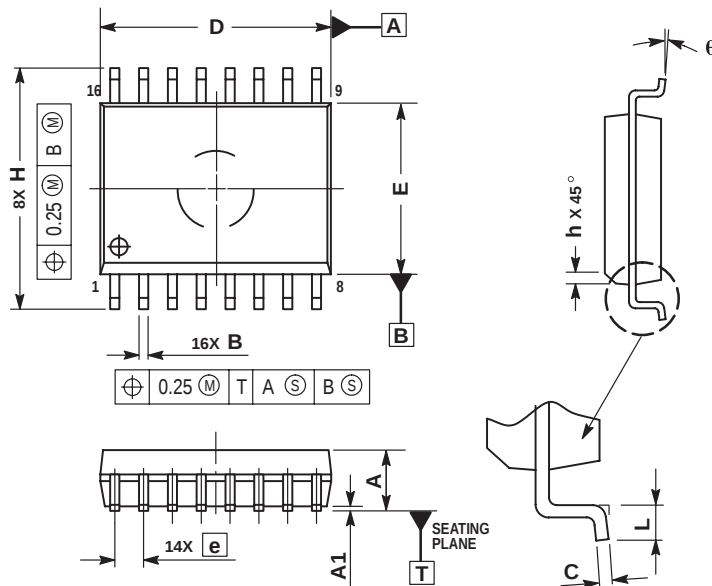
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MC74HC4051A, MC74HC4052A, MC74HC4053A

PACKAGE DIMENSIONS

SOIC-16 WIDE
DW SUFFIX
CASE 751G-03
ISSUE B

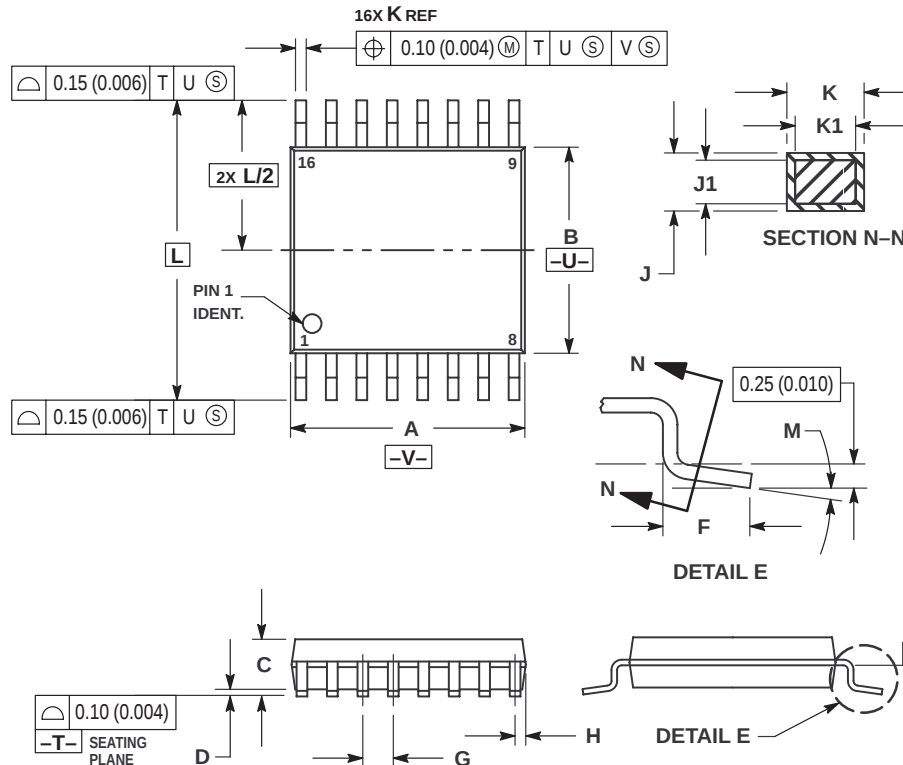


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE O



NOTES:

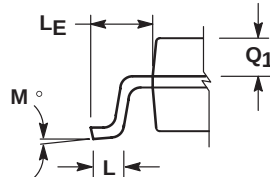
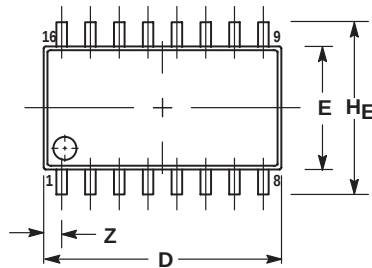
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

MILLIMETERS			INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

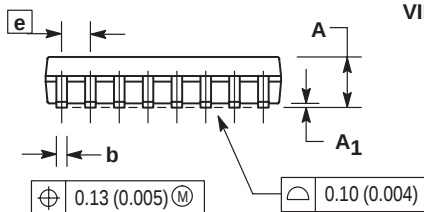
MC74HC4051A, MC74HC4052A, MC74HC4053A

PACKAGE DIMENSIONS

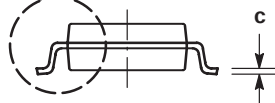
SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



DETAIL P



VIEW P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC	—	0.050 BSC	—
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, England, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549
Phone: 81-3-5740-2745
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.