19-5554; Rev 1; 10/11

EVALUATION KIT AVAILABLE

Satellite IF Switch

MAX12005

General Description

The MAX12005 satellite IF switch IC is designed for multi-user applications supporting two quad universal low-noise blocks (LNBs) to be matrix switched to four satellite receivers. The system can be easily expanded to accept 16 satellite IF inputs using the cascade option and one additional satellite IF switch IC. A configuration of eight satellite IF inputs to eight satellite receivers is also possible by using two ICs and adding eight input splitters. The insertion loss of these splitters can be compensated by a +6dB or +12dB input gain select.

There are two ways to control the switch function. Each IC contains four DiSEqC™ 2.0 decoders and four alternate tone/voltage decoders. The decoders use an integrated trimmed oscillator, simplifying the MAX12005 implementation into any system. There are four operational modes, which include LNB mode (for use within the LNB), cascade master mode, cascade slave mode, and single mode.

The satellite IF switch is designed on an advanced SiGe process and is available in a lead-free 48-pin TQFN surface-mount package (7mm x 7mm).

Applications

Direct Broadcast Satellite Receivers

Satellite IF Distribution

L-Band Distribution

Features

- **8-Input-to-4-Output Matrix Switch**
- **Expandable to 16 Inputs with Cascade Master/Slave Option**
- **950MHz to 2150MHz Operation**
- **Greater than 30dB Switch Isolation**
- **0/+6/+12dB Input Stage Gain Selection to Compensate for Splitter Insertion Loss**
  Gain Step for All Input Stages Is Commonly Controlled Through an Analog Select Pin
- **Four Integrated DiSEqC 2.0 Decoders with Integrated Oscillator**
- **Alternate Tone/Voltage Detection**
- **ESD Protected to 2kV HBM**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX12005ETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed paddle.*

DiSEqC is a trademark of EUTELSAT.

Satellite IF Switch

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND.....-0.3V to +3.6V
RFIN1–RFIN8 to GND.....-0.3V to +1.5V
CASCADE_IN1–CASCADE_IN4 to GND.....-0.3V to +1.5V
RFOUT1–RFOUT4 to GND..... -0.3V to (V_{CC} + 0.3V)
DISEQC_TX1–DISEQC_TX4 to GND .....-0.3V to (V_{CC} + 0.3V)
DISEQC_RX1–DISEQC_RX4 to GND.....-0.3V to (V_{CC} + 0.3V)
GAIN_SELECT, MODE_SELECT
to GND.....-0.3V to (V_{CC} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8 mW/°C above +70°C).....2.2W
Operating Ambient Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.5V, T_A = -40°C to +85°C, mode set to master, input gain stages set to highest gain, inputs matched to 75Ω, output loads = 75Ω. Typical values are at +3.3V and at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0		3.5	V
Supply Current	I_{CC}	V_{CC} = 3.3V, 0dB, one input selected, four outputs selected		150	250	mA
+12dB GAIN_SELECT Input High-Level Voltage	V_{IH}		V_{CC} - 0.4V			V
+6dB GAIN_SELECT Input Voltage Level and Range	V_{IN}		1/2 V_{CC} ±200mV			mV
0dB GAIN_SELECT Input Low-Level Voltage	V_{IL}				0.4	V
Single MODE_SELECT Input High-Level Voltage	V_{IH}		V_{CC} - 0.4V			V
Master MODE_SELECT Input Voltage Level and Range	V_{IN}		2/3 V_{CC} ±200mV			mV
Slave MODE_SELECT Input Voltage Level and Range	V_{IN}		1/3 V_{CC} ±200mV			mV
LNB MODE_SELECT Input Low-Level Voltage	V_{IL}				0.4	V
GAIN_SELECT and MODE_SELECT Input Current	I_{IN}	V_{IN} = V_{CC}			10	µA
DC Voltage Detect Input High Level	V_{IH}	(Note 2)	1.23			V
DC Voltage Detect Input Low Level	V_{IL}	(Note 2)			1.11	V
DISEQC_RX_ Input Current	I_{IN}	V_{IN} = high or low			1	µA
DISEQC_TX_ Output High-Level Voltage	V_{OH}	I_{LOAD} = -1mA		V_{CC} - 0.4V		V
DISEQC_TX_ Output Low-Level Voltage	V_{OL}	I_{LOAD} = +1mA		0.4		V

AC ELECTRICAL CHARACTERISTICS

(MAX12005 EV Kit, V_{CC} = +3.0V to +3.5V, f_{IN} = 950MHz, V_{IN} = 70dBµV, T_A = -40°C to +85°C, mode set to master, input gain stages set to 0dB, RF inputs matched to 75Ω, RF output loads = 75Ω. Typical values are at +3.3V and at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operation Frequency	f_{RF}		950		2150	MHz
DISEQC_RX_ Tone Input Level	V_{IN}	f_{IN} = 22kHz (Note 5)	60			mV_{P-P}
Switch Gain at 950MHz (Note 3)		0dB gain		0		dB
		+6dB gain		+6		
		+12dB gain		+12		
Cascade Input Switch Gain at 950MHz	$\|S_{21}\|$			0		dB
Switch-to-Switch Gain Match	$\Delta\|S_{21}\|$	At 950MHz (Note 4)	-1.5		+3.5	dB
Gain Slope with Frequency		Between 950MHz and 2150MHz		+3		dB
Single-Input Source Gain Change		Gain change from single output connected to a single input to four outputs connected to a single input		-0.4		dB
3rd-Order Intermodulation Product (Case 1)	IM3	Output level set to +89dBµV by varying three equal amplitude tones at 955MHz, 962MHz, and 965MHz; measure products at 952MHz and 958MHz		-35		dBc
3rd-Order Intermodulation Product (Case 2)	IM3	Output level set to +89dBµV by varying three equal amplitude tones at 2135MHz, 2142MHz, and 2145MHz; measure products at 2132MHz and 2138MHz			-34	dBc
RFIN1–RFIN8 Input Return Loss	$\|S_{11}\|$			-12		dB
CASCADE_IN1–CASCADE_IN4 Input Return Loss	$\|S_{11}\|$			-12		dB
RFOUT1–RFOUT4 Output Return Loss	$\|S_{22}\|$			-12		dB
Switch Isolation				55		dB
Port-to-Port Isolation				33		dB
DiSEqC Clock	f_{OSC}			8		MHz

Note 1: Production tested at +25°C; guaranteed by design and characterization at -40°C and +85°C.

Note 2: To supply the specified input-voltage-detect levels requires the use of a voltage-divider comprised of 12.7kΩ and 1.02kΩ ±0.5% tolerance resistors. The voltage being divided is expected to be V_{OL} = 14.75V maximum and V_{OH} = 16.75V minumum.

Note 3: The common input gain step is set by analog control. All gain measurements have only one output connect to each input. Switch gain measurements do not include cascade inputs as part of the switch signal path.

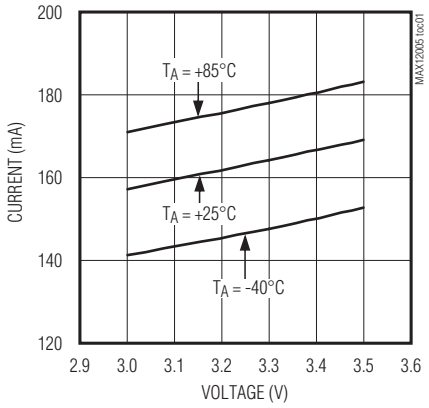
Note 4: Switch-to-switch gain match is defined as each switch to every other switch gain match. Each switch must be set up with the same input gain step.

Note 5: $60mV_{P-P}$ square wave for f_{IN} = 22kHz. For sine wave, the typical minimum is $100mV_{P-P}$.

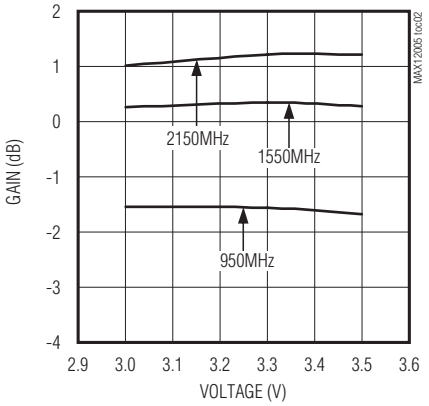
Typical Operating Characteristics

(MAX12005 EV Kit, V_{CC} = +3.0V to +3.5V, f_{IN} = 950MHz, V_{IN} = 70dBµV, T_A = -40°C to +85°C, mode set to master, input gain stages set to 0dB, RF inputs matched to 75Ω, RF output loads = 75Ω. Typical values are at +3.3V and at T_A = +25°C, unless otherwise noted. Production tested at +25°C; guaranteed by design and characterization at -40°C and +85°C.)

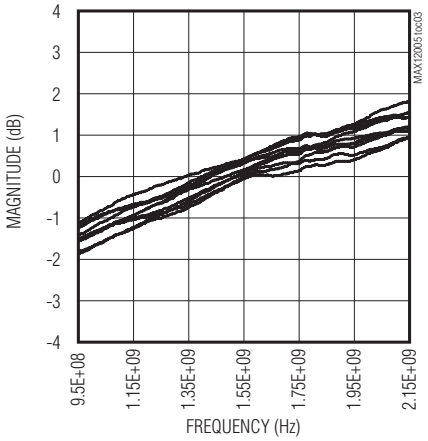
VOLTAGE vs. CURRENT (0dB GAIN)



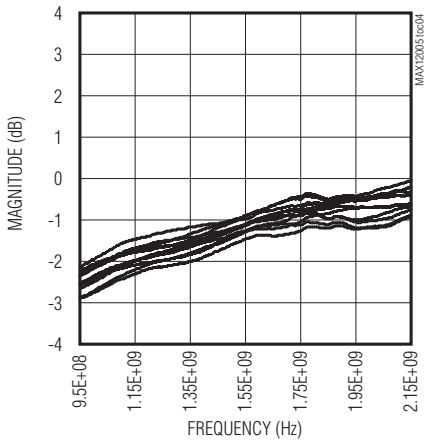
VOLTAGE vs. GAIN (+25°C)



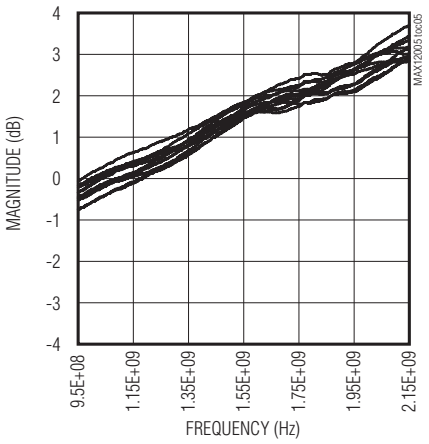
S21 +25°C (0dB GAIN, VAR. IN/OUT)



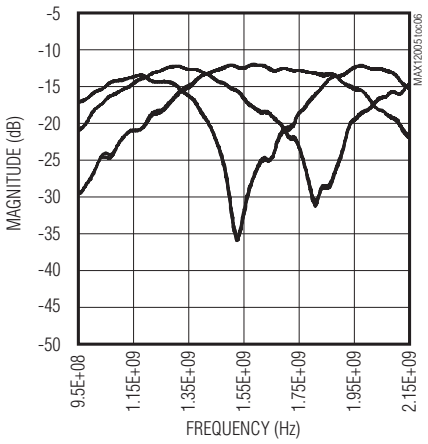
S21 +85°C (0dB GAIN, VAR. IN/OUT)



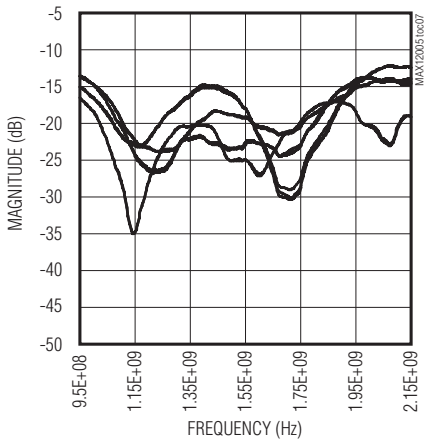
S21 -40°C (0dB GAIN, VAR. IN/OUT)



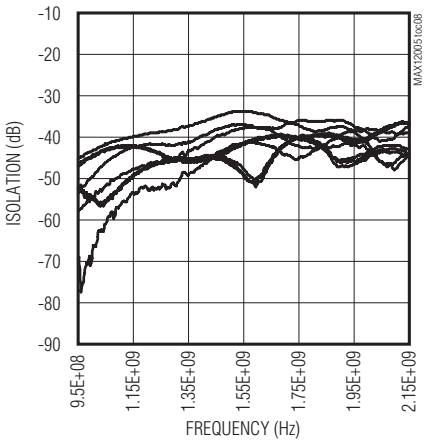
RF S11 (VAR. INPUT)



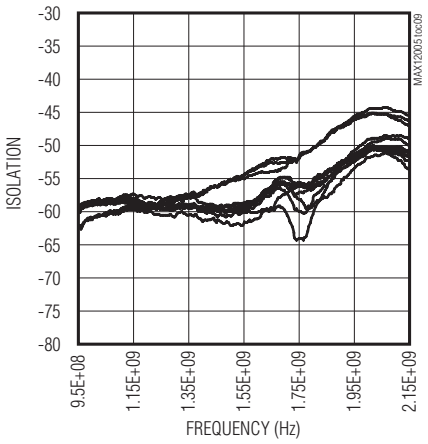
RF S22 (VAR. OUTPUT)



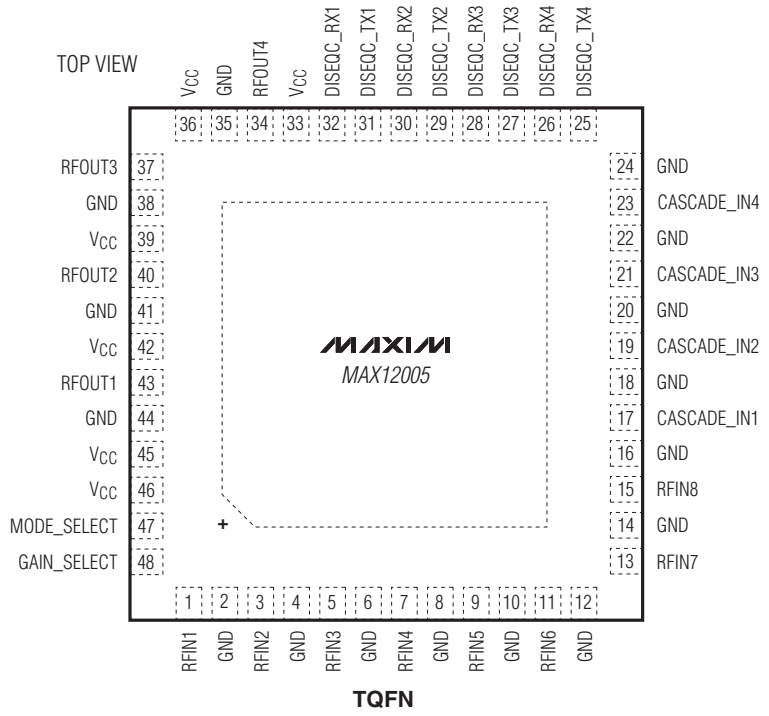
PORT-TO-PORT ISOLATION (VAR. PORTS)



SWITCH ISOLATION (VAR. CH)



Pin Configuration



TQFN

Pin Description

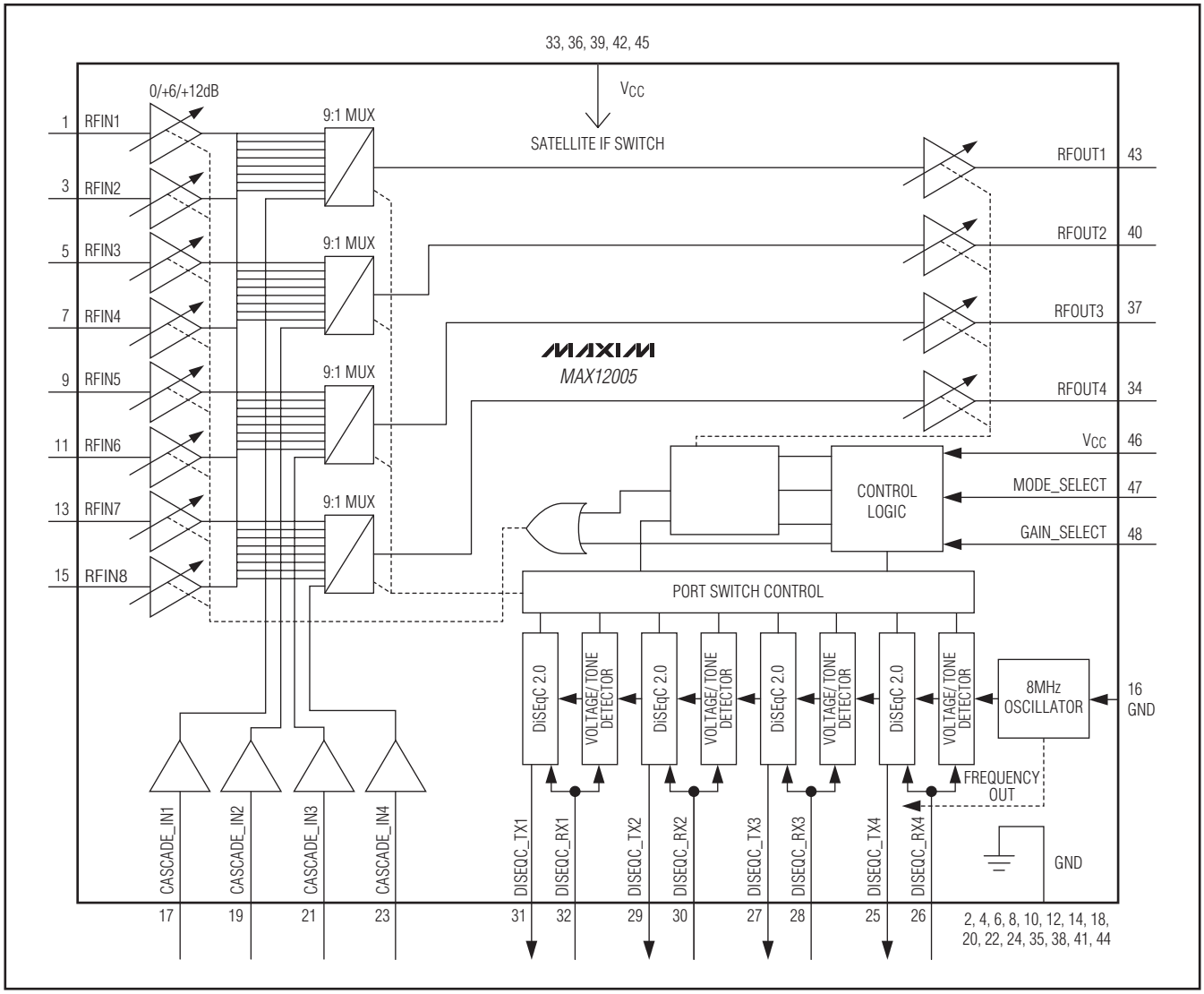
PIN	NAME	FUNCTION
1	RFIN1	RF Input from LNB
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 35, 38, 41, 44	GND	Electrical Ground
3	RFIN2	RF Input from LNB
5	RFIN3	RF Input from LNB
7	RFIN4	RF Input from LNB
9	RFIN5	RF Input from LNB
11	RFIN6	RF Input from LNB
13	RFIN7	RF Input from LNB
15	RFIN8	RF Input from LNB
17	CASCADE_IN1	Cascade Input from RF Output of Second MAX12005 in Slave Mode
19	CASCADE_IN2	Cascade Input from RF Output of Second MAX12005 in Slave Mode
21	CASCADE_IN3	Cascade Input from RF Output of Second MAX12005 in Slave Mode
23	CASCADE_IN4	Cascade Input from RF Output of Second MAX12005 in Slave Mode

Satellite IF Switch

Pin Description (continued)

PIN	NAME	FUNCTION
25	DISEQC_TX4	Return DiSEqC Signal Output to Satellite Receiver (Master) or Outputs Envelope of Received DiSEqC Signal for Use by External Controller
26	DISEQC_RX4	Input for DiSEqC Slave Signal from Satellite Receiver or Master
27	DISEQC _TX3	Return DiSEqC Signal Output to Satellite Receiver (Master) or Outputs Envelope of Received DiSEqC Signal for Use by External Controller
28	DISEQC _RX3	Input for DiSEqC Slave Signal from Satellite Receiver or Master
29	DISEQC _TX2	Return DiSEqC Signal Output to Satellite Receiver (Master) or Outputs Envelope of Received DiSEqC Signal for Use by External Controller
30	DISEQC _RX2	Input for DiSEqC Slave Signal from Satellite Receiver or Master
31	DISEQC _TX1	Return DiSEqC Signal Output to Satellite Receiver (Master) or Outputs Envelope of Received DiSEqC Signal for Use by External Controller
32	DISEQC _RX1	Input for DiSEqC Slave Signal from Satellite Receiver or Master
33, 36, 39, 42, 45, 46	V_{CC}	3.0V to 3.5V Supply. Analog supply pins 33, 36, 39, and 42. Digital supply pins 45 and 46.
34	RFOUT4	RF Output to Satellite Receiver
37	RFOUT3	RF Output to Satellite Receiver
40	RFOUT2	RF Output to Satellite Receiver
43	RFOUT1	RF Output to Satellite Receiver
47	MODE_SELECT	Satellite Switch Mode Select
48	GAIN_SELECT	Gain Select for All Input Stages
—	EP	Exposed Pad Ground. The exposed pad must be soldered to the circuit board for proper thermal and electrical performance.

Functional Diagram



Satellite IF Switch

Detailed Description

The MAX12005 satellite IF switch features eight 75Ω inputs with three selectable gain steps of 0, +6dB, and +12dB. Each of the eight input amplifiers feeds into four nine-to-one multiplexers with the switching controlled by voltage/tone or DiSEqC signaling from up to four receivers. The output of each multiplexer is then sent to a satellite receiver through a 75Ω buffered output stage.

The satellite IF switch has four modes of operation. Two modes are used to increase the number of IF inputs by cascading two MAX12005 ICs together. The first IC is set to master mode to enable the four cascade inputs. The second IC is set to slave mode with its outputs connected to the cascade inputs of the master IC.

The LNB mode sets up the IC to recognize LNB DiSEqC signaling to control switching and ignore DiSEqC signaling for multiswitch applications. The single mode sets up the IC to recognize multiswitch DiSEqC signaling to control switching and ignore LNB DiSEqC signaling. For the LNB, single, and slave modes, the four cascade inputs are disabled.

Input Gain Select

The voltage supplied to the GAIN_SELECT pin provides the selection for one of three gain settings available at all eight input stages, as follows:

GND = 0dB

1/2 V_{CC} = +6dB

V_{CC} = +12dB

The +6dB gain step voltage can be set through the use of a simple supply voltage-divider. This gain select feature is intended to compensate for input signal losses due to the use of input RF signal splitters.

Chip Mode Select

The voltage supplied to the MODE_SELECT pin provides the selection for one of four IC operational modes, as follows:

GND = LNB Mode

1/3 V_{CC} = Slave Mode (Cascade Operation)

2/3 V_{CC} = Master Mode (Cascade Operation)

V_{CC} = Single Mode

The slave mode and master mode voltages can be set through the use of simple supply voltage-dividers.

Switch Control

Voltage/tone signaling is the default switch control after power-up or when a receiver is connected or reconnected with the die power on. After an individual decoder receives a DiSEqC signal, that decoder switches from voltage/one control to DiSEqC control until a new receiver connection is made or when the IC has a power-on reset.

Layout Considerations

To minimize coupling between different sections of the IC, a star power-supply routing configuration with a large decoupling capacitor at a central V_{CC} node is recommended. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the circuit. Place a bypass capacitor as close as possible to each supply pin. This arrangement provides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor for a low-inductance ground connection. Do not share the capacitor ground vias with any other branch. The MAX12005 EV kit can be used as a starting point for layout. For best performance, take into consideration grounding and routing of RF, baseband, and power-supply PCB proper line. Make connections from vias to the ground plane as short as possible. On the high-impedance ports, keep traces short to minimize shunt capacitance. EV kit schematic and Gerber files can be found at **www.maxim-ic.com**.

SPI is a trademark of Motorola, Inc.

DiSEqC Slave Control Interface

The DiSEqC interface is designed according to the DiSEqC Bus Functional Specification version 4.2. All framing bytes 0xE0 through 0xE7 are supported. The following address bytes are supported:

0x00	Any device
0x10	Any LNB, switcher, or SMATV
0x11	LNB
0x14	Switcher, DC-blocking

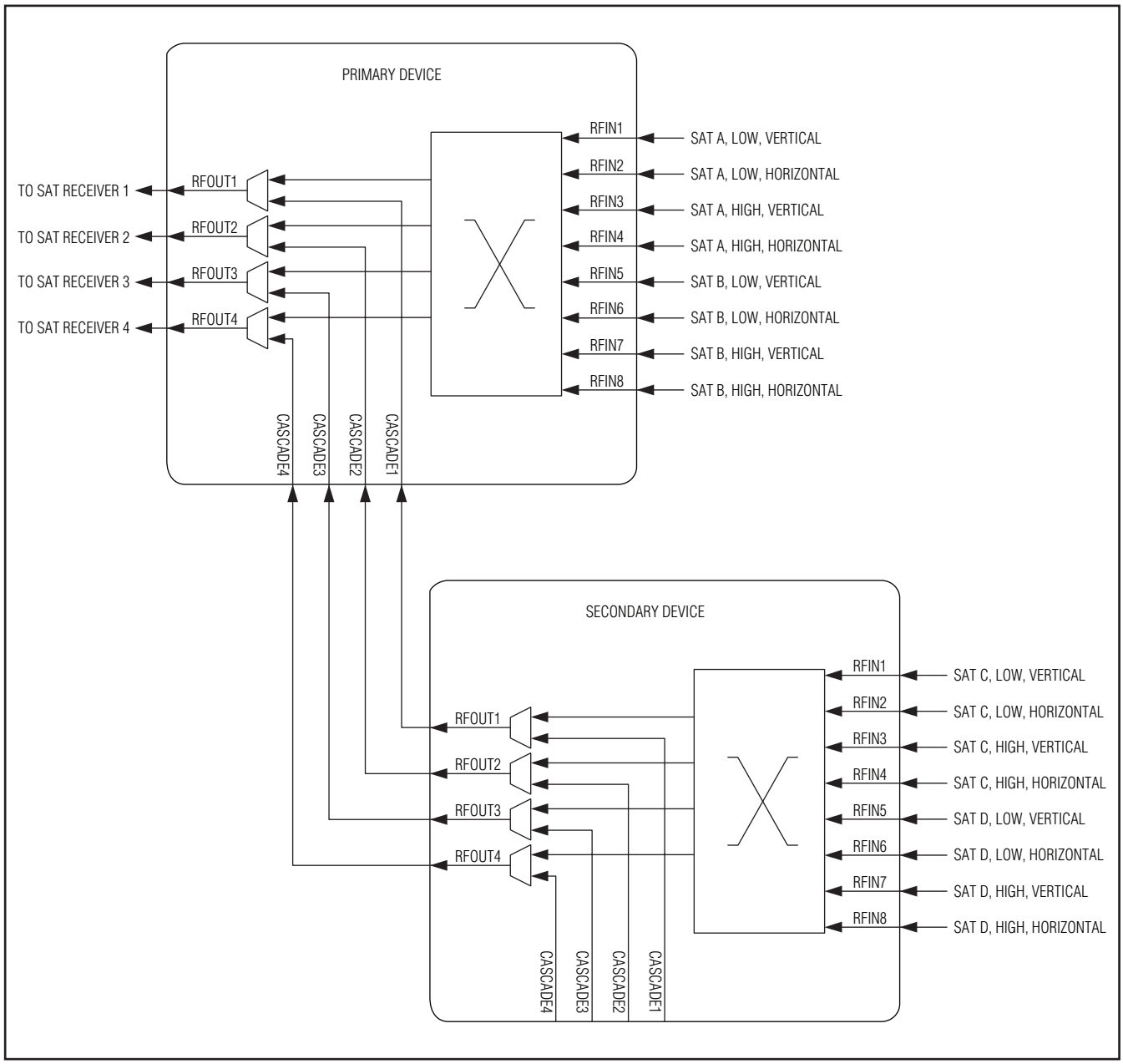


Figure 1. Typical Cascade Connection Between Two Satellite Switch ICs

Satellite IF Switch

Table 1 shows the coherence between the terms used by the DiSEqC standard and the pin names used by the MAX12005 along with the command sequences used to control switching.

Table 2 lists the supported command bytes. The command byte is the 3.byte in the DiSEqC master frame (refer to the DiSEqC Bus Functional Specification version 4.2, top of page 13). The DiSEqC slave only sends a reply if requested by a framing byte 0xE2 or 0xE3 in the master frame (refer to DiSEqC Bus Functional Specification version 4.2, bottom of page 13). All DiSEqC commands control the contents of the DiSEqC registers described in chapter 7.1.

Table 3 lists the supported command bytes. The DiSEqC commands are internally mapped to individually named registers. The registers do not have an address.

Table 1. DiSEqC Slave Control Interface

DEVICE (Note 1)	INPUT	SIGNAL FROM	DiSEqC COMMAND SEQUENCE (Note 2)
Primary	RFIN1	Satellite A, low band, vertical polarization	0x23, 0x22, 0x20, 0x21
	RFIN2	Satellite A, low band, horizontal polarization	0x23, 0x22, 0x20, 0x25
	RFIN3	Satellite A, high band, vertical polarization	0x23, 0x22, 0x24, 0x21
	RFIN4	Satellite A, high band, horizontal polarization	0x23, 0x22, 0x24, 0x25
	RFIN5	Satellite B, low band, vertical polarization	0x23, 0x26, 0x20, 0x21
	RFIN6	Satellite B, low band, horizontal polarization	0x23, 0x26, 0x20, 0x25
	RFIN7	Satellite B, high band, vertical polarization	0x23, 0x26, 0x24, 0x21
	RFIN8	Satellite B, high band, horizontal polarization	0x23, 0x26, 0x24, 0x25
Secondary	RFIN1	Satellite C, low band, vertical polarization	0x27, 0x22, 0x20, 0x21
	RFIN2	Satellite C, low band, horizontal polarization	0x27, 0x22, 0x20, 0x25
	RFIN3	Satellite C, high band, vertical polarization	0x27, 0x22, 0x24, 0x21
	RFIN4	Satellite C, high band, horizontal polarization	0x27, 0x22, 0x24, 0x25
	RFIN5	Satellite D, low band, vertical polarization	0x27, 0x26, 0x20, 0x21
	RFIN6	Satellite D, low band, horizontal polarization	0x27, 0x26, 0x20, 0x25
	RFIN7	Satellite D, high band, vertical polarization	0x27, 0x26, 0x24, 0x21
	RFIN8	Satellite D, high band, horizontal polarization	0x27, 0x26, 0x24, 0x25

Note 1: The primary device outputs connect directly to the satellite receivers. The secondary device outputs connect to the primary device through the cascade inputs. Also see Figure 1.

Note 2: Only those DiSEqC commands that differ between sequences have to be sent to change the input, not all four commands. By default RFIN1 from the primary device is selected.

The DiSEqC interface is designed according to the DiSEqC Bus Functional Specification version 4.2.

Table 2. DiSEqC Slave Control Interface Command Bytes

HEX VALUE	COMMAND	FUNCTION	DATA BYTES	SLAVE REPLY
0x00	Reset	Reset DiSEqC decoder	—	Framing byte
0x01	Clr Reset	Clear reset flag *Clears Status_reg, bit 0*	—	Framing byte
0x04	Set Contend	Set contention flag *Sets Status_reg, bit 7*	—	Framing byte
0x05	Contend	Return address only if contention flag is set *Reads Address_reg*	—	Framing + data byte
0x06	Clr Contend	Clear contention flag *Clears Status_reg, bit 7*	—	Framing byte
0x07	Address	Return address unless contention flag is set *Reads Address_reg*	—	Framing + data byte
0x08	Move C	Change address only if contention flag is set *Writes to Address_reg*	1 byte	Framing byte
0x09	Move	Change address unless contention flag is set *Writes to Address_reg*	1 byte	Framing byte
0x10	Status	Read status register flags *Reads Status_reg*	—	Framing + data byte
0x11	Config	Read configuration flags *Reads Configuration_reg*	—	Framing + data byte
0x14	Switch 0	Read switching state flags *Reads Switch_reg*	—	Framing + data byte
0x20	Set Lo	Select the low local oscillator frequency *Clears Switch_reg, bit 4*	—	Framing byte
0x21	Set VR	Select vertical polarization (or right circular) *Clears Switch_reg, bit 5*	—	Framing byte
0x22	Set Pos A	Select satellite position A (or position C) *Clears Switch_reg, bit 6*	—	Framing byte
0x23	Set S0A	Select switch option A (i.e. positions A/B) *Clears Switch_reg, bit 7*	—	Framing byte
0x24	Set Hi	Select the high local oscillator frequency *Sets Switch_reg, bit 4*	—	Framing byte
0x25	Set HL	Select horizontal polarization (or left circular) *Sets Switch_reg, bit 5*	—	Framing byte
0x26	Set Pos B	Select satellite position B (or position D) *Sets Switch_reg, bit 6*	—	Framing byte
0x27	Set S0B	Select switch option B (i.e. positions C/D) *Sets Switch_reg, bit 7*	—	Framing byte
0x30	Sleep	Ignore all bus commands except Awake *Sets Status_reg, bit 1*	—	Framing byte
0x31	Awake	Respond to future bus commands normally *Clears Status_reg, bit 1*	—	Framing byte

Table 2. DiSEqC Slave Control Interface Command Bytes (continued)

HEX VALUE	COMMAND	FUNCTION	DATA BYTES	SLAVE REPLY
0x38	Write N0	Write to port group 0 *Controls Switch_reg, bits 7 downto 4* (Note 1)	1 byte	Framing byte
0x50	LO string	Read current frequency *Reads Low_LOF_reg2/1 or High_LOF_reg2/1 depending on Switch_reg, bit 4* (Note 2)	—	Framing + 2 data bytes
0x51	LO now	Read current frequency table entry number *Reads Low_LOF_reg0, bit 3 downto 0 or High_LOF_reg0, bit 3 downto 0 depending on Switch_reg, bit 4*	—	Framing + data byte
0x52	LO Lo	Read low-frequency table entry number *Reads Low_LOF_reg0, bit 3 downto 0*	—	Framing + data byte
0x53	LO Hi	Read high-frequency table entry number *Reads High_LOF_reg0, bit 3 downto 0*	—	Framing + data byte

Note 1: Refer to DiSEqC Bus Functional Specification version 4.2, page 18.
Note 2: Refer to DiSEqC Bus Functional Specification version 4.2, page 22.

Table 3. DiSEqC Slave Control Interface Registers

ADDRESS	BIT	ACC	NAME	FUNCTION	DEFAULT
Address_reg	7:0	RW	address	DiSEqC address	LNB: 0x11 Switch: 0x14
Status_reg	7	RW	contention	Bus contention flag	0
	6	R	standby	Standby mode	0
	5	—	*Unused*	—	—
	4	R	aux_power	Auxiliary power available	0
	3	—	*Unused*	—	—
	2	RW	voltage	0 = Low DC, 1 = High DC	Depends on voltage input
	1	RW	sleep	0 = Awake, 1 = Sleep	0
	0	RW	reset	Reset flag	1
Configuration_reg	7	R	analog	Analog output facility	0
	6	R	standby	Standby facility	0
	5	R	positioner	Positioner capability	0
	4	R	power_detection	External power-detection capability	0
	3	R	loop_through	Loopthrough facility	0
	2	R	polarizer	Polarizer capability	0
	1	R	switch	Switcher capability	1
	0	R	lof_values	LOF value output capability	1

Table 3. DiSEqC Slave Control Interface Registers (continued)

ADDRESS	BIT	ACC	NAME	FUNCTION	DEFAULT
Switch_reg	7	RW	option	0 = Positions A/B, 1 = Positions C/D	0
	6	RW	satellite	0 = Satellite A(C), 1 = Satellite B(D)	0
	5	RW	polarization	0 = Vertical, 1 = Horizontal	0
	4	RW	band	0 = Low band, 1 = High band	0
	3	RW	option_switchable	Options switch available	Depends on cascade input
	2	R	satellite_switchable	Satellite switch available	1
	1	R	polarization_switchable	Polarization switch available	1
	0	R	band_switchable	Band switch available	1
Low_LOF_reg_2	7:4	R	low_10GHz	Low LOF value, 10GHz digit	0000
	3:0	R	low_1GHz	1GHz digit	1001
Low_LOF_reg_1	7:4	R	low_100MHz	100MHz digit	0111
	3:0	R	low_10MHz	10MHz digit	0101
Low_LOF_reg_0	7:4	R	low_1MHz	1MHz digit	0000
	3:0	R	low_table_entry	Table entry number	0010
High_LOF_reg_2	7:4	R	high_10GHz	High LOF value, 10GHz digit	0001
	3:0	R	high_1GHz	1GHz digit	0000
High_LOF_reg_1	7:4	R	high_100MHz	100MHz digit	0110
	3:0	R	high_10MHz	10MHz digit	0000
High_LOF_reg_0	7:4	R	high_1MHz	1MHz digit	0000
	3:0	R	high_table_entry	Table entry number	0100

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN	T4877+4	21-0144	90-0130

Satellite IF Switch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	11/11	Added Note 5 to *Electrical Characteristics* table	3