

12MHz, High Input Impedance, Operational Amplifier

HA-2505 is an operational amplifier whose design is optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

This dielectrically isolated amplifier is ideally suited for applications such as data acquisition, RF, video, and pulse conditioning circuits. Slew rates of $\pm 30V/\mu s$ and 330ns (0.1%) settling time make this device an excellent component in fast, accurate data acquisition and pulse amplification designs. 12MHz small signal bandwidth and 500kHz power bandwidth make this device well suited to RF and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2505 is particularly useful in signal conditioning designs.

The gain and offset voltage figures of the HA-2505 are optimized by internal component value changes while the similar design of the HA-2515 is maximized for slew rate.

MIL-STD-883 product and data sheets are available upon request.

Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. NO.
HA3-2505-5	0 to 75	8 Ld PDIP	E8.3

Features

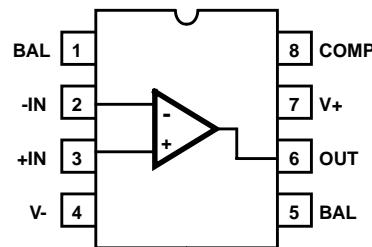
- Slew Rate 30V/ μ s
- Fast Settling 330ns
- Full Power Bandwidth 500kHz
- Gain Bandwidth 12MHz
- High Input Impedance 50M Ω
- Low Offset Current 10nA
- Internally Compensated For Unity Gain Stability

Applications

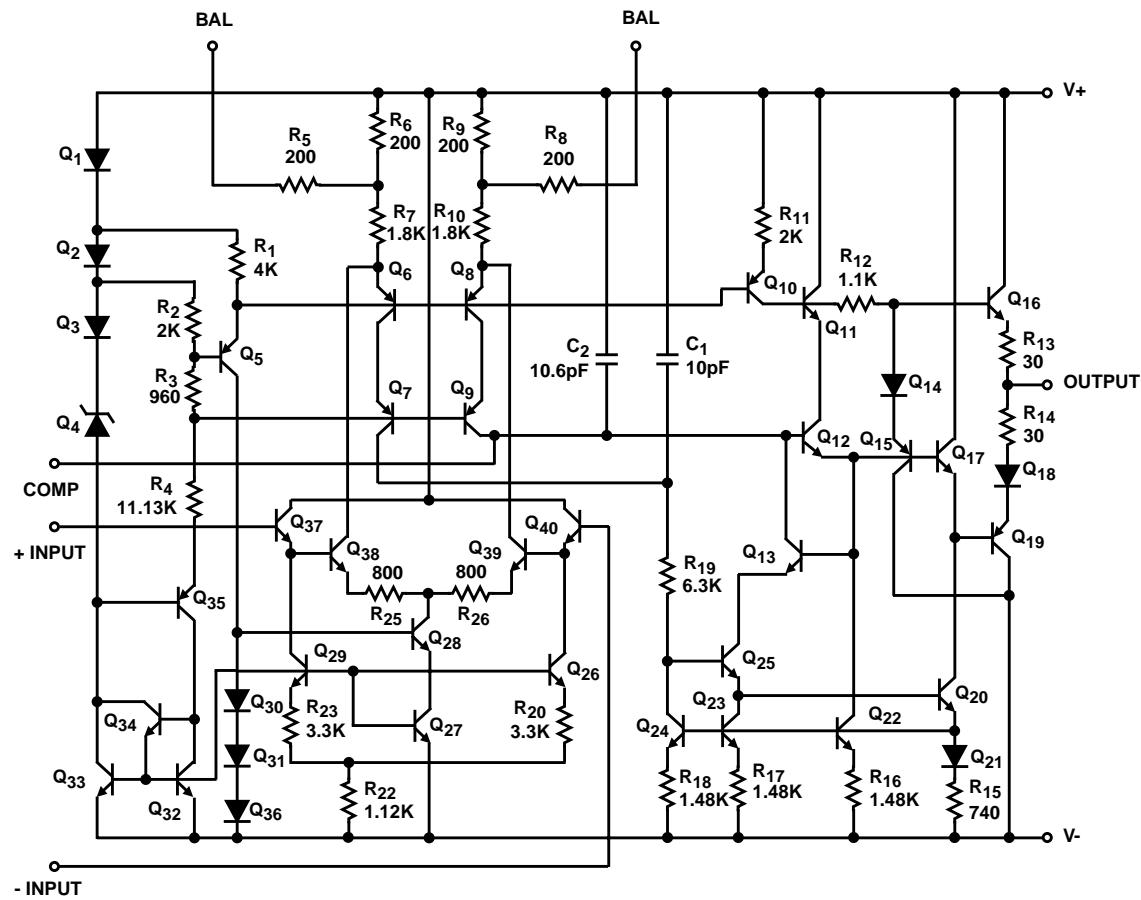
- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators

Pinout

HA-2505 (PDIP)
TOP VIEW



Schematic



Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals	40V
Differential Input Voltage	15V
Peak Output Current	50mA

Operating Conditions

Temperature Range HA-2505-5	0°C to 75°C
--------------------------------------	-------------

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_S = \pm 15V$

PARAMETER	TEMP (°C)	HA-2505-5			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Offset Voltage	25	-	4	8	mV
	Full	-	-	10	mV
Offset Voltage Average Drift	Full	-	20	-	µV/°C
Bias Current	25	-	125	250	nA
	Full	-	-	500	nA
Offset Current	25	-	20	50	nA
	Full	-	-	100	nA
Input Resistance (Note 2)	25	20	50	-	MΩ
Common Mode Range	Full	±10	-	-	V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 3, 6)	25	15	25	-	kV/V
	Full	10	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	74	90	-	dB
Gain Bandwidth Product (Note 5)	25	-	12	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 3)	Full	±10	±12	-	V
Output Current (Note 6)	25	±10	±20	-	mA
Full Power Bandwidth (Notes 6, 11)	25	300	500	-	kHz
TRANSIENT RESPONSE					
Rise Time (Notes 3, 7, 8, 9)	25	-	25	50	ns
Overshoot (Notes 3, 7, 8, 9)	25	-	25	50	%
Slew Rate (Notes 3, 7, 9, 12)	25	±20	±30	-	V/µs
Settling Time to 0.1% (Notes 3, 7, 9, 12)	25	-	0.33	-	µs
POWER SUPPLY CHARACTERISTICS					
Supply Current	25	-	4	6	mA
PSRR (Note 10)	Full	74	90	-	dB

NOTES:

2. This parameter value is based on design calculations.
3. $R_L = 2k\Omega$.
4. $V_{CM} = \pm 10V$.
5. $A_V > 10$.
6. $V_O = \pm 10V$.
7. $C_L = 50pF$.
8. $V_O = \pm 200mV$.
9. See Transient Response Test Circuits and Waveforms.
10. $\Delta V = \pm 5V$.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \text{Slew Rate}/2\pi V_{PEAK}$.
12. $V_{OUT} = \pm 5V$.

Test Circuits and Waveforms

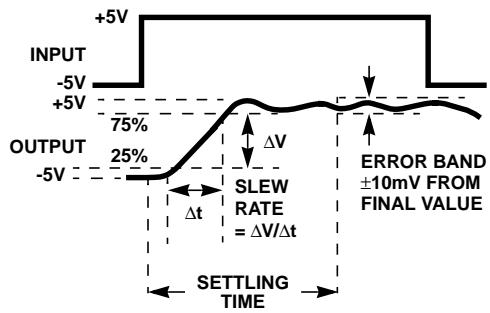
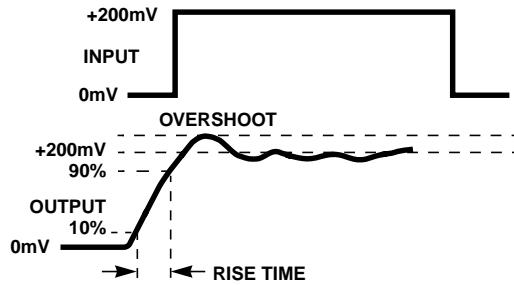


FIGURE 1. SLEW RATE AND SETTLING TIME



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE

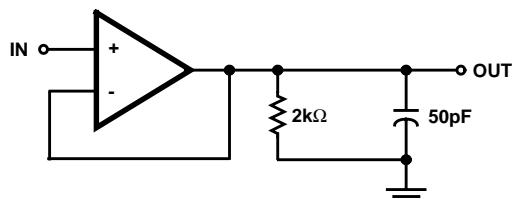
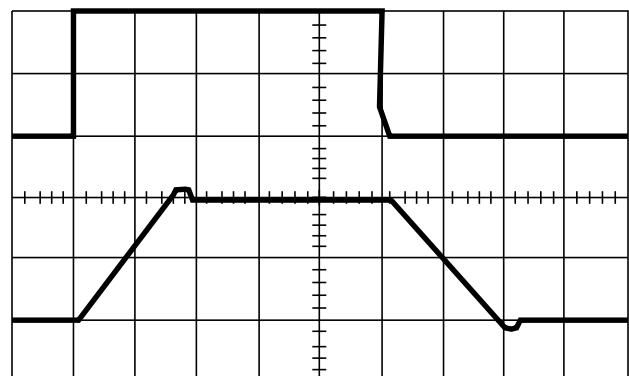
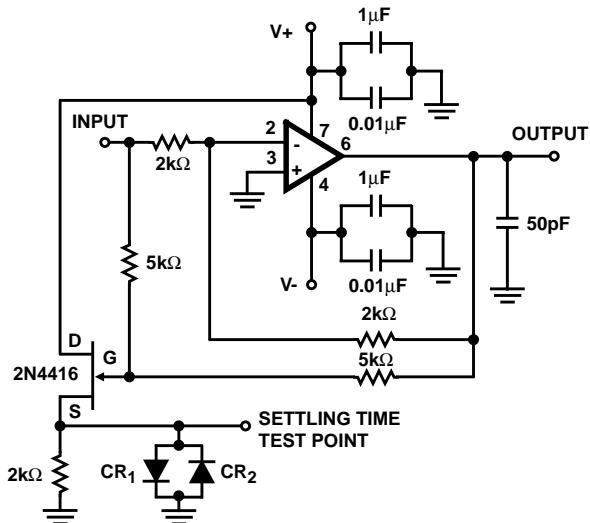


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE



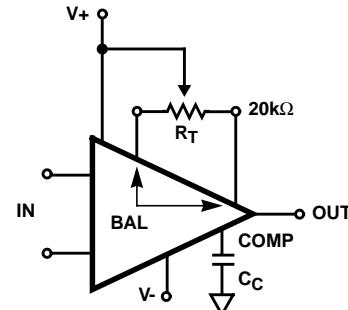
$R_L = 2k\Omega$, $C_L = 50pF$
 Upper Trace: Input
 Lower Trace: Output
 $T_A = 25^\circ C$, $V_S = \pm 15V$

FIGURE 4. VOLTAGE FOLLOWER PULSE RESPONSE



13. $A_V = -1$.
14. Feedback and Summing Resistor Ratios should be 0.1% matched.
15. Clipping Diodes CR₁ and CR₂ are optional. HP5082-2810 recommended.

FIGURE 5. SETTLING TIME TEST CIRCUIT



NOTE: Tested offset adjustment range is $|V_{OS} + 1mV|$ minimum referred to output. Typical ranges are $\pm 6mV$ with $R_T = 20k\Omega$.

FIGURE 6. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified

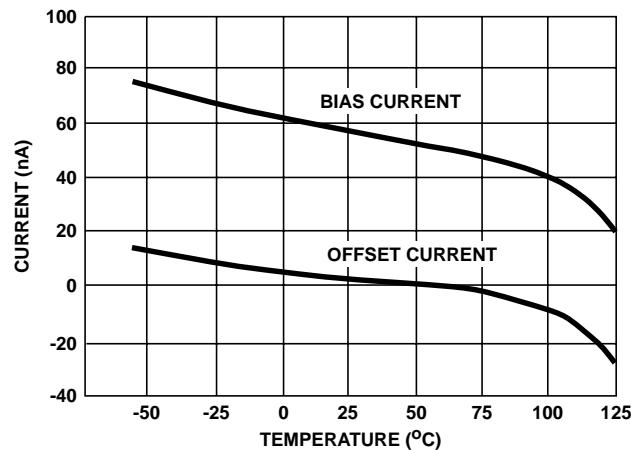


FIGURE 7. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

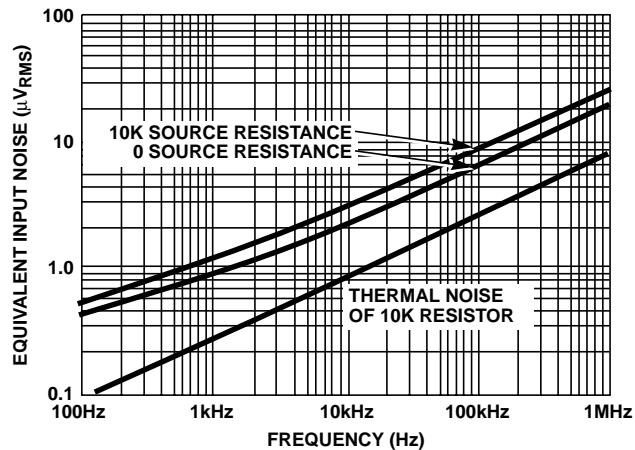


FIGURE 8. EQUIVALENT INPUT NOISE vs BANDWIDTH (WITH 10Hz HIGH PASS FILTER)

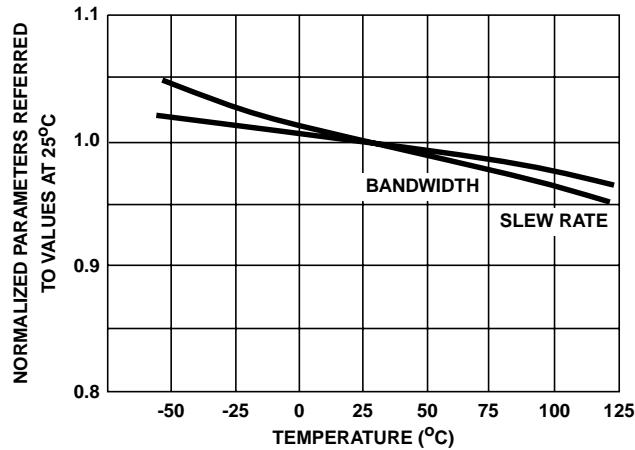


FIGURE 9. NORMALIZED AC PARAMETERS vs TEMPERATURE

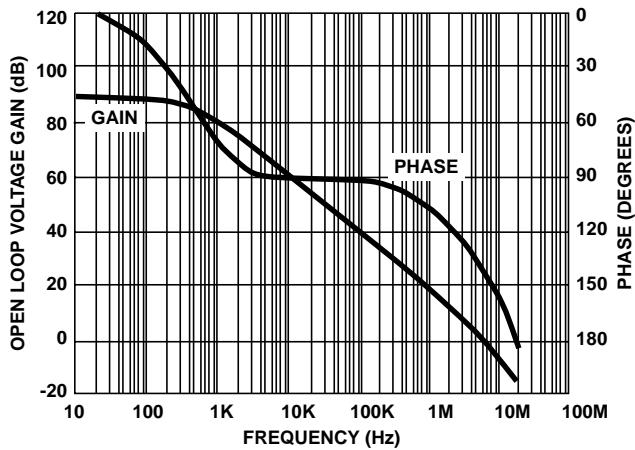


FIGURE 10. OPEN LOOP FREQUENCY AND PHASE RESPONSE

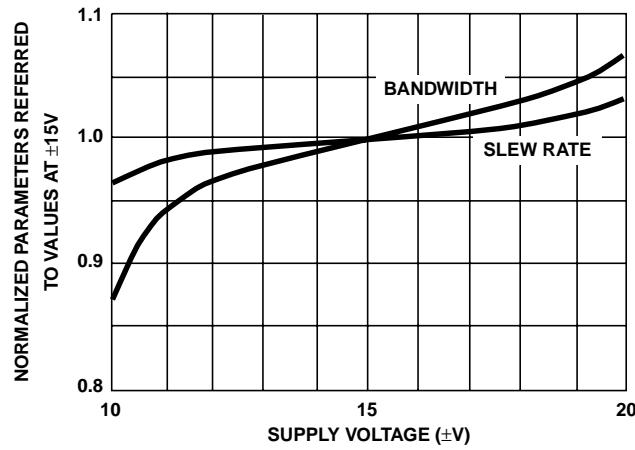
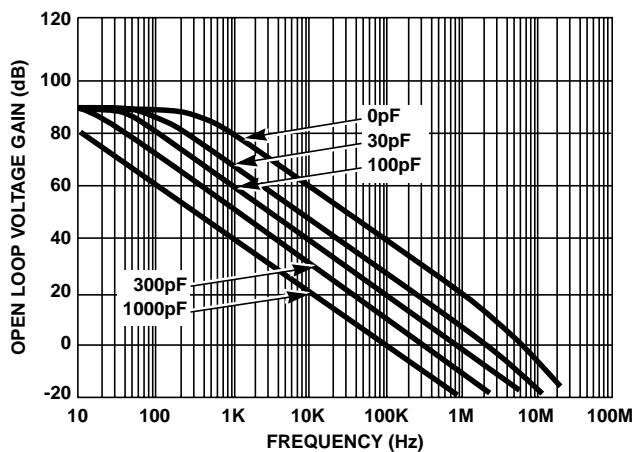


FIGURE 11. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE



NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

FIGURE 12. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

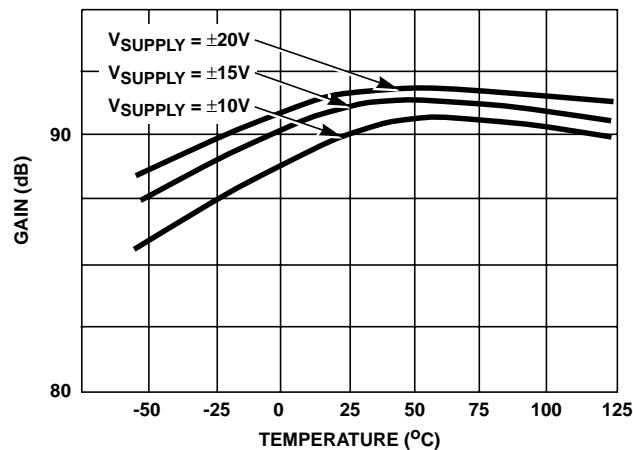
Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^{\circ}C$, Unless Otherwise Specified **(Continued)**

FIGURE 13. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

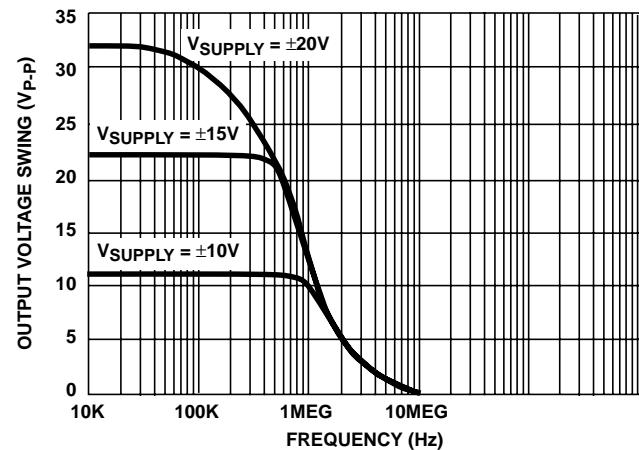


FIGURE 14. OUTPUT VOLTAGE SWING vs FREQUENCY

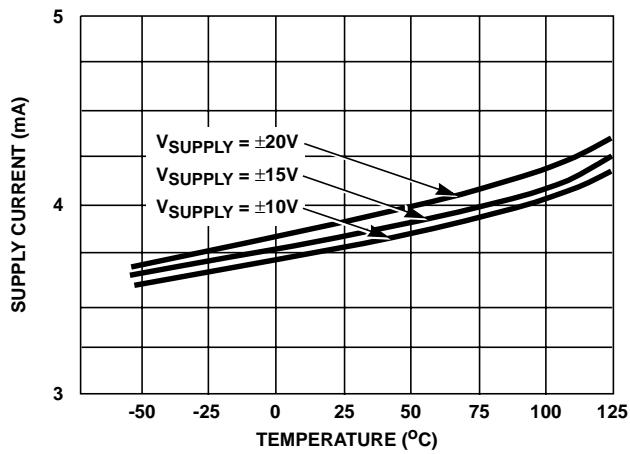


FIGURE 15. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

57 mils x 65 mils x 19 mils
1450 μ m x 1650 μ m x 483 μ m

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16k \AA \pm 2k \AA

PASSIVATION:

Type: Nitride (Si₃N₄) over Silox (SiO₂, 5% Phos.)
Silox Thickness: 12k \AA \pm 2k \AA
Nitride Thickness: 3.5k \AA \pm 1.5k \AA

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

TRANSISTOR COUNT:

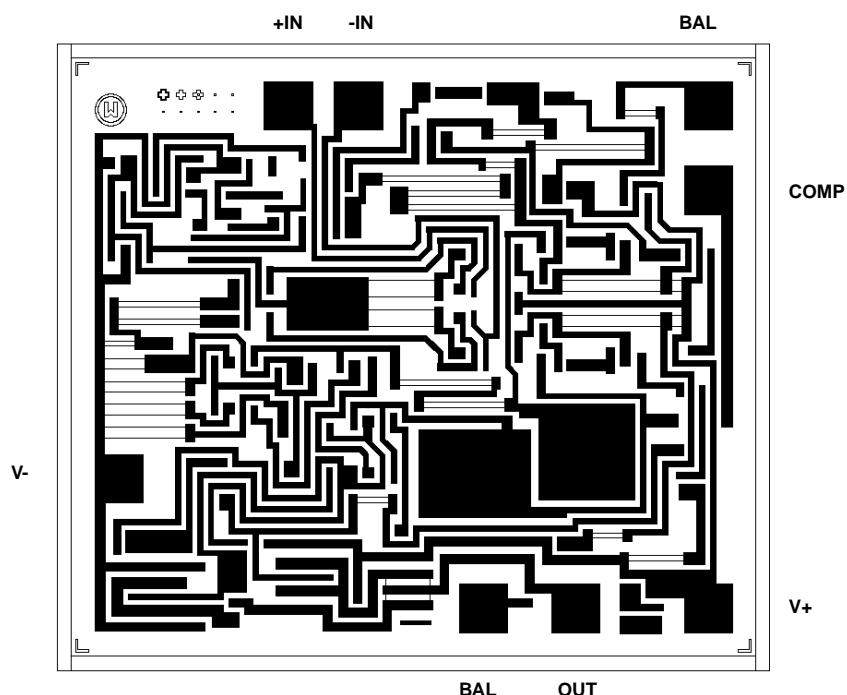
40

PROCESS:

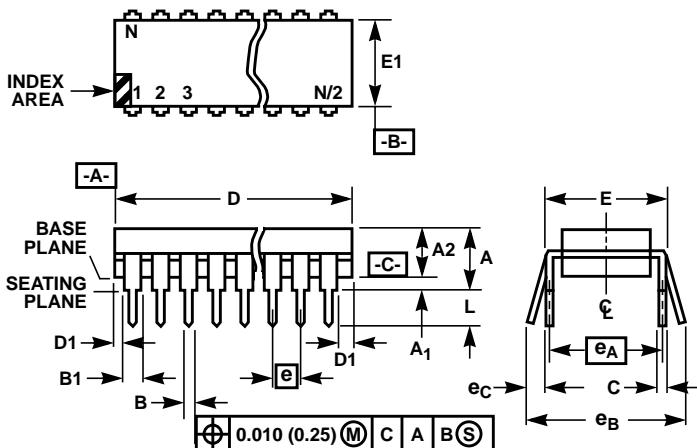
Bipolar Dielectric Isolation

Metalization Mask Layout

HA-2505



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum [-C-].
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusée
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029