4.5V to 18V, 3A 1ch Synchronous Buck Converter

BD86123AEFJ

●Description

The BD86123AEFJ is synchronous buck converters. The device integrates power MOSFETS that provide a each maximums current output current continuous load current over a wide operating input voltage of 4.5V to 18V.

Current mode operation provides fast transient response and easy phase compensation.

The output power MOSFETs using P-type MOSEFT (HI side) and N-type MOSEFT (LOW side), then this device don't need boot capacitor.

The BD86123AEFJ is HTSOP-J8 standard packages.

●Applications

- LCD TVs
- Set top boxes
- DVD/Blu-ray players/recorders
- Broadband Network and Communication Interface
- Amusement, other

●Features

- Input voltage range: 4.5V to 18.0V
- Reference voltage 0.8V ± 1%
- Average output Current: 3A(Max.)
- Switching frequency: 550kHz(Typ.)
- Pch FET ON resistance: 90mΩ(Typ.)
- Nch FET ON resistance: 50mΩ(Typ.)
- Standby current: 1μA (Typ.)
- Operating temperature range: -40℃ to +85℃
- Cycle by cycle over current protection(OCP)
- Thermal shutdown (TSD)
- Under voltage lock out(UVLO)
- Short circuit protection(SCP)
- Over voltage protection(OVP)
- Fixed soft start 5msec

●Package

	W(Typ.) x D(Typ.) x H(Max.)
HTSOP-J8	4.90mm x 6.00mm x 1.00mm

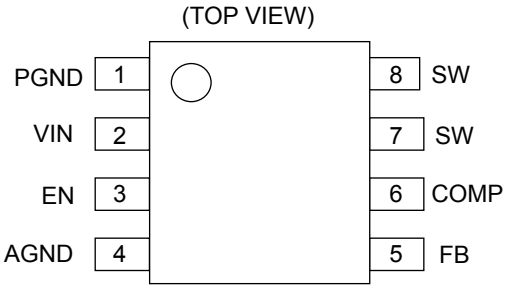


Figure 2. Pin configuration

●Typical Application

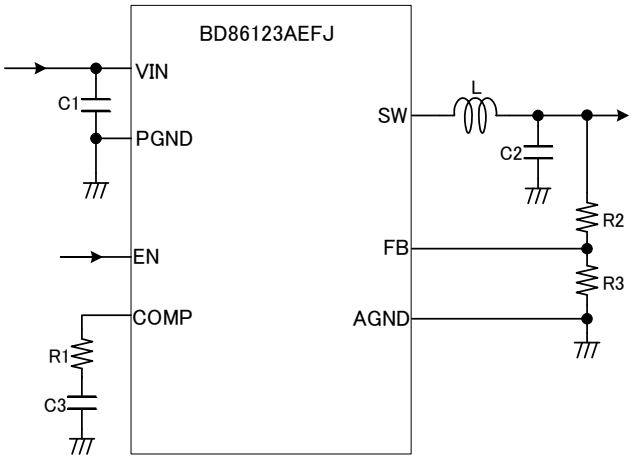


Figure 1. Application Circuit

●Block Diagram

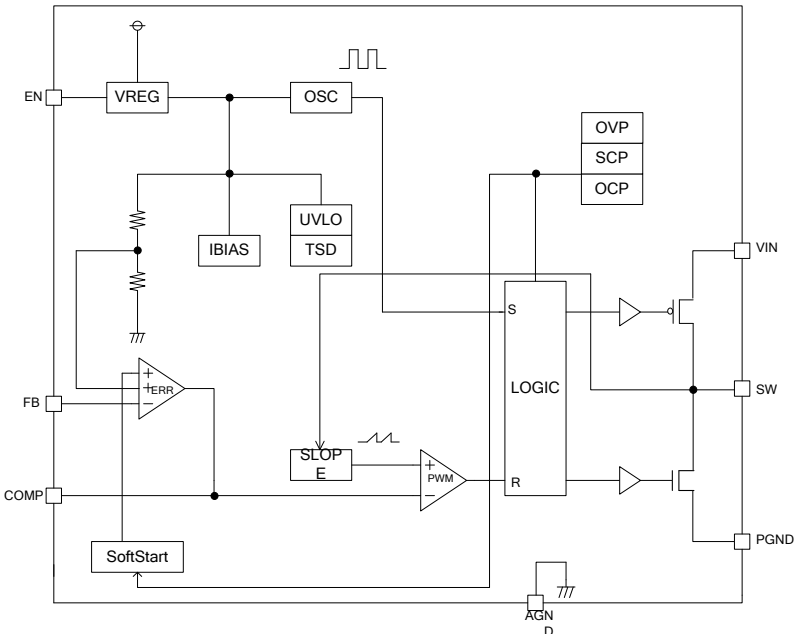


Figure 3. Block diagram

●Pin Description

No.	Symbol	Description
1	PGND	Power Ground pin. Power ground return for switching circuit.
2	VIN	Input voltage supply pin.
3	EN	Enable input control. Active high.
4	AGND	Analog Ground pin. Electrically needs to be connected to PGND.
5	FB	Converter feedback input. Connect to output voltage with feedback resistor divider.
6	COMP	Error amplifier output, and input to the output switch current comparator. External loop compensation pin.
7	SW	Switch node connection between high-side Pch FET and Low-side Nch FET.
8	SW	Switch node connection between high-side Pch FET and Low-side Nch FET.
Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to AGND.

●**Absolute maximum ratings** (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Condition
Input supply voltage	V_{IN}	20	V	
SW terminal voltage	V_{SW}	20	V	
EN terminal voltage	V_{EN}	20	V	
Power dissipation	Pd	3760*	mW	70mm×70mm, thickness 1.6mm, and 4 layer glass epoxy substrates
Operating temperature	Topr	-40～+85	℃	
Storage temperature	Tstg	-55～+150	℃	
Maximum Junction temperature	Tjmax	150	℃	
FB, COMP terminal voltage	V_{LVPINS}	7	V	

* Operating at higher than Ta=25℃, 30.08mW shall be reduced per 1℃

●**Operating conditions**

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Input supply voltage	V_{IN}	4.5	-	18.0	V
Output current	I_{OUT}	-	-	5.0	A
Output voltage range	V_{RANGE}	$V_{IN} \times 0.08^{*}$	-	V_{IN}×0.8	V

* $V_{IN} \times 0.08 \geqq 0.8$ [V]

●Electrical characteristics

(Unless otherwise noted Ta=25℃, V_{IN}=12V, V_{EN} = 3V)

Parameter	Symbol	Limits			UNIT	Condition
		Min.	Typ.	Max.		
V_{IN} supply current (operating)	I_{Q_active}	-	1.5	2.5	mA	V_{FB}= 0.75V, V_{EN}= 5V
V_{IN} supply current (standby)	I_{Q_stby}	-	1.0	10.0	μA	V_{EN} = 0V
Reference voltage (VREF)	V_{FB}	0.792	0.800	0.808	V	FB-COMP Short (Voltage follower)
FB input bias current	I_{FB}	-	0	2	μA	
Oscillation frequency	f_{OSC}	500	550	600	kHz	
High side FET ON resistance	R_{ONH}	-	90	-	mΩ	V_{IN}= 12V , I_{SW} = -1A
Low side FET ON resistance	R_{ONL}	-	50	-	mΩ	V_{IN}= 12V , I_{SW} = -1A
SW leak current	I_{LSW}	-	0	5	μA	V_{IN}= 18V , V_{SW} = 18V
Switch Current Limit	I_{LIMIT}	3.7	-	-	A	
Min duty	Min_duty	-	-	8	%	
UVLO voltage	V_{UVLO}	3.8	4.1	4.4	V	V_{IN} Sweep up
UVLO hysteresis	$V_{UVLOHYS}$	-	0.3	-	V	
EN terminal H threshold voltage	V_{ENH}	2.0	-	-	V	
EN terminal L threshold voltage	V_{ENL}	-	-	0.8	V	
Soft Start Time	T_{SS}	3.0	5.0	7.0	msec	

- V_{FB} :FB terminal voltage, V_{EN} :EN terminal voltage,
- Current capability should not exceed Pd.

●Typical Performance Curves (Reference data)

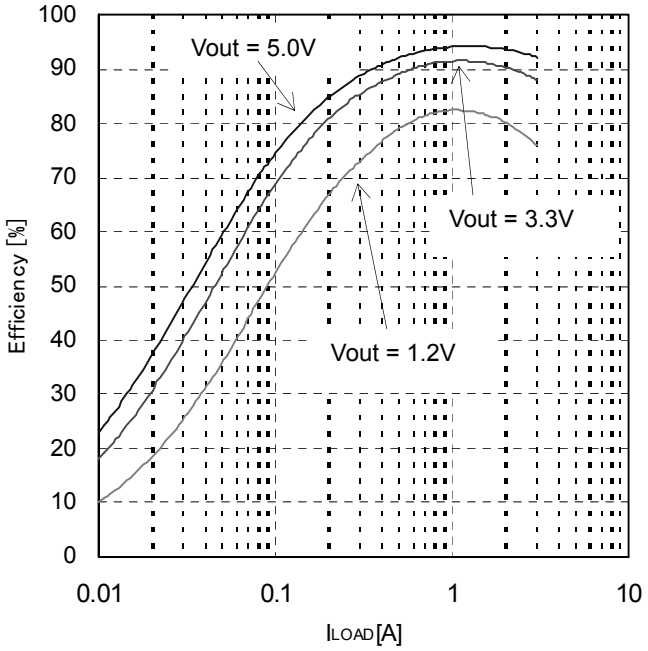


Figure 4. Efficiency
(VIN=12V, L=3.3/4.7/4.7μH(Vout=1.2/3.3/5.0V), Cout=44μF)

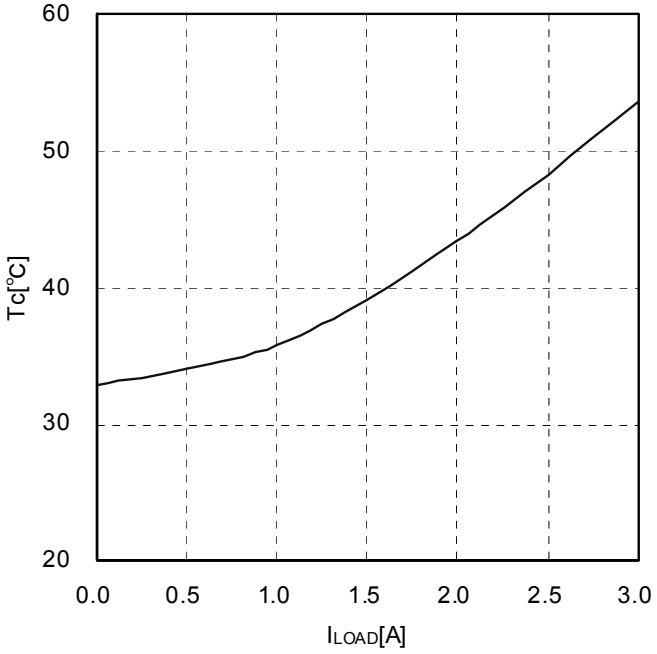
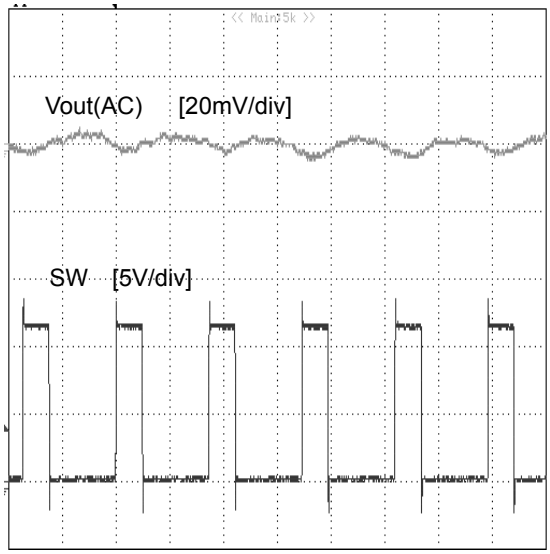
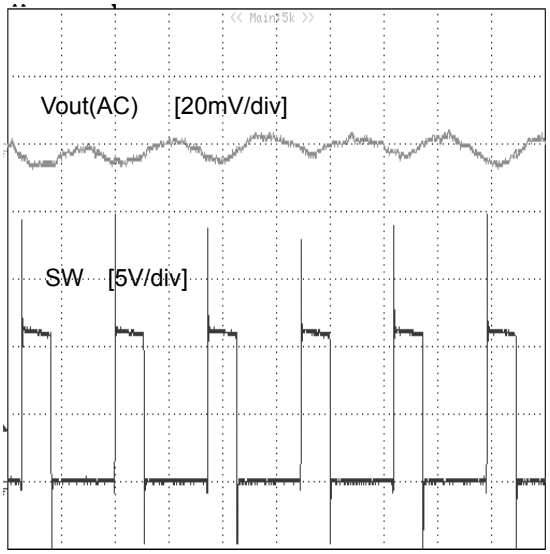


Figure 5. T_C-I_{LOAD}
(VIN=12V, Vout=3.3V, L=4.7μH, Cout=44μF)



T - Time - 1μsec/div

Figure 6. Vout Ripple
(VIN=12V, Vout=3.3V, L=4.7μH, Cout=44μF, Iout=0A)



T - Time - 1μsec/div

Figure 7. Vout Ripple
(VIN=12V, Vout=3.3V, L=4.7μH, Cout=44μF, Iout=3A)

●Typical Performance Curves (Reference data) (continued)

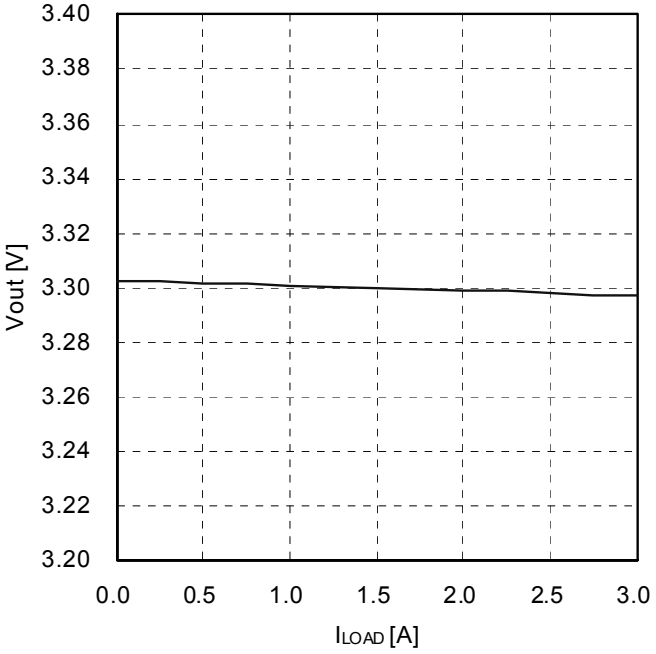


Figure 8. Load regulation
(VIN=12V, Vout=3.3V, L=4.7μH, Cout=44μF)

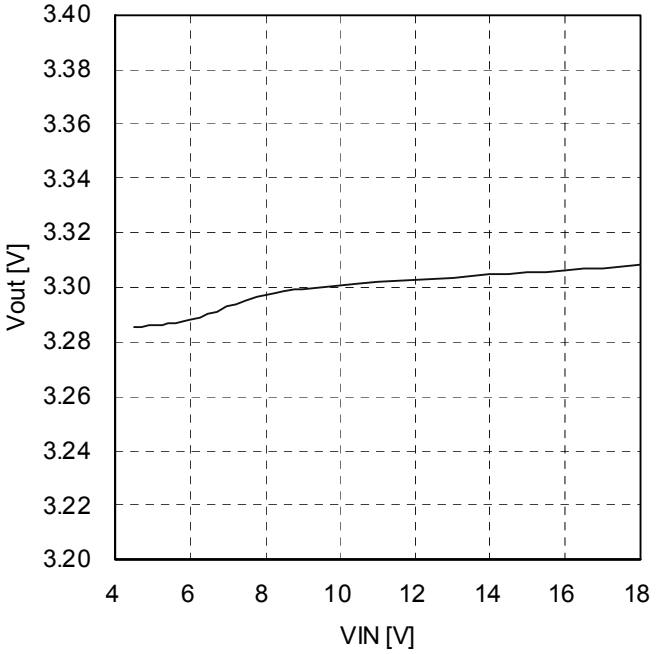


Figure 9. Line regulation
(Vout=3.3V, L=4.7μH, Cout=44μF, Iout=0A)

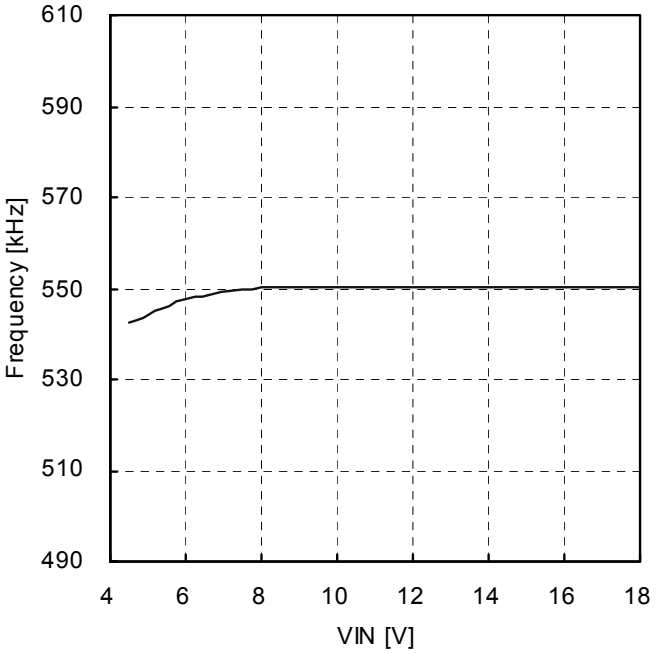


Figure 10. Frequency
(Vout=3.3V, L=4.7μH, Cout=44μF, Iout=0A)

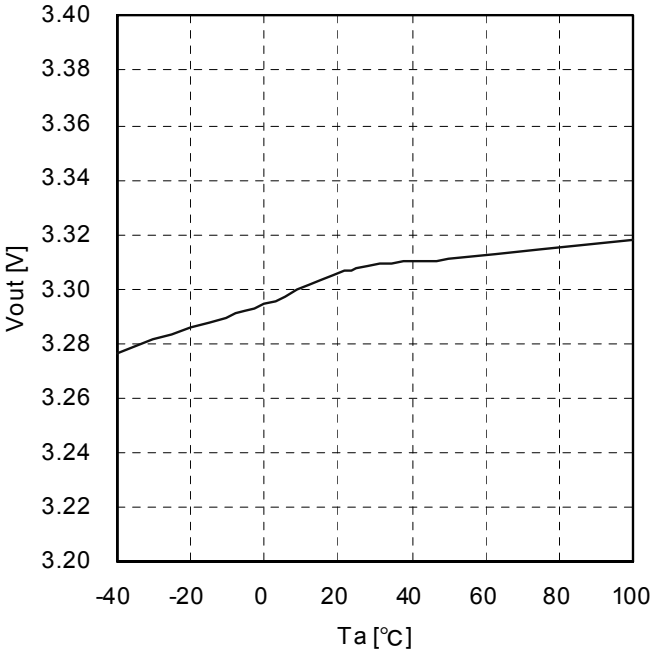
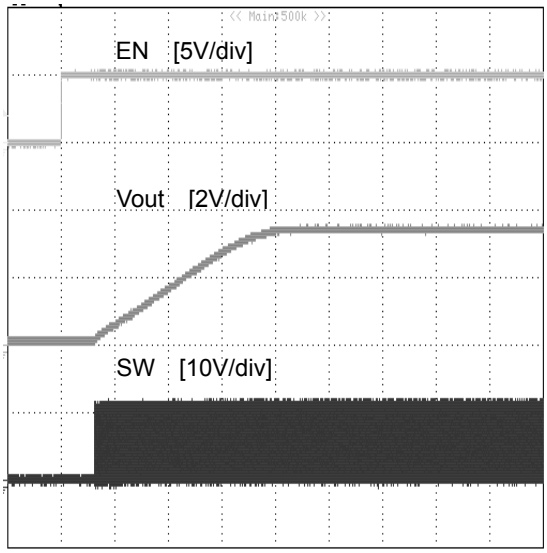


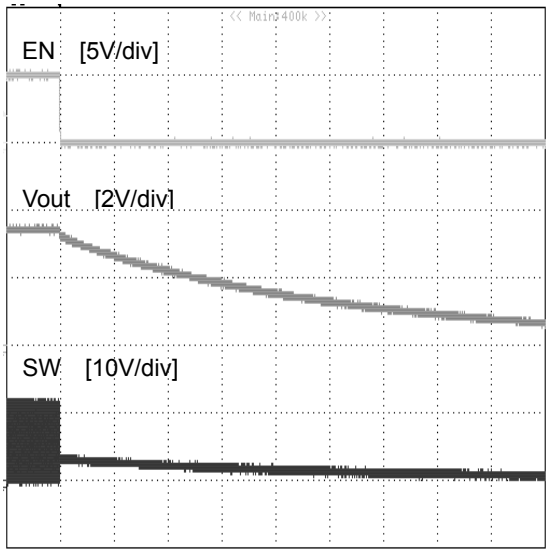
Figure 11. Vout-Temperature
(Vin=12V, Vout=3.3V, L=4.7μH, Cout=44μF, Iout=0A)

●Typical Performance Curves (Reference data) (continued)



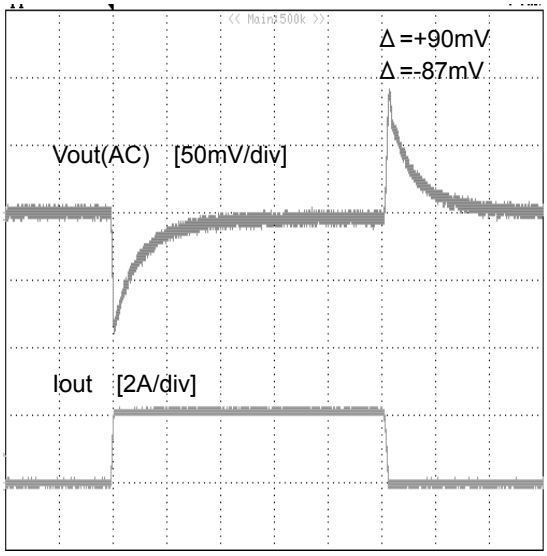
T - Time – 1msec/div

Figure 12. Start up wave form
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)



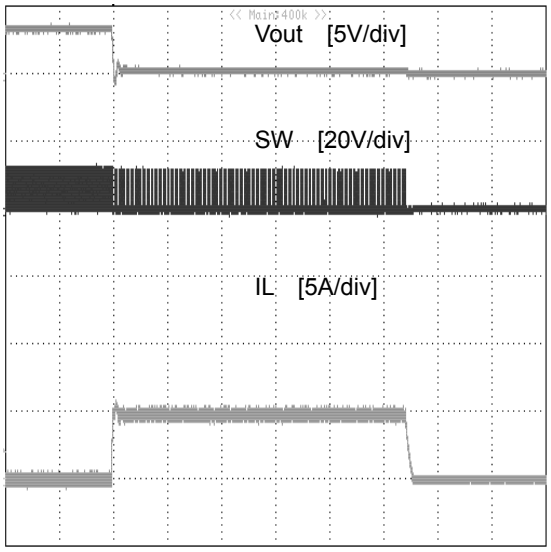
T - Time – 200msec/div

Figure 13. Off wave form
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)



T - Time - 100µsec/div

Figure 14. Transient response
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=2A)



T - Time - 200µsec/div

Figure 15. OCP function
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Vout is short to GND)

●Functional descriptions

1 Enable control

The device can be controlled ON/OFF by EN terminal voltage.
An internal circuit starts when VEN reaches 2.0V.
When standing up of VIN is too steep (1msec or less), a defective start might be caused according to the state of Pascon between GND substrate pattern and power supply-when the terminal EN is short-circuited to the terminal VIN and it is used.

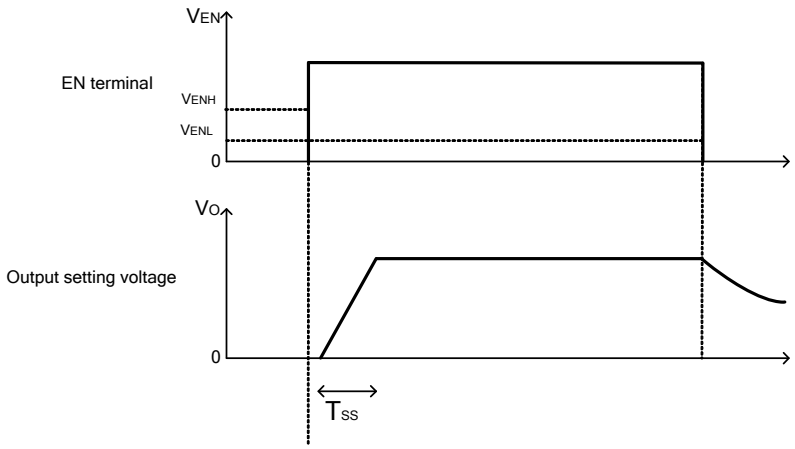


Figure 16. ON/OFF transition wave form in EN controlling

2 Protection function

Protection circuit is effective for destruction prevention due to accident so that avoid using under continuous protection operation.

2-1 Short Circuit protection function (SCP)

The FB terminal voltage is compared with internal reference voltage VREF.
If FB terminal voltage falls below V_{SCP} (= VREF - 240mV) and the state continues, output changes to low voltage and the state is fixed.
During soft start, the FB terminal voltage is compared with internal soft start slope

Table 1. output short circuit protection function

EN terminal	FB terminal	Short Circuit Protection function	Short Circuit Protection operation
$>V_{ENH}$	$<V_{SCP}$	Effective	ON
	$>V_{SCP}$		OFF
$<V_{ENL}$	-	Invalidity	OFF

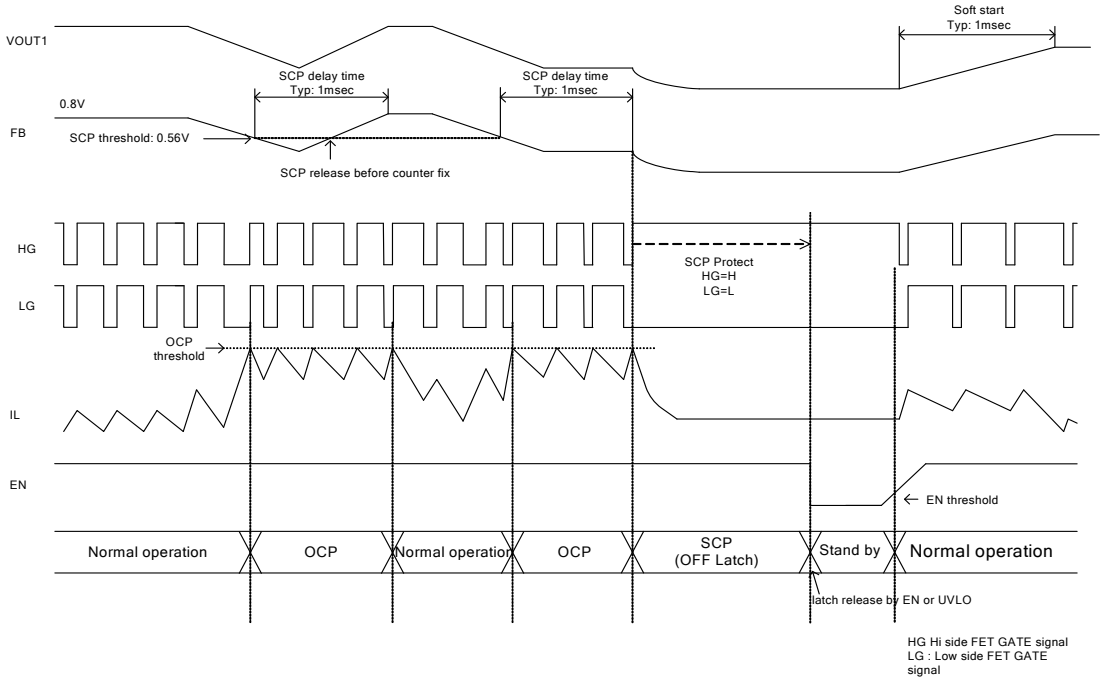


Figure 17. SCP Timing chart

2-2 Over voltage protection function (OVP)

Output over Voltage Protection is activated when FB voltage rises to or above V_{OVP} (= VREF + 240mV) and the state continues, output changes to low voltage and the state is fixed.

Table 2. output over voltage protection function

EN terminal	FB terminal	Short Circuit Protection function	Short Circuit Protection operation
$>V_{ENH}$	$>V_{OVP}$	Effective	ON
	$<V_{OVP}$		OFF
$<V_{ENL}$	-	Invalidity	OFF

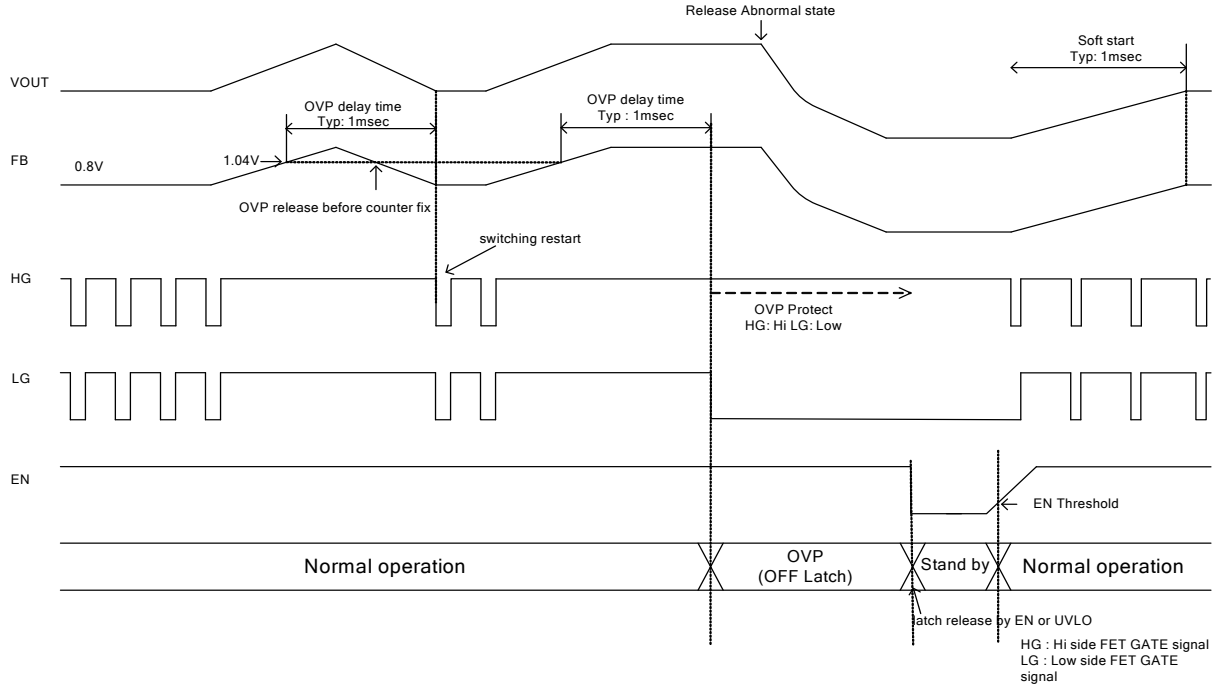


Figure 18. OVP Timing chart

2-3 Under voltage lock out protection (UVLO)

Under voltage lock out protection monitors the VIN terminal voltage.
When the VIN terminal voltage is lower than 3.8V (typ), the device state changes to the standby mode.
When the VIN terminal voltage is higher than 4.1V (typ), the device starts operation.

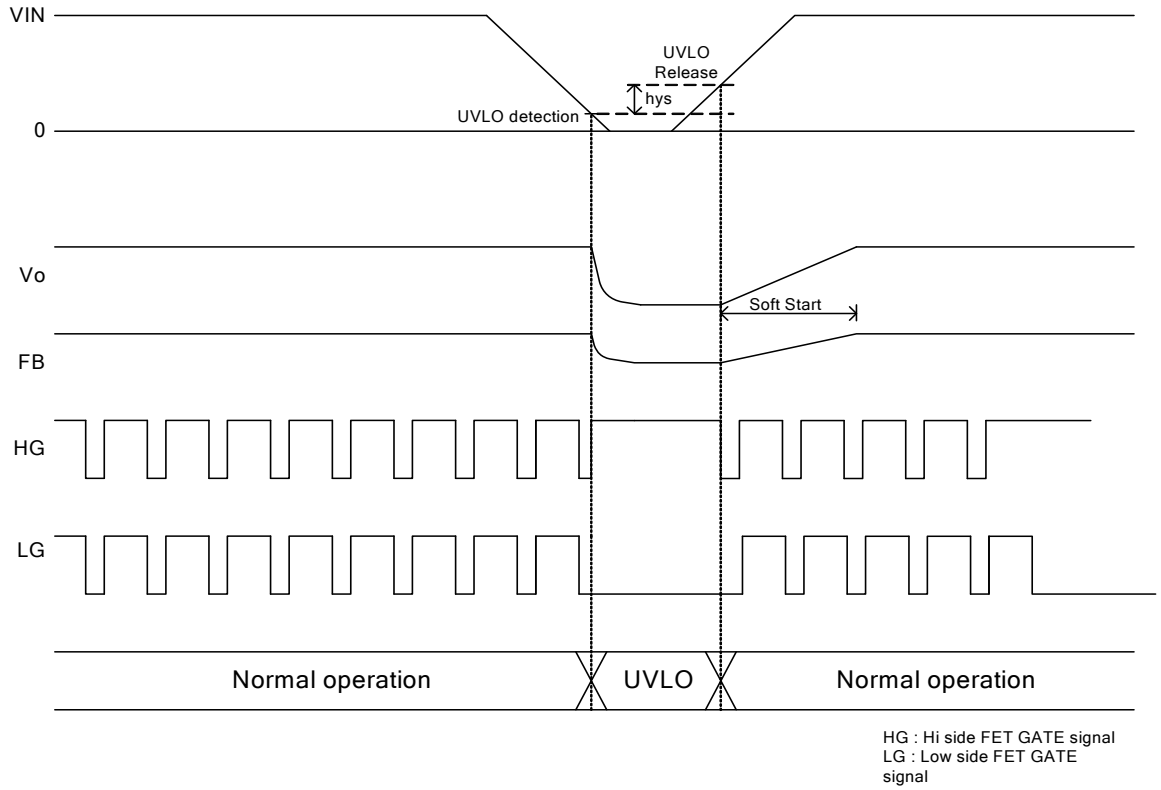


Figure 19. UVLO Timing chart

2-4 Thermal shut down function

BD86123A monitors the temperature of itself. When the temperature of the chip exceeds Tj=175, the DC/DC converter is fixed in a low voltage.
TSD function is aimed to shut down IC from thermal reckless driving under an abnormal state to exceed Tjmax=150.
It aims at neither protection nor the guarantee of the set. Therefore, please do not use this function to protect the set.

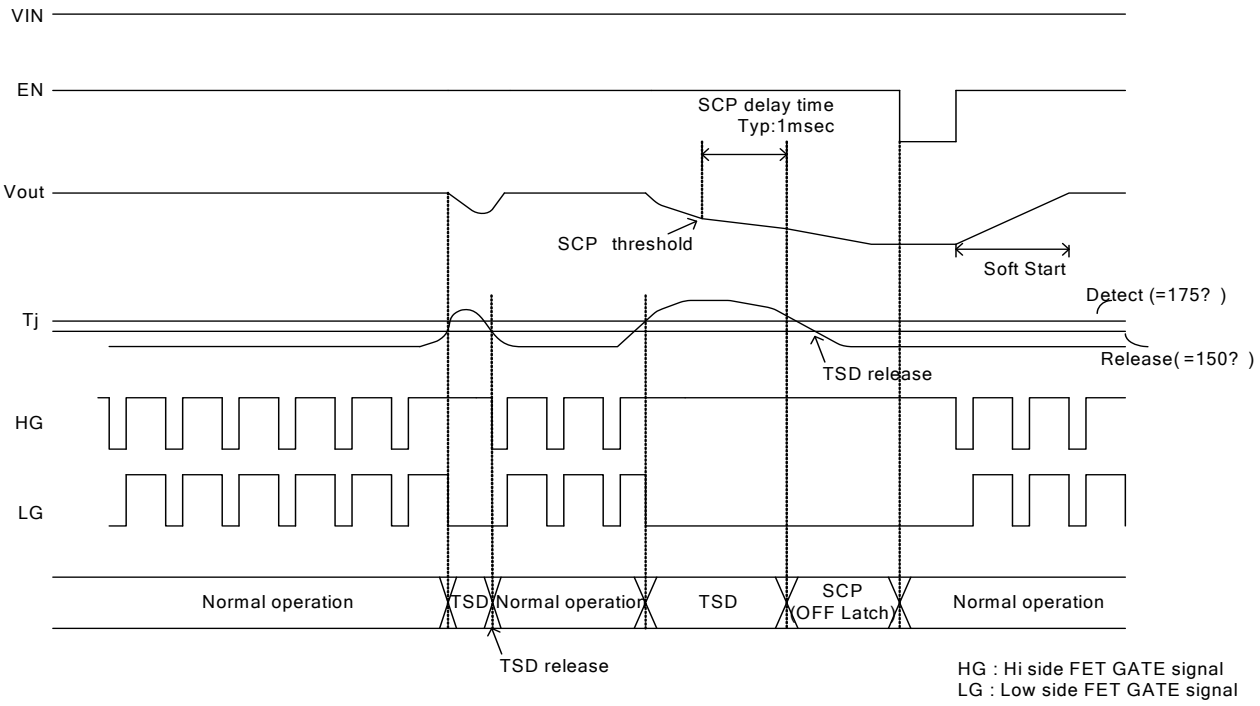


Figure 20. TSD Timing chart

2-5 Over current protection function

The over current protection function has been achieved by limiting the current that flows on high side MOSFET. Output current is limited by cycle-by-cycle. When an abnormal state continues, the output is fixed in a low level.

2-6 Error detection (off latch) release method

BD86123A enters the state of off latch when the protection function operates.
To release the off latch state, the VIN terminal voltage should be changed to less than UVLO level (=3.8V [typ]) or, the EN terminal voltage falls below V_{ENL}.voltage.

●Application Example(s)

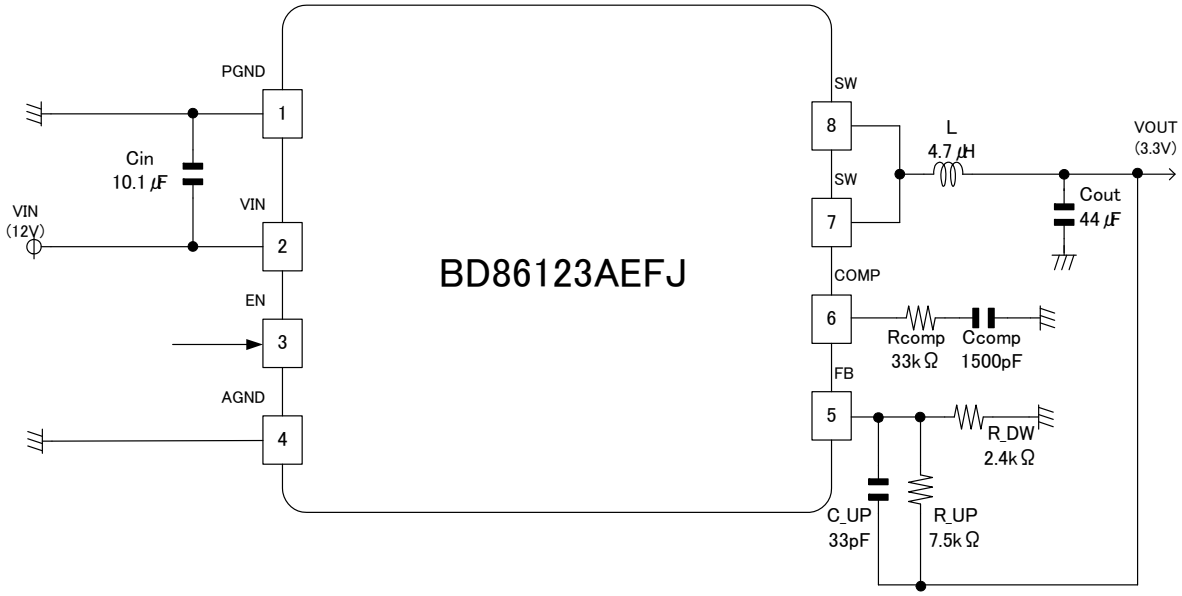


Figure 21. Application circuit

However, the best values of Application Components are different between applications.
please confirm actual application and decide values finally.

		Maker	**Part No**
Input capacitor(Cin)	10μF/25V + 0.1μF/50V	TDK	C3225JB1E106K + C1608JB1H104K
Output capacitor(Cout)	22μF/16V × 2	TDK	C3216JB1C226M × 2
Inductor (L)	4.7μH	TDK	SPM6530-4R7

	FB	
Vo(V)	R_UP [kΩ]	R_DW [kΩ]
5	4.3	0.82
3.3	7.5	2.4
1.8	15	12
1.5	16	18
1.2	10	20
1	5.1	20

●How to select parts of application

(1) Output LC filter constant selection

The Output LC filter is required to supply constant current to the output load.
A larger value inductance at this filter results in less inductor ripple current(ΔI_L) and less output ripple voltage. However, the larger value inductors tend to have less fast load transient-response, a larger physical size, a lower saturation current and higher series resistance. A smaller value inductance has almost opposite characteristics above.
So Choosing the Inductor ripple current(ΔI_L) between 20 to 40% of the averaged inductor current (equivalent to the output load current) is a good compromise.

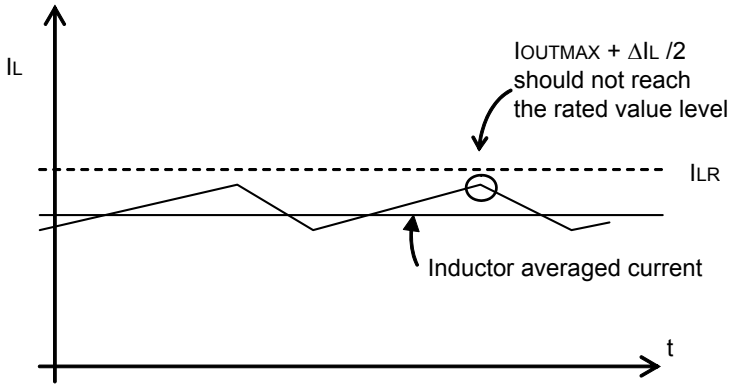


Figure 22.

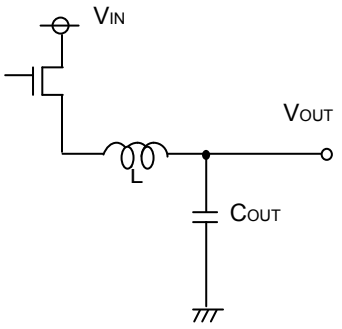


Figure 23.

Setting ΔI_L = 30% x Averaged Inductor current (3A) = 0.9 [A]、

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 4.83\mu\,[H] \fallingdotseq 4.7\mu\,[H]$$

Where V_{IN}= 12V, V_{OUT}= 3.3V, F_{OSC}= 550 kHz,
; F_{OSC} is a switching frequency

Also the inductor should have the higher saturation current than $I_{OUTMAX} + \Delta I_L / 2$.

The output capacitor C_{OUT} affects the output ripple-voltage. Choose the large capacitor to achieve the small ripple-voltage enough to meet the application requirement.

Output ripple voltage ΔV_{RPL} is calculated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}} \right) \quad [V]$$

Where R_{ESR} is a parasitic series resistance in output capacitor.

Setting C_{OUT} = 44µF, R_{ESR} = 10mΩ
ΔV_{RPL} = 0.9 × (10m + 1 / (8 × 44µ × 550k)) = 13.6mV

(2) Design of Feedback Resistance constant

Set the feedback resistance as shown below.

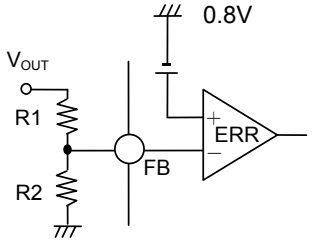


Figure 24.

$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.8 \quad [V]$$

(3)Loop Compensation

Choosing compensation capacitor C_{CMP} and resistor R_{CMP}

The current-mode buck converter has 2-poles and 1-zero system. Choosing the compensation resistor and capacitor is important for a good load-transient response and good stability.
The example of DC/DC converter application bode plot is shown below.

The compensation resistor R_{CMP} will decides the cross over frequency F_{CRS} (the frequency that the total DC-DC loop-gain falls to 0dB).
Setting the higher cross over frequency achieves good response speed, however less stability. While setting the lower cross over frequency shows good stability but worse response speed.
The 1/10 of switching frequency for the cross over frequency shows a good performance at most applications.

(i) Choosing phase compensation resistor R_{CMP}
The compensation resistor R_{CMP} can be on following formula.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} \quad [\Omega]$$

Where
V_{OUT} ; Output voltage, **F_{CRS}** ; Cross over frequency, **C_{OUT}** ; Output Capacitor,
V_{FB} ; internal feedback voltage (**0.8V(TYP)**),
G_{MP} ; Current Sense Gain (**4.3A/V(TYP)**) , **G_{MA}** ; Error Amplifier Trans-conductance (**400μA/V(TYP)**)

Setting V_{OUT}= 3.3V, F_{CRS}= 55kHz, C_{OUT}= 44μF、

$$R_{CMP} = \frac{2\pi \times 3.3 \times 55k \times 44\mu}{0.8 \times 4.3 \times 400\mu} = 37.3k \fallingdotseq 33k \quad [\Omega]$$

(ii) Choosing phase compensation capacitor C_{CMP}
For the stability of DC/DC converter, canceling the phase delay that derives from output capacitor C_{OUT} and resistive load R_{OUT} by inserting the phase advance.
The phase advance can be added by the zero on compensation resistor R_{CMP} and capacitor C_{CMP}.
Making Fz= F_{CRS} / 6 gives a first-order estimate of C_{CMP}.

$$\text{Compensation Capacitor} \quad C_{CMP} = \frac{Vout \times Cout}{Iout \times R_{CMP}} \quad [F]$$

$$\text{Compensation Capacitor} \quad C_{CMP} = \frac{3.3 \times 44\mu}{3 \times 33k} = 1.47n \fallingdotseq 1.5n \quad [F]$$

However, the best values of zero and F_{CRS} are different between applications. After calculation above formula and confirmation actual application, please decide values finally.

(iii) The condition of the loop compensation stability
The stability of DC/DC converter is important. To secure the operating stability, please check the loop compensation has the enough phase-margin. For the condition of loop compensation stability, the phase-delay must be less than 150 degree where Gain is 0 dB.
Feed forward capacitor C_{RUP} boosts phase margin over a limited frequency range and is sometimes used to improve loop response. C_{RUP} will be more effective if R_{UP} >> R_{UP}||R_{DW}

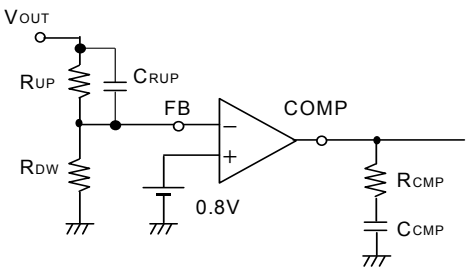


Figure 25.

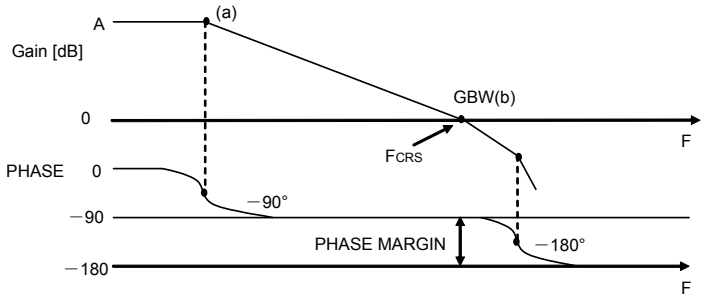


Figure 26.

●**I/O equivalence circuit**(s)

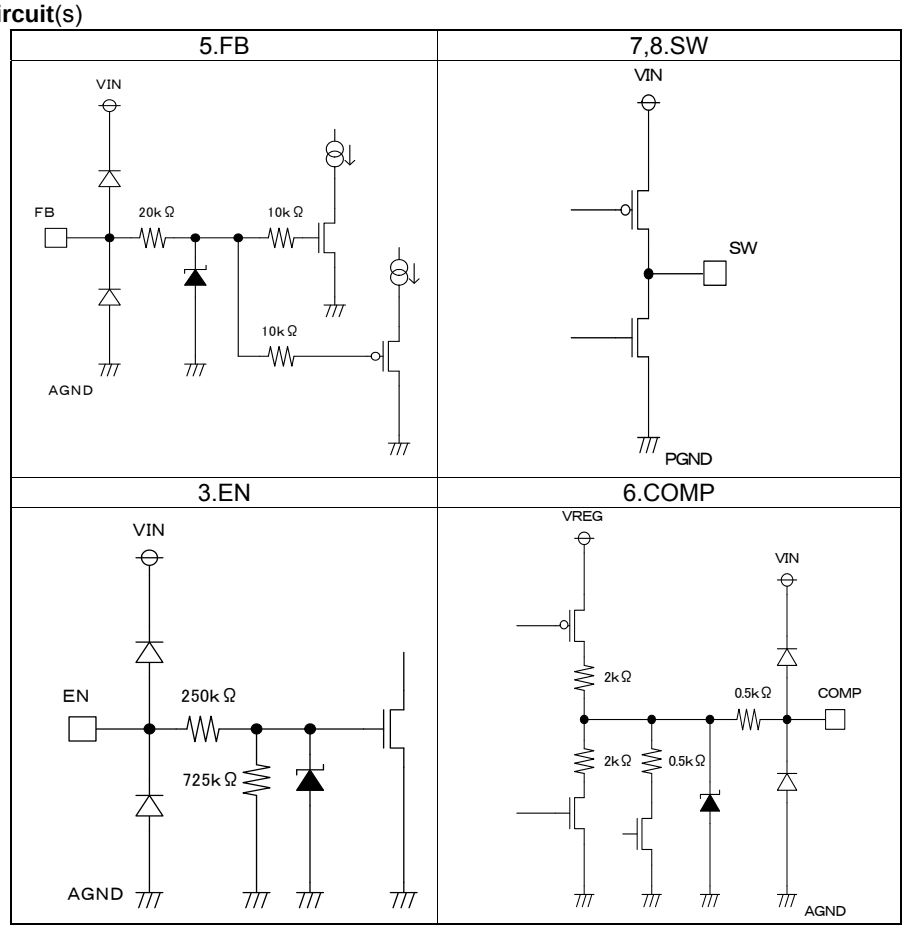


Figure 27.

●**Notes for use**

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when the resistors and transistors are connected to the pins as shown in Figure 26. , a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

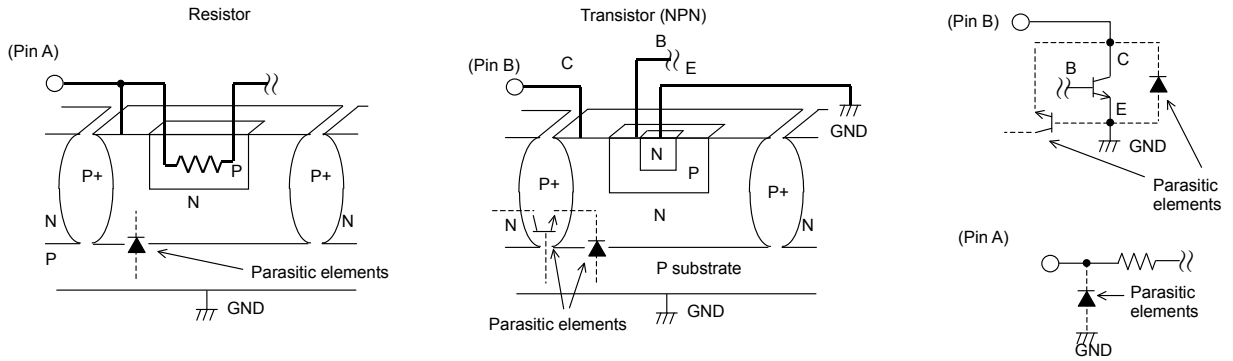


Figure 28. Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits

An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)

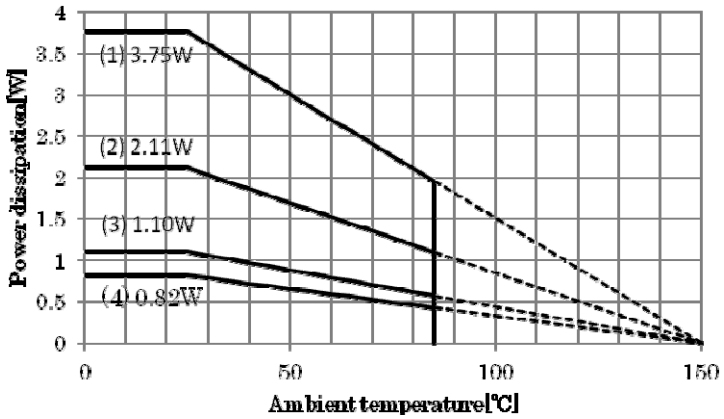
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the
IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) EN control speed

Chattering happens if standing lowering speed is slow when standing of EN pin is lowered.
The reverse current in which the input side and the pressure operation are done from the output side is generated when chattering operates with the output voltage remained, and there is a case to destruction.
Please set to stand within 100μs when you control ON/OFF by the EN signal.

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

●**Power Dissipation**



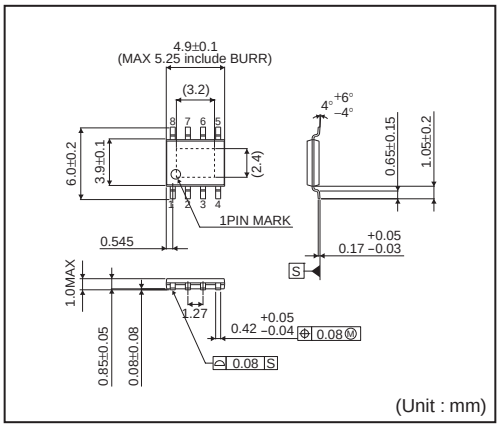
HTSOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm× 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

●Ordering Information

B D 8 6 1 2 3 A E F J	-	E 2
Part Number		Packaging and forming specification E2: Embossed tape and reel
	Package EFJ: HTSOP-J8	

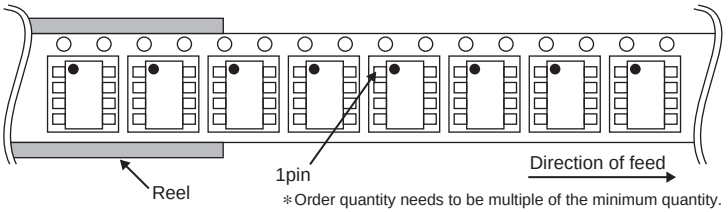
●Physical Dimension Tape and Reel Information

HTSOP-J8



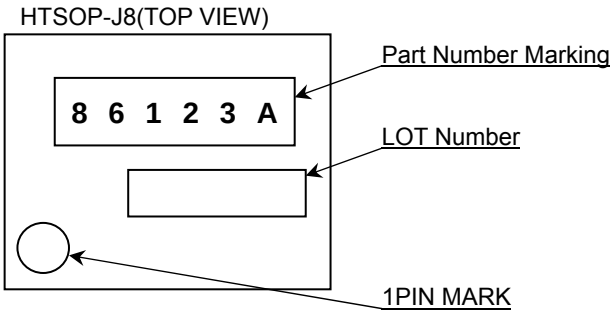
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram(s)(TOP VIEW)



●History

Date	Revision	Changes
04.Sep.2012	001	New Release