

TYPES SN54H78, SN54L78, SN54LS78A, SN74H78, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'H78 and 'L78 contain two J-K flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The 'H78 and 'L78 are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

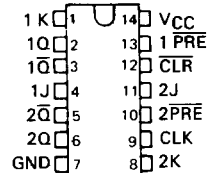
The 'LS78A contain two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and K inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN54H78, SN54L78, and the SN54LS78A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74H78 and the SN74LS78A are characterized for operation from 0°C to 70°C.

FOR CHIP CARRIER INFORMATION,
CONTACT THE FACTORY

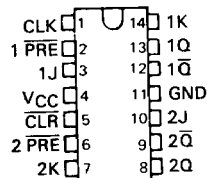
SN54H78 ... J PACKAGE
SN74H78 ... J OR N PACKAGE

(TOP VIEW)



SN54L78 ... J PACKAGE
SN54LS78A ... J OR W PACKAGE
SN74LS78A ... D, J OR N PACKAGE

(TOP VIEW)



'H78, 'L78
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	

'LS78A

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	Q̄ ₀

† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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TTL DEVICES

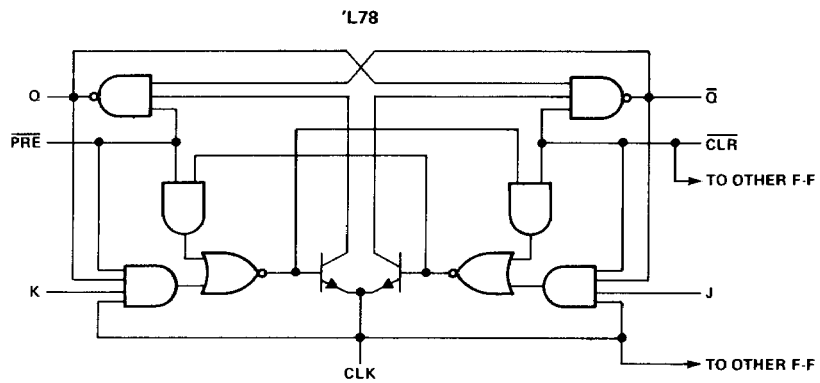
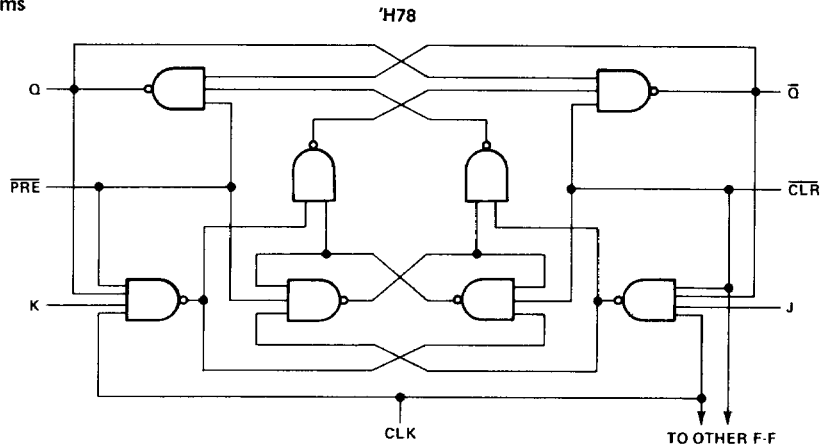
PRODUCTION DATA
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TYPES SN54H78, SN54L78, SN74H78
DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

logic diagrams



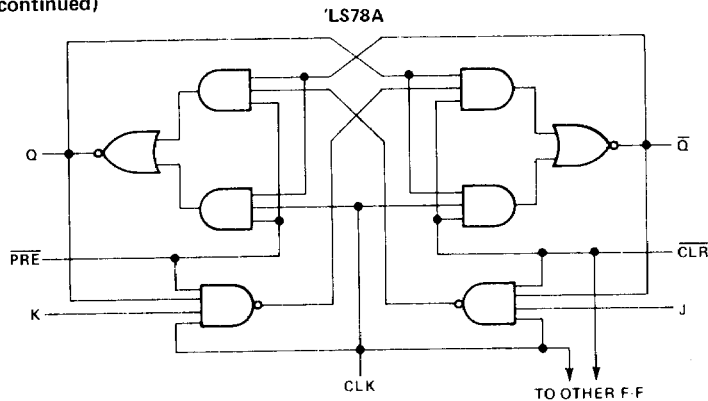
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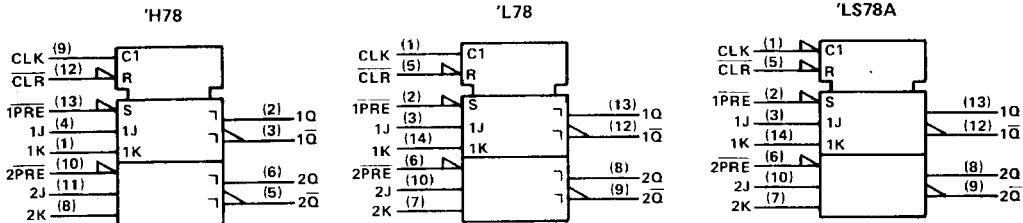
TYPES SN54H78, SN54L78, SN54LS78A,
SN74H78, SN74LS78A

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

logic diagrams (continued)

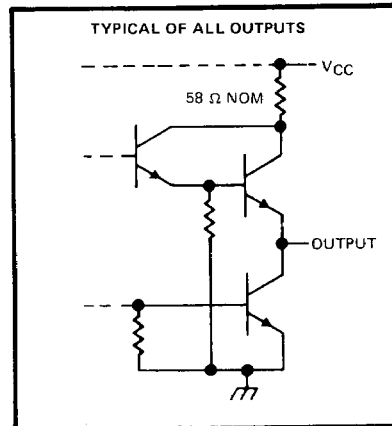
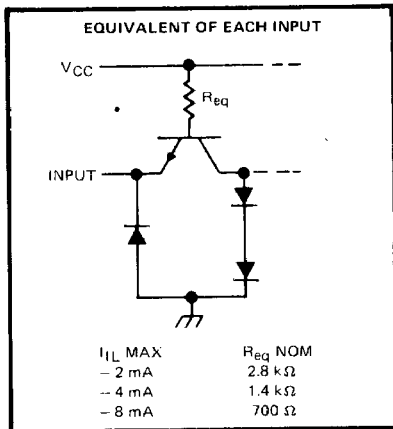


logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs

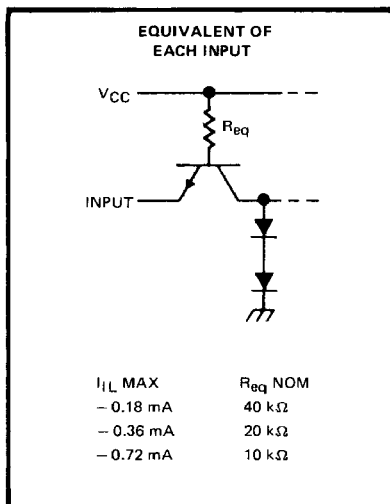


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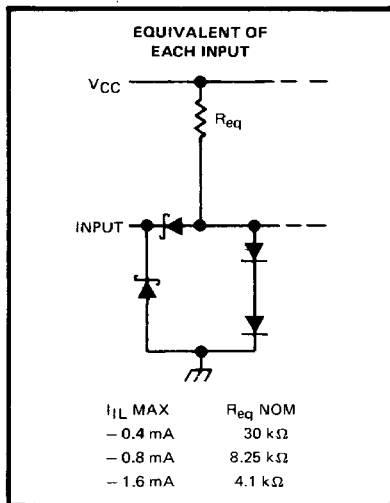
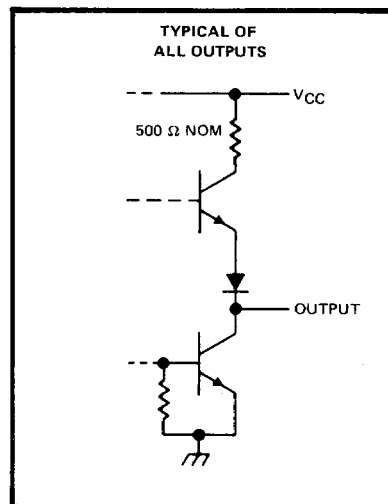
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**TYPE SN54H78, SN54L78, SN54LS78A,
SN74H78, SN74L78, SN74LS78A
DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR**

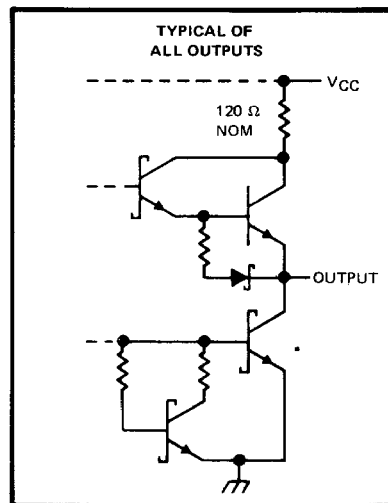
schematics of inputs and outputs (continued)



'L78



'LS78A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'H78, 'L78	5.5 V
'LS78A	7 V
Operating free-air temperature range: SN54'	- 55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54H78, SN74H78

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

			SN54H78			SN74H78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		− 0.5			− 0.5			mA
I _{OL}	Low-level output current		20			20			mA
t _w	Pulse duration	CLK high	12			12			ns
		CLK low	28			28			
		CLR or PRE low	16			16			
t _{su}	Setup time before CLK †		0			0			ns
t _h	Hold time-data after CLK †		0			0			ns
T _A	Operating free-air temperature		− 55 125			0 70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54H78		SN74H78		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
V _{IK}		V _{CC} = MIN, I _I = - 8 mA			- 1.5		- 1.5		V
V _{OH}		V _{CC} = MIN, I _{OH} = - 0.5 mA	V _{IH} = 2 V, V _{IL} = 0.8 V,	2.4 3.4		2.4 3.4		V	
V _{OL}		V _{CC} = MIN, I _{OL} = 20 mA	V _{IH} = 2 V, V _{IL} = 0.8 V,	0.2 0.4		0.2 0.4		V	
I _I		V _{CC} = MAX, V _I = 5.5 V			1		1		mA
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.4 V			50		50		μA
	CLR				200		200		
	PRE or CLK				100		100		
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V			- 2		- 2		mA
	CLR★				- 8		- 8		
	PRE★				- 4		- 4		
	CLK				- 4		- 4		
I _{OS} §		V _{CC} = MAX			- 40	- 100	- 40	- 100	mA
I _{CC}		V _{CC} = MAX, See Note 2			16	25	16	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than output should be shorted at a time, and the duration of the short circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{max}			$R_L = 280\ \Omega, \quad C_L = 25\ \text{pF}$	25	30		MHz
t_{PLH}	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$	Q or $\overline{\text{Q}}$		6	13		ns
t_{PHL}				12	24		ns
t_{PLH}				CLK	Q or $\overline{\text{Q}}$	14	21
t_{PHL}	22	27					ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage	Clock input		0.6	V
		All other inputs		0.7	
I _{OH}	High-level output current			-0.1	mA
I _{OL}	Low-level output current			2	mA
t _w	Pulse duration	CLK high or low		200	ns
		CLR or PRE low		100	
t _{su}	Setup time before CLK ↑		0		ns
t _h	Hold time-data after CLK ↓		0		ns
T _A	Operating free-air temperature	-55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.1 mA			2.4	3.3		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 2 mA				0.15		V
I _I	J or K	V _{CC} = MAX, V _I = 5.5 V					0.1	mA
	PRE						0.2	
	CLK or CLR						0.4	
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.4 V					10	μA
	CLR						40	
	PRE						20	
	CLK						400	
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.3 V					-0.18	mA
	PRE						-0.36	
	CLK or CLR						-0.72	
I _{OS}		V _{CC} = MAX			-3		-15	mA
I _{CC}		V _{CC} = MAX, See Note 2				0.76	1.44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.switching characteristics, V_{CC} = 5 V, T_A = 25° C (see note 3)

PARAMETER	FROM {INPUT}	TO {OUTPUT}	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f _{max}			R _L = 4 kΩ, C _L = 50 pF	2.5	3		MHz	
t _{PLH}	PRE or CLR	Q or $\bar{Q}$			35	75	ns	
t _{PHL}	PRE or CLR (CLK high)	$\bar{Q}$ or Q			60	150	ns	
	PRE or CLR (CLK low)					200		
t _{PLH}	CLK	Q or $\bar{Q}$			10	35	75	ns
t _{PHL}					10	60	150	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54LS78A, SN74LS78A

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

recommended operating conditions

			SN54LS78A			SN74LS78A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
I _{OH}	High-level output current				-0.4			-0.4	mA
I _{OL}	Low-level output current				4			8	mA
f _{clock}	Clock frequency		0		30	0		30	MHz
t _w	Pulse duration	CLK high	20			20			ns
		PRE or CLR low	25			25			
t _{su}	Setup time before CLK ↓	data high or low	20			20			ns
		PRE or CLR inactive	20			20			
t _h	Hold time-data after CLK ↓		0			0			ns
T _A	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS78A			SN74LS78A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.7 V, I _{OH} = -0.4 mA	2.5	3.4					V
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA				2.7	3.4		
V _{OL}		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA				0.35	0.5		
I _I	J or K	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
	CLR			0.6			0.6		
	PRE			0.3			0.3		
	CLK			0.8			0.8		
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V		20			20		μA
	CLR			120			120		
	PRE			60			60		
	CLK			160			160		
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
	CLR			-1.6			-1.6		
	PRE			-0.8			-0.8		
	CLK			-1.6			-1.6		
I _{OS} §		V _{CC} = MAX, See Note 4	-20		-100	-20		-100	mA
I _{CC}		V _{CC} = MAX, See Note 2		4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

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TYPES SN54LS78A, SN74LS78A

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{\max}$			$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$		30	45		MHz
t_{PLH}	$\overline{\text{PRE}}, \overline{\text{CLR}}$ or CLK	Q or $\overline{Q}$			15	20		ns
t_{PHL}					15	20		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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