19-4611; Rev 5; 5/09

Improved, Quad, SPST Analog Switches

General Description

Maxim's redesigned DG441/DG442 analog switches now feature on-resistance matching (4Ω max) between switches and guaranteed on-resistance flatness over the signal range (9Ω max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection (10pC max), low power consumption (1.65mW), and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers lower off-leakage current over temperature (less than 5nA at +85°C).

The DG441/DG442 are quad, single-pole/single-throw (SPST) analog switches. The DG441 has four normally closed switches, and the DG442 has four normally open switches. Switching times are less than 250ns for t_{ON} and less than 170ns for t_{OFF}. These devices operate from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Maxim's improved DG441/DG442 continue to be fabricated with a 44V silicon-gate process.

Applications

Sample-and-Hold Circuits
Communication Systems
Test Equipment
Battery-Operated Systems
Heads-Up Displays
Fax Machines
PBX, PABX
Guidance and Control Systems
Audio-Signal Routing
Military Radios
Modems

New Features

- **Plug-In Upgrades for Industry-Standard DG441/DG442**
- **Improved $r_{DS(ON)}$ Match Between Channels(4Ωmax)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (9Ωmax)**
- **Improved Charge Injection (10pC max)**
- **Improved Off-Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstand Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (85Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (1.65mW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Ordering Information

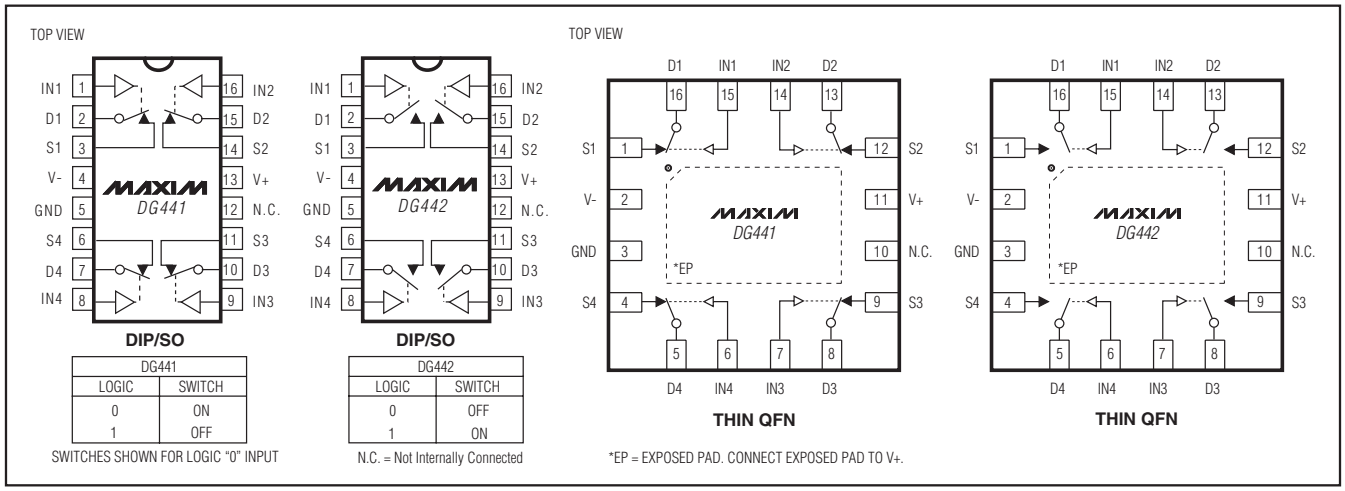
PART	TEMP RANGE	PIN-PACKAGE
DG441CJ	0°C to +70°C	16 Plastic DIP
DG441CY	0°C to +70°C	16 Narrow SO
DG441C/D	0°C to +70°C	Dice*
DG441DJ	-40°C to +85°C	16 Plastic DIP
DG441DY	-40°C to +85°C	16 Narrow SO

Ordering Information continued at end of data sheet.

Note: *Devices are available in both leaded and lead(Pb)-free packaging. Specify lead-free by adding the + symbol at the end of the part number when ordering.*

**Contact factory for dice specifications.*

Pin Configurations/Functional Diagrams/Truth Tables



Improved, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L .....(GND - 0.3V) to (V+ + 0.3V)
Digital Inputs, V_S, V_D (Note 1).....(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current, S or D
(pulsed at 1ms, 10% duty-cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Thin QFN (derate 20.8mW/°C above +70°C).....1667mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
DG441C/DG442C .....0°C to +70°C
DG441D, E/DG442D, E .....-40°C to +85°C
DG441AK, MY/DG442AK, MY .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_{GND} = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog-Signal Range	V_{ANALOG}	(Note 3)			-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = 8.5V or -8.5V	T_A = +25°C			50	85	Ω
			T_A = T_{MIN} to T_{MAX}				100	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 15V, V- = -15V, V_D = ±10V, I_S = -10mA	T_A = +25°C				4	Ω
			T_A = T_{MIN} to T_{MAX}				5	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, V_D = 5V or -5V, I_S = -10mA	T_A = +25°C				9	Ω
			T_A = T_{MIN} to T_{MAX}				15	
Source Off-Leakage Current (Note 5)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ∓15.5V, V_S = ±15.5V	T_A = +25°C		-0.50	0.01	0.50	nA
			T_A = T_{MAX}	C, D	-5		5	
				A	-20		20	
Drain Off-Leakage Current (Note 5)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ∓15.5V, V_S = ±15.5V	T_A = +25°C		-.0.50	0.01	0.50	nA
			T_A = T_{MAX}	C, D	-5		5	
				A	-20		20	
Drain On-Leakage Current (Note 5)	$I_{D(ON)}$ or $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	T_A = +25°C		-0.50	0.08	0.50	nA
			T_A = T_{MAX}	C, D	-10		10	
				A	-20		20	
DIGITAL								
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V			-500	0.01	500	nA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V			-500	0.01	500	nA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_{GND} = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SUPPLY							
Power-Supply Range	V+, V-			±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V			15	100	µA
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V		-100	-15		µA
DYNAMIC							
Turn-On Time	t_{ON}	V_S = ±10V, R_L = 1kΩ, Figure 2	T_A = +25°C		150	250	ns
Turn-Off Time	t_{OFF}	DG441, V_D = ±10V, Figure 2	T_A = +25°C		90	120	ns
		DG442, V_D = ±10V, Figure 2	T_A = +25°C		110	170	
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	T_A = +25°C		5	10	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		60		dB
Crosstalk (Note 7)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		-100		dB
Source Off-Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
Drain Off-Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
Drain On-Capacitance	$C_{D(ON)}$	f = 1MHz, Figure 6	T_A = +25°C		16		pF

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, V_{GND} = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 10.8V, V_D = 3V, 8V, I_S = 1.0mA	T_A = +25°C		100	160	Ω
			T_A = T_{MIN} to T_{MAX}			200	
SUPPLY							
Power-Supply Range	V+			10		30	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V			15	100	µA
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V		-100	-15		µA
DYNAMIC							
Turn-On Time	t_{ON}	V_S = 8V, Figure 2	T_A = +25°C		300	400	ns
Turn-Off Time	t_{OFF}	V_S = 8V, Figure 2	T_A = +25°C		60	200	ns
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0V	T_A = +25°C		5	10	pC

Note 2: Typical values are for **design aid only,** are not guaranteed, and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On-resistance match between channels and flatness is guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

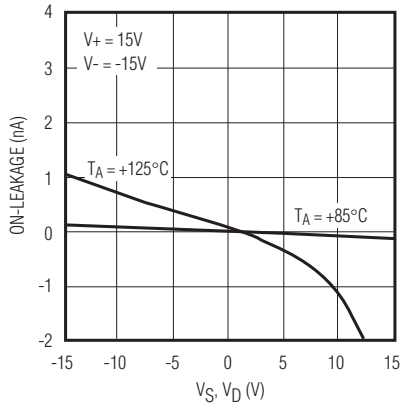
Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.

Note 7: Between any two switches.

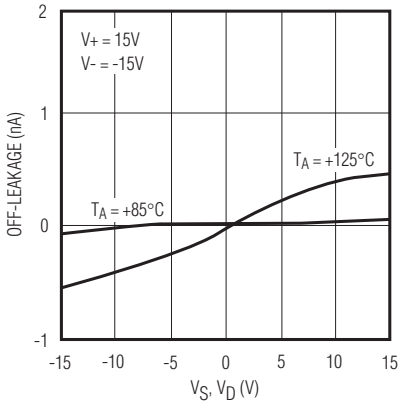
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

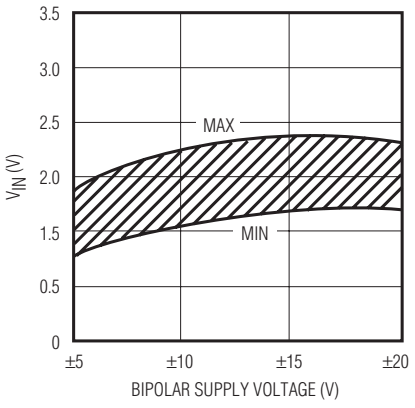
ON-LEAKAGE CURRENTS



OFF-LEAKAGE CURRENTS



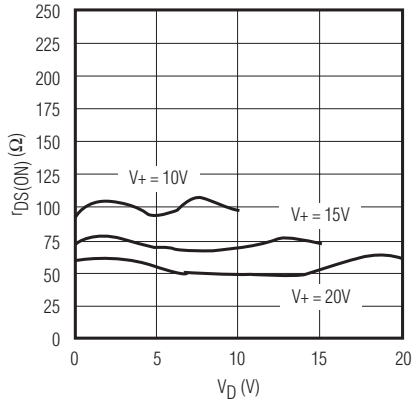
SWITCHING THRESHOLD vs. BIPOLAR SUPPLY VOLTAGE



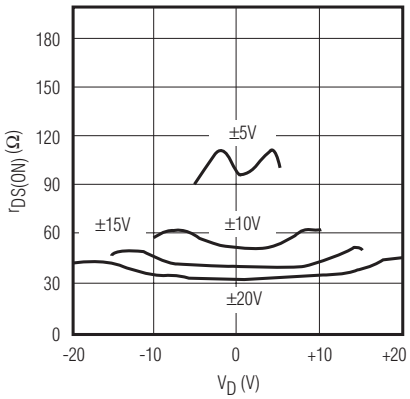
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

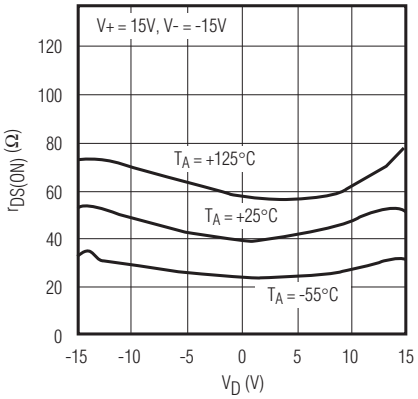
ON-RESISTANCE vs. V_D AND UNIPOLAR SUPPLY VOLTAGE



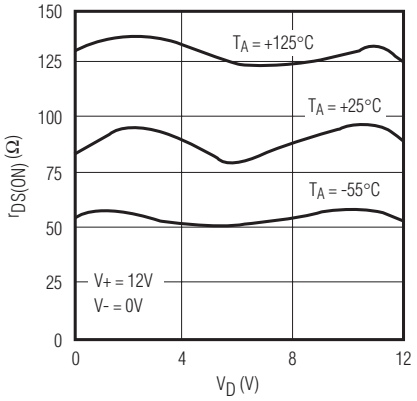
ON-RESISTANCE vs. V_D AND BIPOLAR SUPPLY VOLTAGE



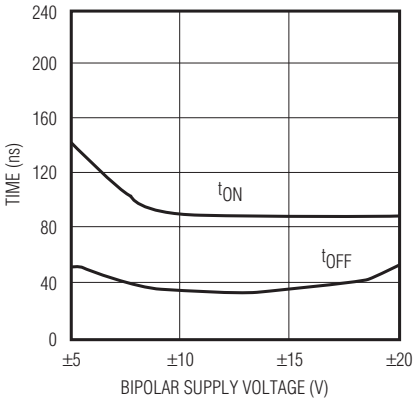
ON-RESISTANCE vs. V_D AND BIPOLAR VOLTAGE AND TEMPERATURE



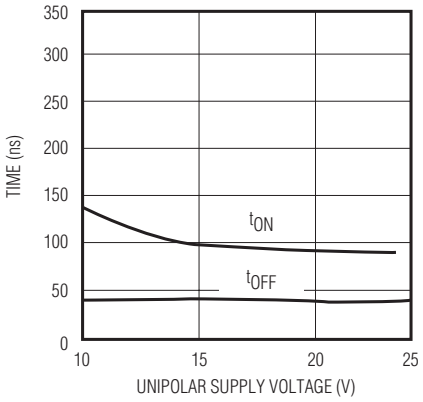
ON-RESISTANCE vs. V_D AND UNIPOLAR SUPPLY VOLTAGE AND TEMPERATURE



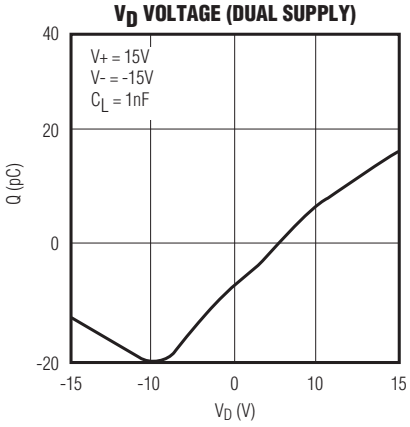
SWITCHING TIMES vs. BIPOLAR SUPPLY VOLTAGE



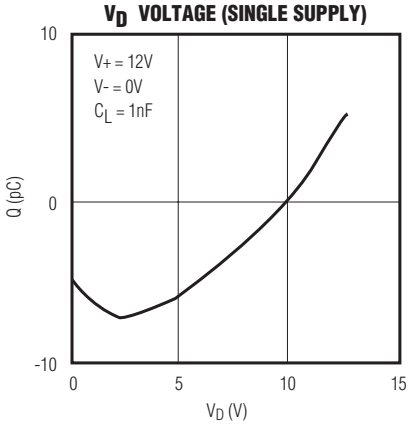
SWITCHING TIMES vs. UNIPOLAR SUPPLY VOLTAGE



CHARGE INJECTION vs. V_D VOLTAGE (DUAL SUPPLY)



CHARGE INJECTION vs. V_D VOLTAGE (SINGLE SUPPLY)



Pin Description

PIN		NAME	FUNCTION
DIP/SO	THIN QFN-EP		
1, 16, 9, 8	15, 14, 7, 6	IN1–IN4	Input
2, 15, 10, 7	16, 13, 8, 5	D1–D4	Analog Switch Drain Terminal
3, 14, 11, 6	1, 12, 9, 4	S1–S4	Analog Switch Source Terminal
4	2	V-	Negative-Supply Voltage Input
5	3	GND	Ground
12	10	N.C.	Not Internally Connected
13	11	V+	Positive-Supply Voltage Input—Connected to Substrate
—	—	EP	Exposed Pad. Connect EP to V+. Do not use EP as a sole V+ connection. (Thin QFN package only.)

Applications Information

Operation with Supply Voltages Other Than ±15V

Using supply voltages other than ±15V reduces the analog signal range. The DG441/DG442 switches operate with ±4.5V to ±20V bipolar supplies or with a +10V to +30V single supply; connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies such as +24V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with ±20V, ±15V, ±10V, and ±5V supplies. (Switching times increase by a factor of two or more for operation at ±5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, followed by V- and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding external diodes reduces the analog-signal range to 1V below V+ and 1V above V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

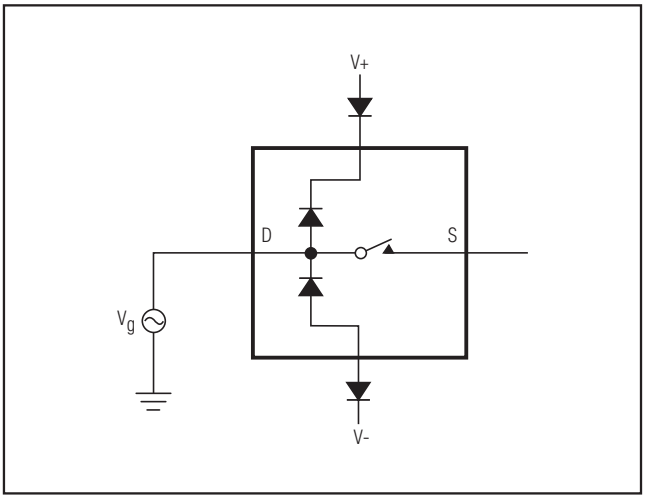


Figure 1. Overvoltage Protection Using External Blocking Diodes

Timing Diagrams/Test Circuits

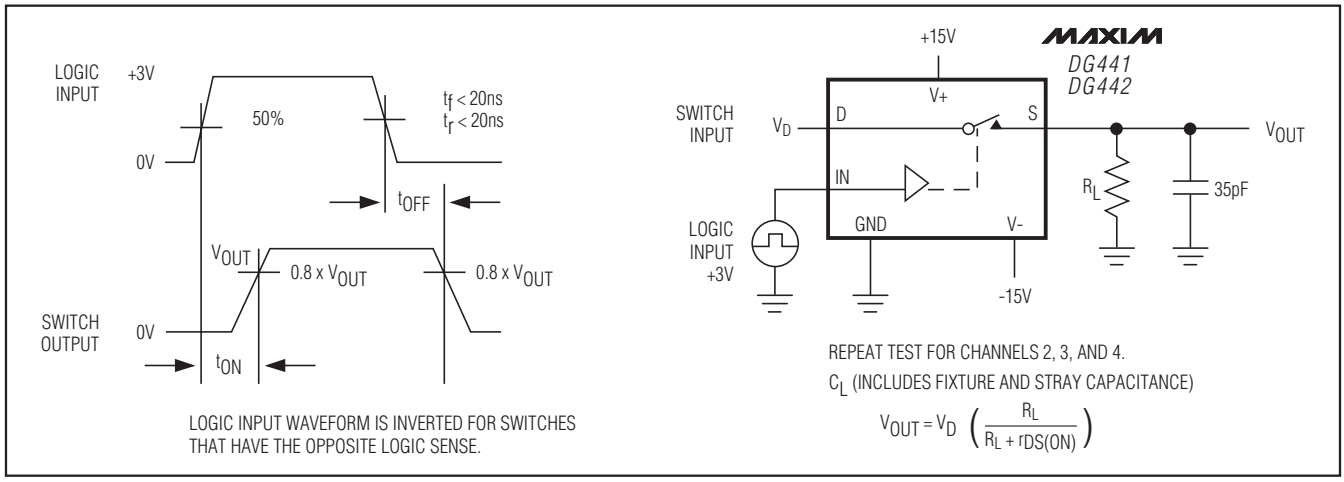


Figure 2. Switching Time

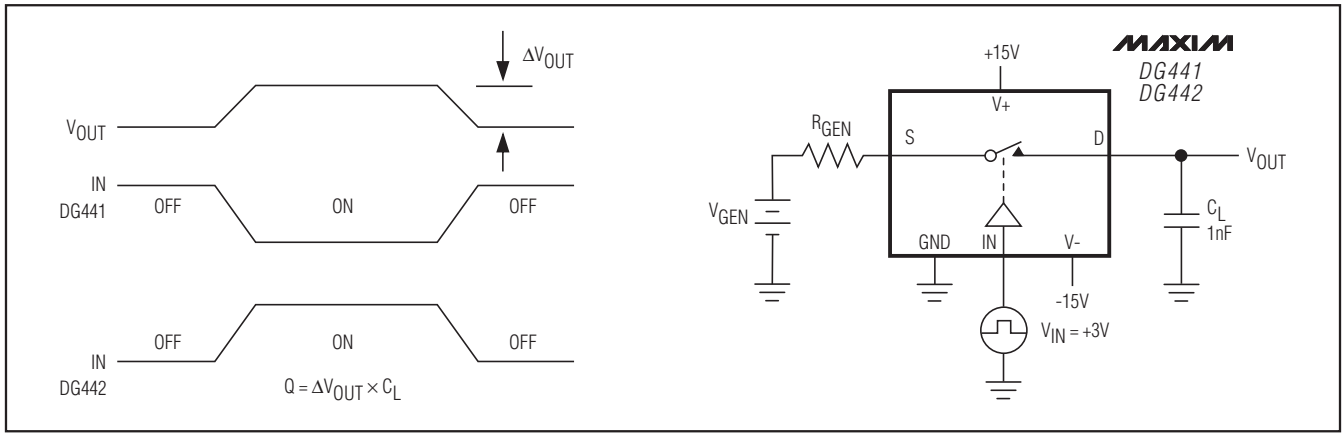


Figure 3. Charge Injection

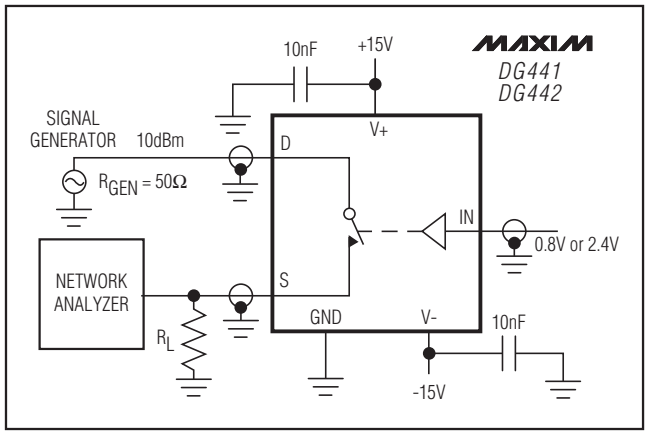


Figure 4. Off-Isolation Rejection Ratio

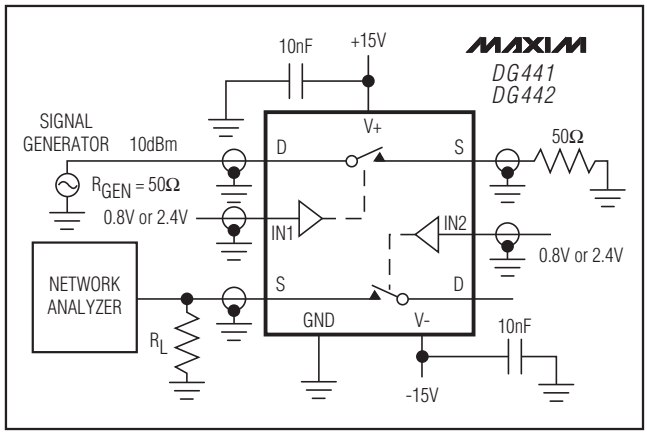


Figure 5. Crosstalk (repeat for channels 3 and 4)

Improved, Quad, SPST Analog Switches

Timing Diagrams/ Test Circuits (continued)

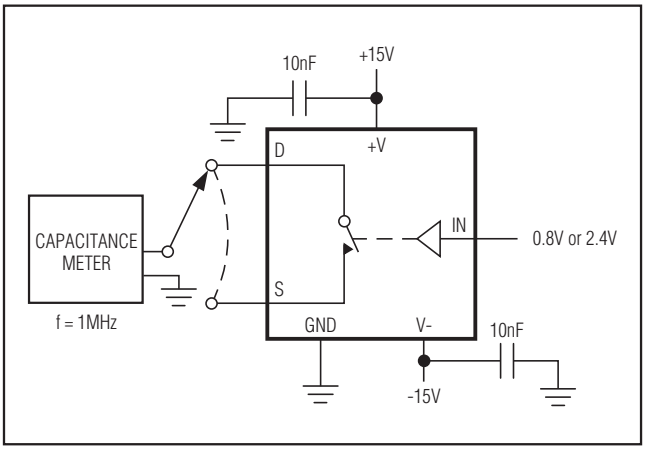


Figure 6. Source/Drain-On/Off Capacitance

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG441DK	-40°C to +85°C	16 CERDIP
DG441ETE	-40°C to +85°C	16 Thin QFN-EP**
DG441AK	-55°C to +125°C	16 CERDIP***
DG441MY/PR	-55°C to +125°C	16 Narrow SO
DG442CJ	0°C to +70°C	16 Plastic DIP
DG442CY	0°C to +70°C	16 Narrow SO
DG442C/D	0°C to +70°C	Dice*
DG442DJ	-40°C to +85°C	16 Plastic DIP
DG442DY	-40°C to +85°C	16 Narrow SO
DG442DK	-40°C to +85°C	16 CERDIP
DG442ETE	-40°C to +85°C	16 Thin QFN-EP**
DG442AK	-55°C to +125°C	16 CERDIP***
DG442MY/PR	-55°C to +125°C	16 Narrow SO

Note: *Devices are available in both leaded and lead(Pb)-free packaging. Specify lead-free by adding the + symbol at the end of the part number when ordering.*
**Contact factory for dice specifications.*
***EP = Exposed pad.*
****Contact factory for availability and processing to MIL-STD-883B. Not available in lead-free.*

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 Plastic DIP	P16-1	**21-0043**
16 Narrow SO	S16-3	**21-0041**
16 CERDIP	J16-3	**21-0045**
16 Thin QFN-EP (5mm x 5mm)	T1655-2	**21-0140**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	5/09	Added ruggedized plastic.	1, 2, 6, 8