

MITSUBISHI LSTTLs M74LS166AP

8-BIT SHIFT REGISTER

DESCRIPTION

The M74LS166AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input — serial output shift register function.

FEATURES

- Parallel-to-serial conversion
- Clock inhibit input
- Direct overriding reset
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

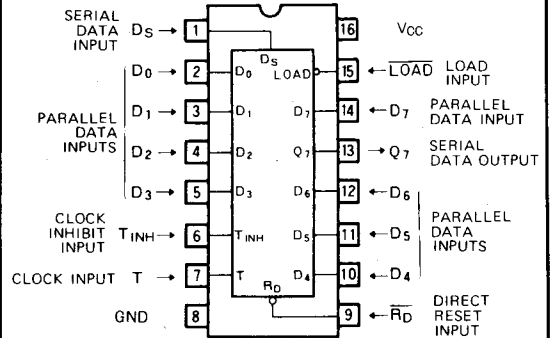
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

Parallel or serial input mode is selected via the load input $\overline{\text{LOAD}}$ signal. When $\overline{\text{LOAD}}$ is high-level, serial input enables the serial data input and couples the eight flip-flop for serial shifting with each clock pulse. Conversely, when $\overline{\text{LOAD}}$ is low-level, parallel data inputs $D_0 \sim D_7$ are enabled and synchronous loading occurs on the next clock pulse. While during parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enable the clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other

PIN CONFIGURATION (TOP VIEW)

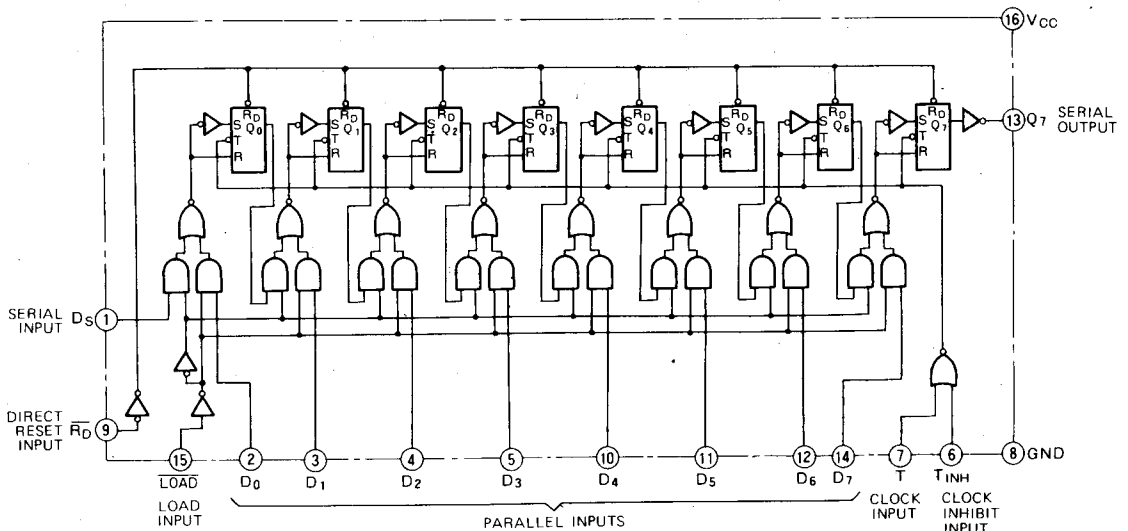


Outline 16P4

clock input. The clock-inhibit input should be change to the high level only while the clock input is high. The buffered, direct reset input $\overline{R_D}$ overrides all other inputs, including the clock, and sets all flip-flop to zero.

M74LS166AP has been improved to resolve timing problems on $\overline{\text{LOAD}}$ input signal switching that occurred in the M74LS166P. Serial output Q_7 has also been provided with a buffer to reduce noise, resulting in a change in specifications.

BLOCK DIAGRAM



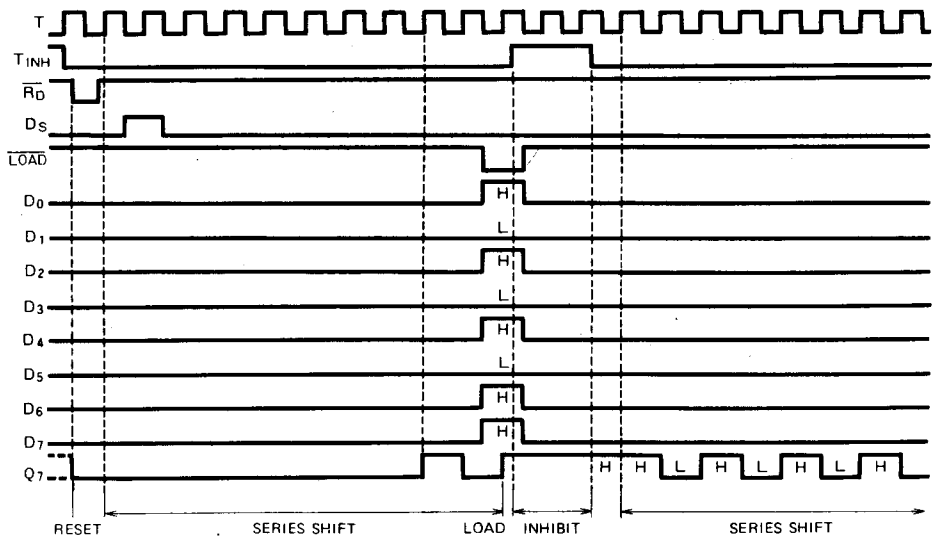
8-BIT SHIFT REGISTER

FUNCTION TABLE (Note 1)

t_n						t_{n+1}		
$\overline{R_D}$	$\overline{LOAD}$	T_{INH}	T	D_S	Parallel Inputs	Internal outputs		Q_7
					$D_0 \cdots D_7$	Q_0	Q_1	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{00}	Q_{10}	Q_{70}
H	L	L	$\uparrow$	X	$D_0 \cdots D_7$	D_0	D_1	D_7
H	H	L	$\uparrow$	H	X	H	Q_{0n}	Q_{6n}
H	H	L	$\uparrow$	L	X	L	Q_{0n}	Q_{6n}
H	X	H	$\uparrow$	X	X	Q_{00}	Q_{1n}	Q_{70}

Note 1. X : Irrelevant
 $\uparrow$: Transition from low to high (positive edge trigger)
 $D_0 \sim D_7$: Indicates status prior to clock pulse at input D_0 thru D_7 .
 $Q_{00} \cdots Q_{70}$: Indicates initial status of output Q_0 thru Q_7 .
 $Q_{0n} \cdots Q_{7n}$: Indicates status of Q_0 thru Q_7 immediately prior to clock input
 t_{n+1} : Bit time after one clocking transition.

TIMING DIAGRAM



8-BIT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level output	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	$^\circ\text{C}$
T_{stg}	Storage temperature range		$-65 \sim +150$	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geq 2.7\text{V}$	0	-400	μA
I_{OL}	Low-level output current	$V_{OL} \leq 0.4\text{V}$	0	4	mA
		$V_{OL} \leq 0.5\text{V}$	0	8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75\text{V}$, $I_{IC} = -18\text{mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75\text{V}$, $V_I = 0.8\text{V}$ $V_I = 2\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75\text{V}$ $V_I = 0.8\text{V}$, $V_I = 2\text{V}$		0.25	0.4	V
		$I_{OL} = 4\text{mA}$ $I_{OL} = 8\text{mA}$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$			20	μA
		$V_{CC} = 5.25\text{V}$, $V_I = 10\text{V}$			0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$			-0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25\text{V}$, $V_O = 0\text{V}$	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = 5.25\text{V}$ (Note 3)		20	32	mA

* : All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

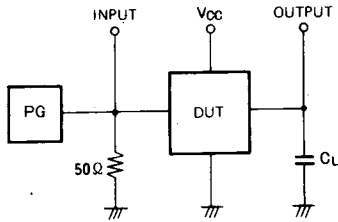
3. With all outputs open, 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency		25	38		MHz
t_{PHL}	High-to-low-level output propagation time, from input R_D to output Q_7	$C_L = 15\text{pF}$ (Note 5)		18	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output Q_7			10	20	ns
t_{PHL}				12	25	ns

8-BIT SHIFT REGISTER

Note 4. Measurement circuit

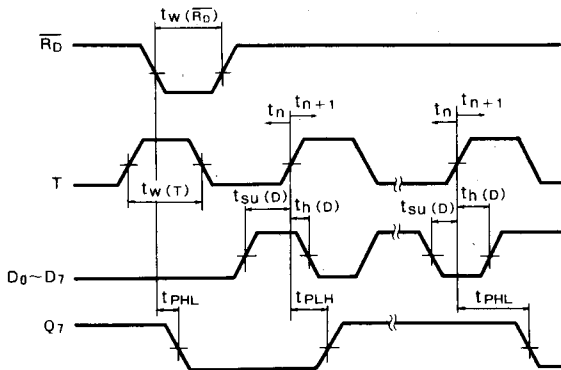


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$, $t_w = 500\text{ns}$, $V_P = 3V_{P-P}$, $Z_0 = 50\Omega$.
 (2) C_L includes jig and probe capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(T)$	Clock pulse width		20	14		ns
$t_w(\overline{R_D})$	Reset pulse width		20	8		ns
$t_{su}(D)$	Setup time D_S , $D_0 \sim D_7$ to T		20	12		ns
$t_{su}(\overline{LOAD})$	Setup time $\overline{LOAD}$ to T		30	12		ns
t_h	Hold time all inputs to T		0	-10		ns

TIMING DIAGRAM (Reference level = 1.3V)

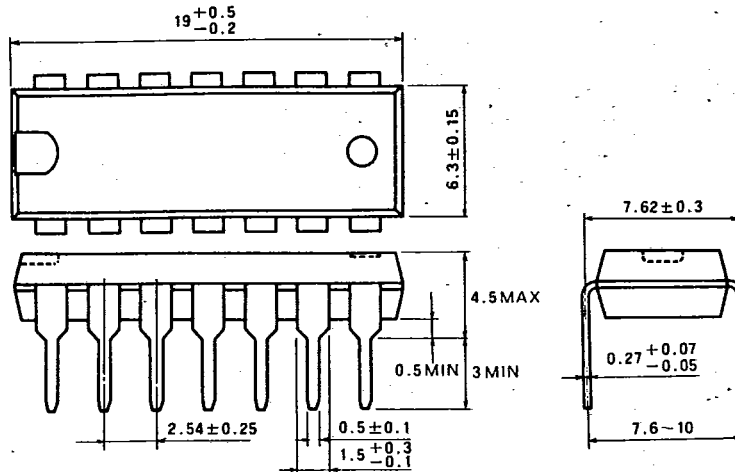


TEST CONDITION TABLE

Data input for test	$\overline{LOAD}$	Output tested	Bit time
D_7	0V	Q_7	t_{n+1}
D_S	4.5V	Q_7	t_{n+8}

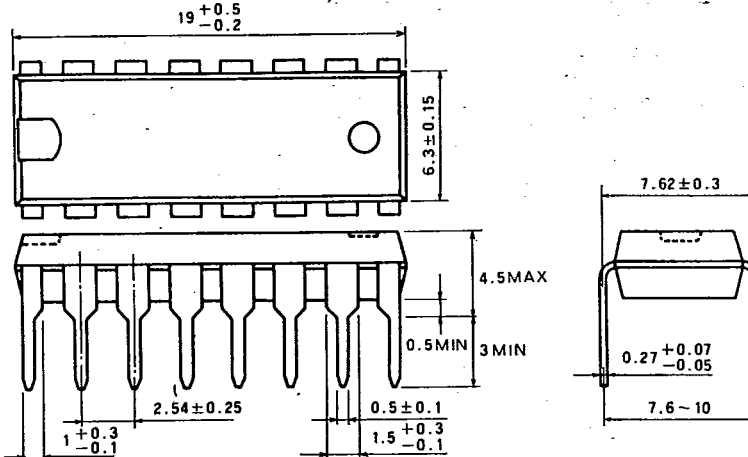
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

