

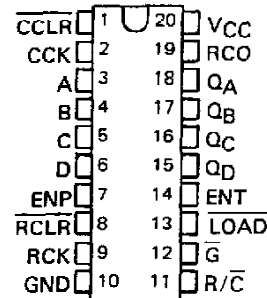
SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

SDLS198

D2423, JANUARY 1981—REVISED MARCH 1988

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . . Decade Counter, Direct Clear
- 'LS691 . . . Binary Counter, Direct Clear
- 'LS693 . . . Binary Counter, Synchronous Clear

SN54LS690, SN54LS691, SN54LS693 . . . J PACKAGE
SN74LS690, SN74LS691, SN74LS693 . . . DW OR N PACKAGE
(TOP VIEW)



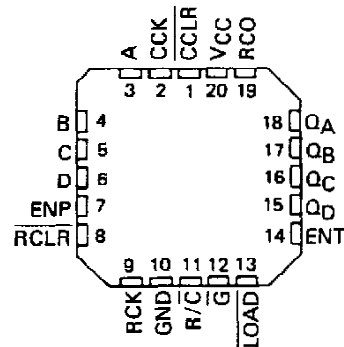
description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P inputs and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/\bar{C} , selects the counter when low or the register when high for the three-state outputs, Q_A , Q_B , Q_C , and Q_D . These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

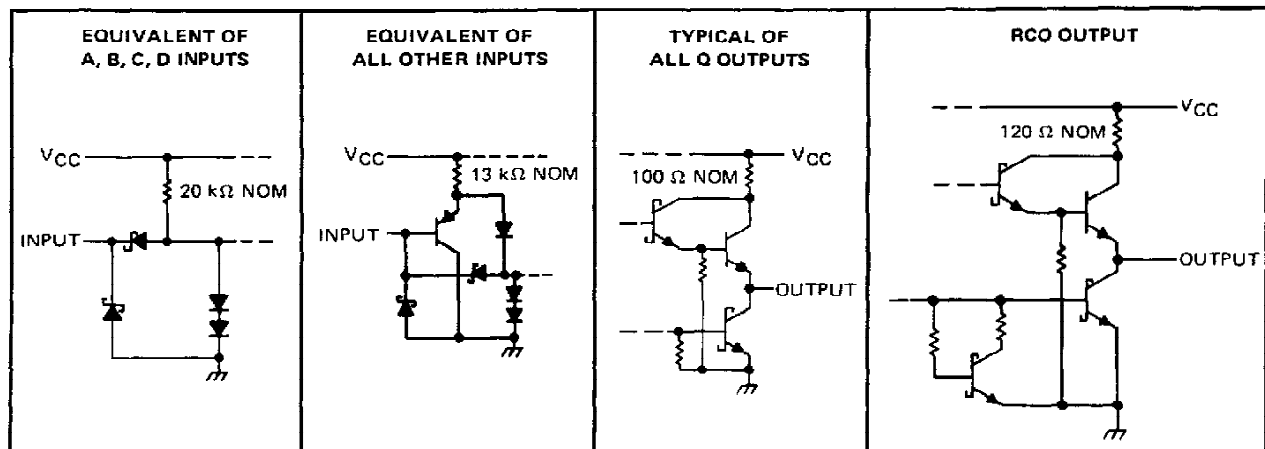
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered: The clear line is active low and is asynchronous on the 'LS690 and 'LS691, synchronous on the 'LS693. Loading of the counter is accomplished when \overline{LOAD} is taken low and a positive-transition occurs on the counter clock CCK.

Expansion is easily accomplished by connecting RCO of the first stage to ENT of the second stage, etc. All ENP inputs can be tied common and used as master enable or disable control.

SN54LS690, SN54LS691, SN54LS693 . . . FK PACKAGE
(TOP VIEW)



schematics of inputs and outputs



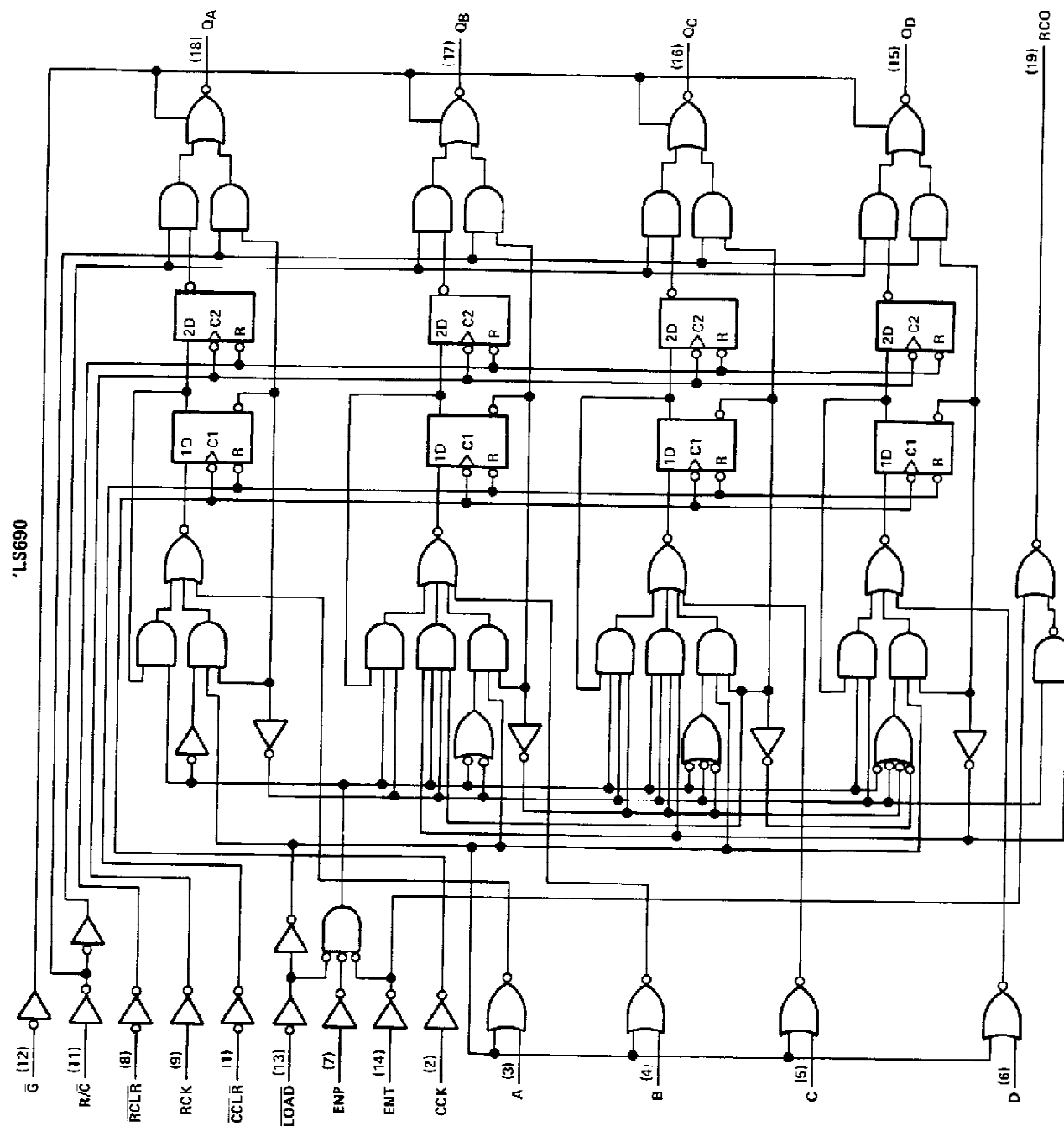
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SN54LS690, SN74LS690
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (positive logic)

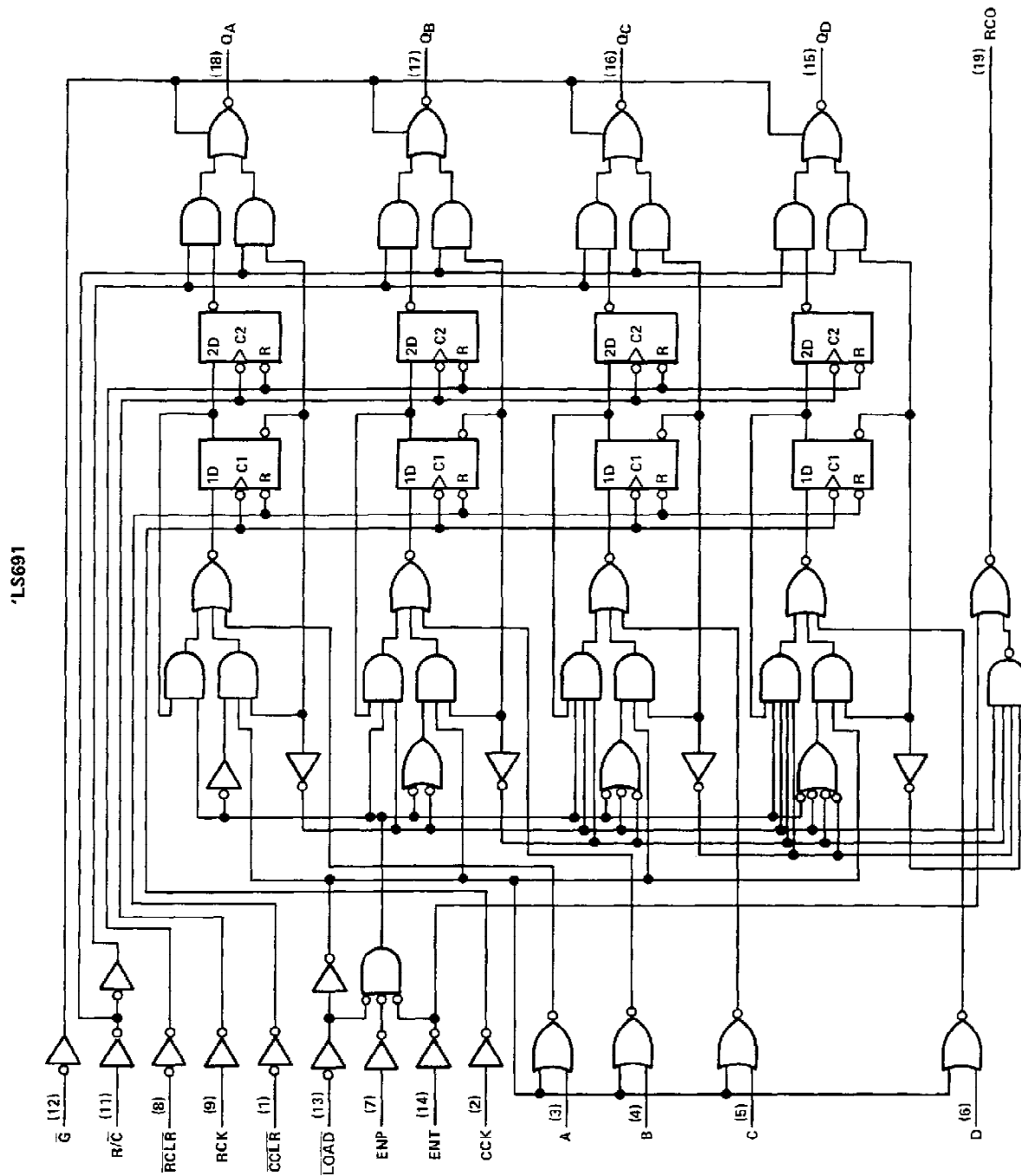


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SN54LS691, SN74LS691
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (positive logic) (continued)



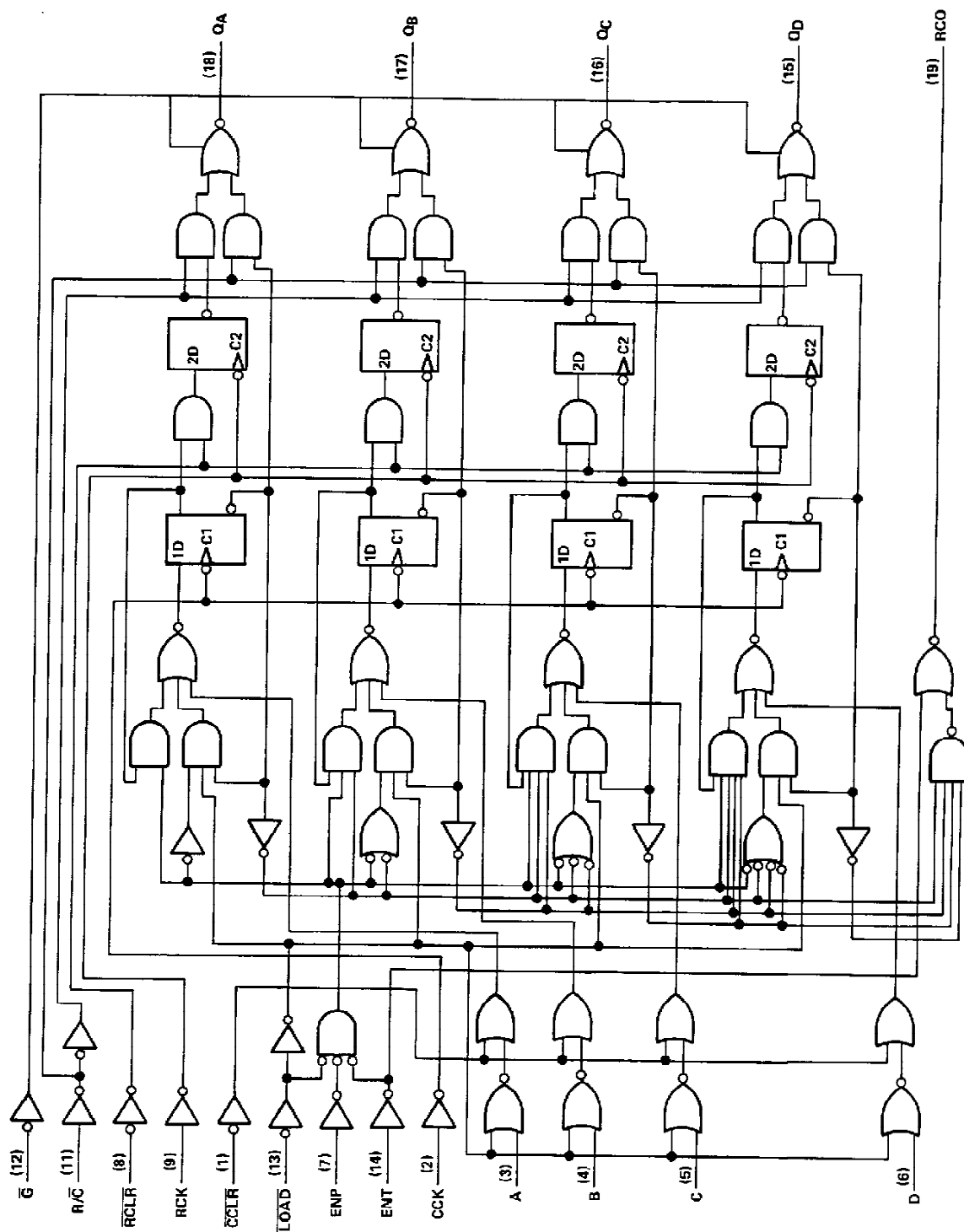
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SN54LS693, SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (positive logic) (continued)

'LS693

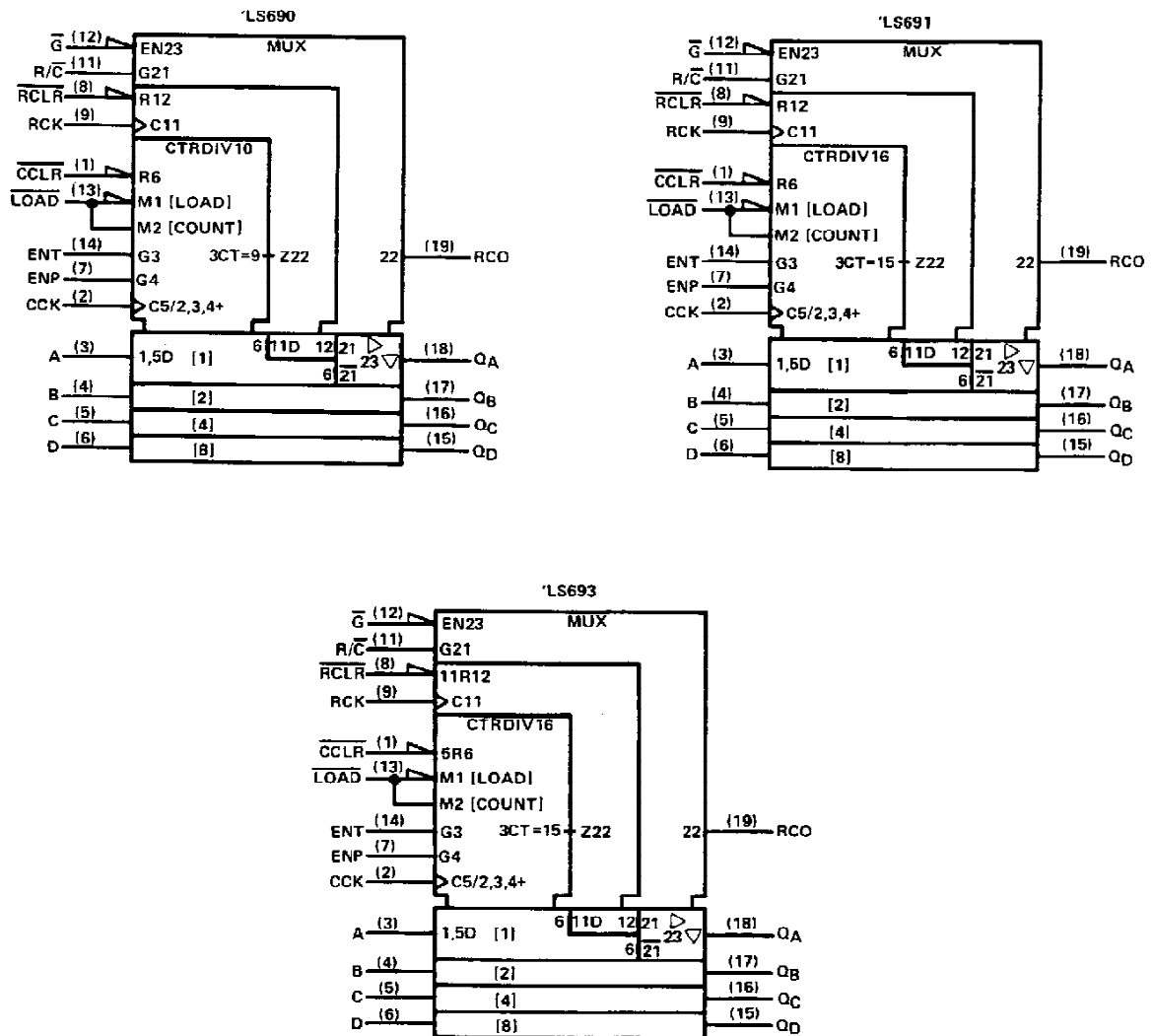


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SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

logic symbols[†]



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

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SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693 **SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS** **AND MULTIPLEXED 3-STATE OUTPUTS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|-----------------------------------------------------------------------|----------------|
| Supply voltage, V_{CC} (See Note 1) | 7 V |
| Input voltage | 7 V |
| Off-state output voltage | 5.5 V |
| Operating free-air temperature range: SN54LS690, SN54LS691, SN54LS693 | -55°C to 125°C |
| SN74LS690, SN74LS691, SN74LS693 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | | | SN54LS [*] | | | SN74LS [*] | | | UNIT |
|-------------|--------------------------------|--------------------------------|---------------------|-----|------|---------------------|-----|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| I_{OH} | High-level output current | Q | | | -1 | | | -2.6 | mA |
| | | R _{CO} | | | -0.4 | | | -0.4 | mA |
| I_{OL} | Low-level output current | Q | | | 12 | | | 24 | mA |
| | | R _{CO} | | | 4 | | | 8 | mA |
| f_{clock} | Clock frequency | CCK | 0 | | 20 | 0 | | 20 | MHz |
| | | RCK | 0 | | 20 | 0 | | 20 | MHz |
| t_w | Pulse duration | CCK high or low | 25 | | | 25 | | | ns |
| | | RCK high or low | 25 | | | 25 | | | |
| | | 'LS690, 'LS691 RCLR low | 20 | | | 20 | | | |
| | | CCLR low | 20 | | | 20 | | | |
| t_{su} | Setup time before CCK ↑ | A thru D | 30 | | | 30 | | | ns |
| | | ENP or ENT | 30 | | | 30 | | | |
| | | LOAD ↓ | 30 | | | 30 | | | |
| | | 'LS693 CCLR ↓ | 40 | | | 40 | | | |
| | | 'LS690, 'LS691 CCLR ↑ inactive | 25 | | | 25 | | | |
| t_{su} | Setup time before RCK ↑ | CCK ↑ (see Note 2) | 30 | | | 30 | | | ns |
| | | 'LS690, 'LS691 RCLR ↑ inactive | 25 | | | 25 | | | |
| | | 'LS693 RCLR ↓ | 20 | | | 20 | | | |
| t_h | Hold time | Any input from CCK ↑ or RCK ↑ | 0 | | | 0 | | | ns |
| T_A | Operating free-air temperature | | -55 | | 125 | 0 | | 70 | °C |

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.



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SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54LS* | | | SN74LS* | | | UNIT | |
|-------------------|----------------------------|------------------------------------------------------------------------------------------------|--------------------------|-------|----------|---------|----------|-----|------|----|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V _{IK} | | V _{CC} = MIN, I _I = - 18 mA | | - 1.5 | | | - 1.5 | | | V |
| V _{OH} | Any Q | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX | I _{OH} = - 1 mA | | 2.4 3.1 | | | | | V |
| | I _{OH} = - 2.6 mA | | | | 2.4 3.1 | | | | | |
| | I _{OH} = - 0.4 mA | | 2.5 3.2 | | 2.7 3.2 | | | | | |
| V _{OL} | Any Q | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX | I _{OL} = 12 mA | | 0.25 0.4 | | 0.25 0.4 | | V | |
| | I _{OL} = 24 mA | | | | 0.35 0.5 | | | | | |
| | I _{OL} = 4 mA | | 0.25 0.4 | | 0.25 0.4 | | | | | |
| | I _{OL} = 8 mA | | | | 0.35 0.5 | | | | | |
| I _{OZH} | Any Q | V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 2.7 V | | 20 | | | 20 | | | μA |
| I _{OZL} | Any Q | V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 0.4 V | | - 20 | | | - 20 | | | μA |
| I _I | | V _{CC} = MAX, V _I = 7 V | | 0.1 | | | 0.1 | | | mA |
| I _{IH} | | V _{CC} = MAX, V _I = 2.7 V | | 20 | | | 20 | | | μA |
| I _{IL} | A thru D | V _{CC} = MAX, V _I = 0.4 V | | - 0.4 | | | - 0.4 | | | mA |
| | - 0.2 | | | - 0.2 | | | | | | |
| I _{OS} § | Any Q | V _{CC} = MAX, V _O = 0 V | | - 30 | - 130 | - 30 | - 130 | mA | | |
| | - 20 | | | - 100 | - 20 | - 100 | | | | |
| I _{CCH} | | V _{CC} = MAX, All outputs open | See Note 3 | | 46 65 | | 46 65 | | mA | |
| I _{CCL} | | | See Note 4 | | 48 70 | | 48 70 | | | |
| I _{CCZ} | | | See Note 5 | | 48 70 | | 48 70 | | | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured after two 4.5 V to 0-V to 4.5-V pulses have been applied to CCK and RCK while \bar{G} is grounded and all other inputs are at 4.5 V.

4. I_{CCL} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while all other inputs are grounded.

5. I_{CCZ} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while \bar{G} is at 4.5 V and all other inputs are grounded.


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SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS690, 'LS691 | | 'LS693 | | UNIT |
|-----------|-----------------|----------------|------------------------|----------------|-----|--------|-----|------|
| | | | | MIN | TYP | MAX | MIN | |
| tPLH | CCK↑ | RCO | RL = 2 kΩ, CL = 15 pF | 23 | 40 | 23 | 40 | ns |
| tPHL | | | | 23 | 40 | 23 | 40 | |
| tPLH | ENT | RCO | | 13 | 20 | 13 | 20 | ns |
| tPHL | | | | 13 | 20 | 13 | 20 | |
| tPLH | CCK↑ | Q | RL = 667 Ω, CL = 45 pF | 12 | 20 | 12 | 20 | ns |
| tPHL | | | | 17 | 25 | 17 | 25 | |
| tPLH | RCK↑ | Q | | 12 | 20 | 12 | 20 | ns |
| tPHL | | | | 17 | 25 | 17 | 25 | |
| tPHL | CCLR↓ | Q | | 23 | 40 | | | ns |
| tPHL | RCLR↓ | Q | | 20 | 30 | | | ns |
| tPLH | R/C | Q | | 16 | 25 | 16 | 25 | ns |
| tPHL | | | | 16 | 25 | 16 | 25 | |
| tPZH | G↓ | Q | | 19 | 30 | 19 | 30 | ns |
| tPZL | | | | 19 | 30 | 19 | 30 | |
| tPHZ | G↑ | Q | RL = 667 Ω, CL = 5 pF | 17 | 30 | 17 | 30 | ns |
| tPLZ | | | | 17 | 30 | 17 | 30 | |

NOTE 6: Load circuits and voltage waveforms are shown in Section 1.

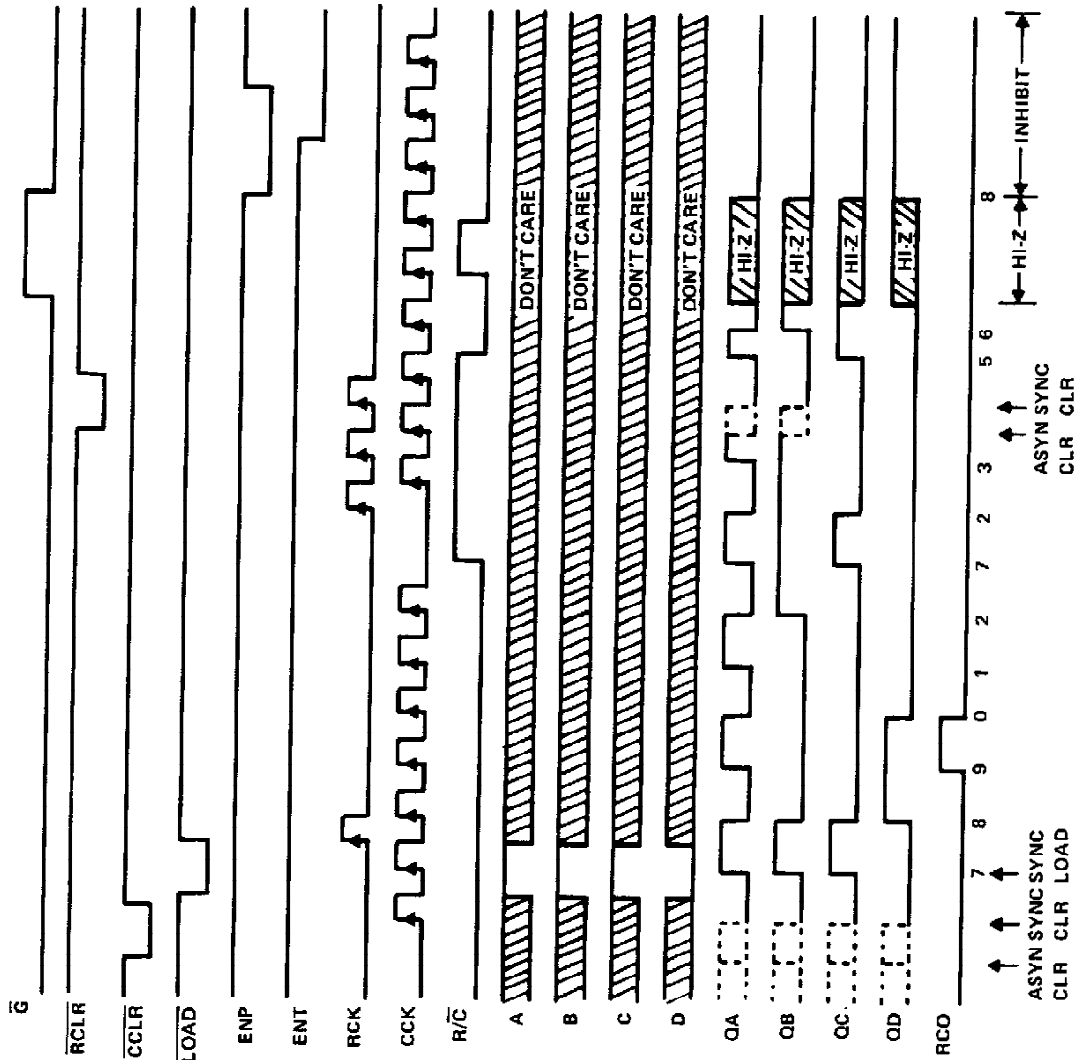
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SN54LS690, SN74LS690
 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
 AND MULTIPLEXED 3-STATE OUTPUTS

typical operating sequences

'LS690 DECADE COUNTER, Asynchronous Clear

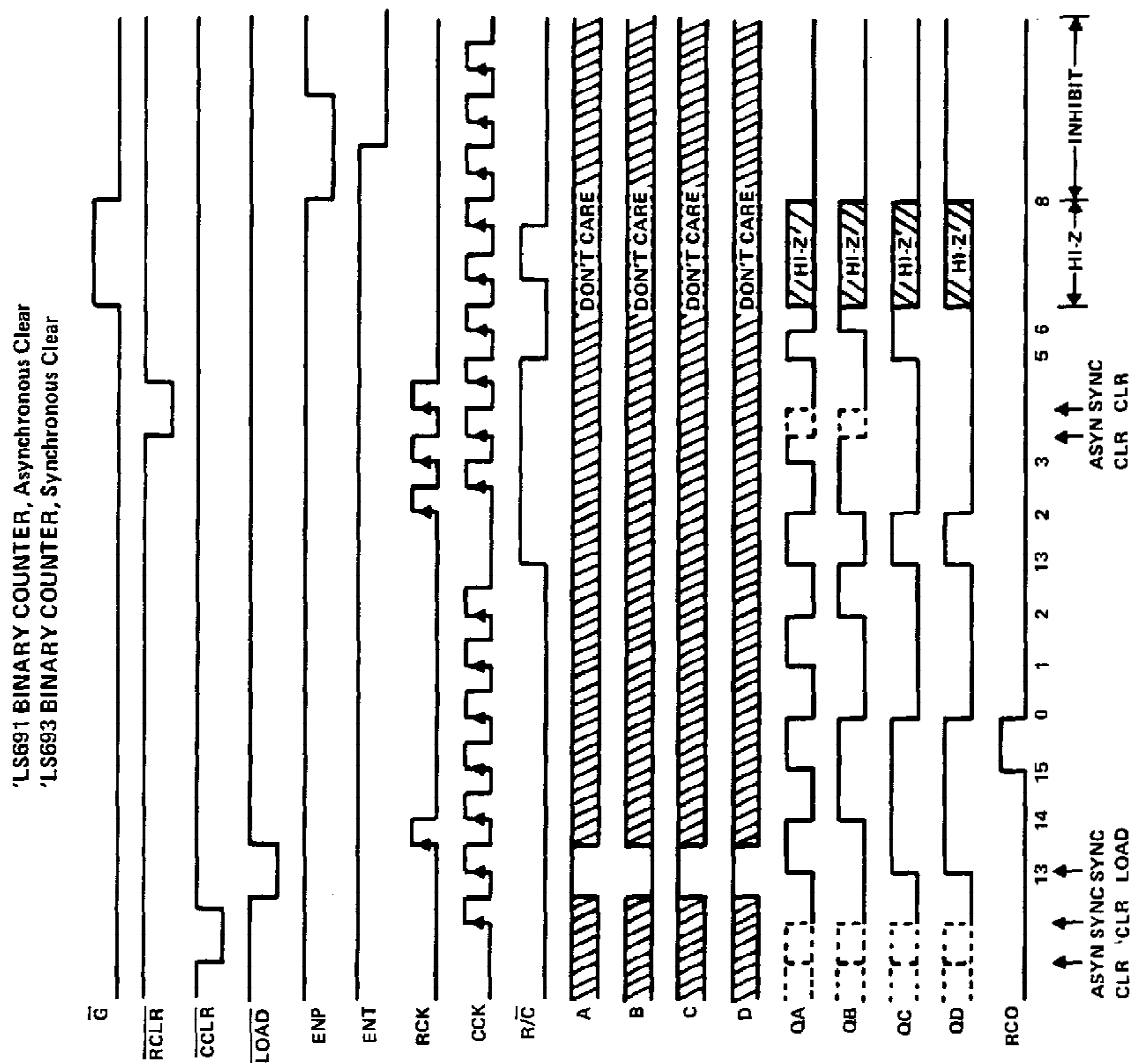


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SN54LS691, SN54LS693, SN74LS691, SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

typical operating sequences (continued)



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