

# SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

SDLS198

02423, JANUARY 1981—REVISED MARCH 1988

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . . Decade Counter, Direct Clear  
'LS691 . . . Binary Counter, Direct Clear  
'LS693 . . . Binary Counter, Synchronous Clear

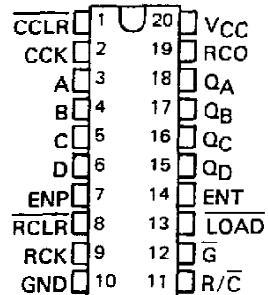
## description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P inputs and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, and Q<sub>D</sub>. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

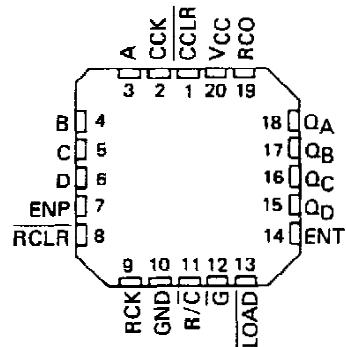
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered: The clear line is active low and is asynchronous on the 'LS690 and 'LS691, synchronous on the 'LS693. Loading of the counter is accomplished when LOAD is taken low and a positive-transition occurs on the counter clock CCK.

Expansion is easily accomplished by connecting RCO of the first stage to ENT of the second state, etc. All ENP inputs can be tied common and used as master enable or disable control.

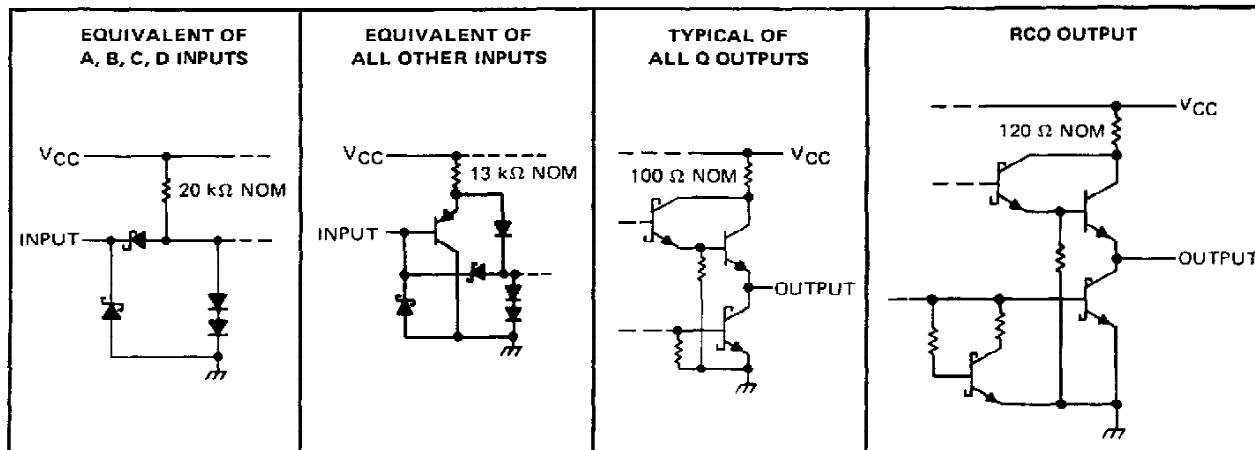
SN54LS690, SN54LS691, SN54LS693 . . . J PACKAGE  
SN74LS690, SN74LS691, SN74LS693 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54LS690, SN54LS691, SN54LS693 . . . FK PACKAGE  
(TOP VIEW)



## schematics of inputs and outputs



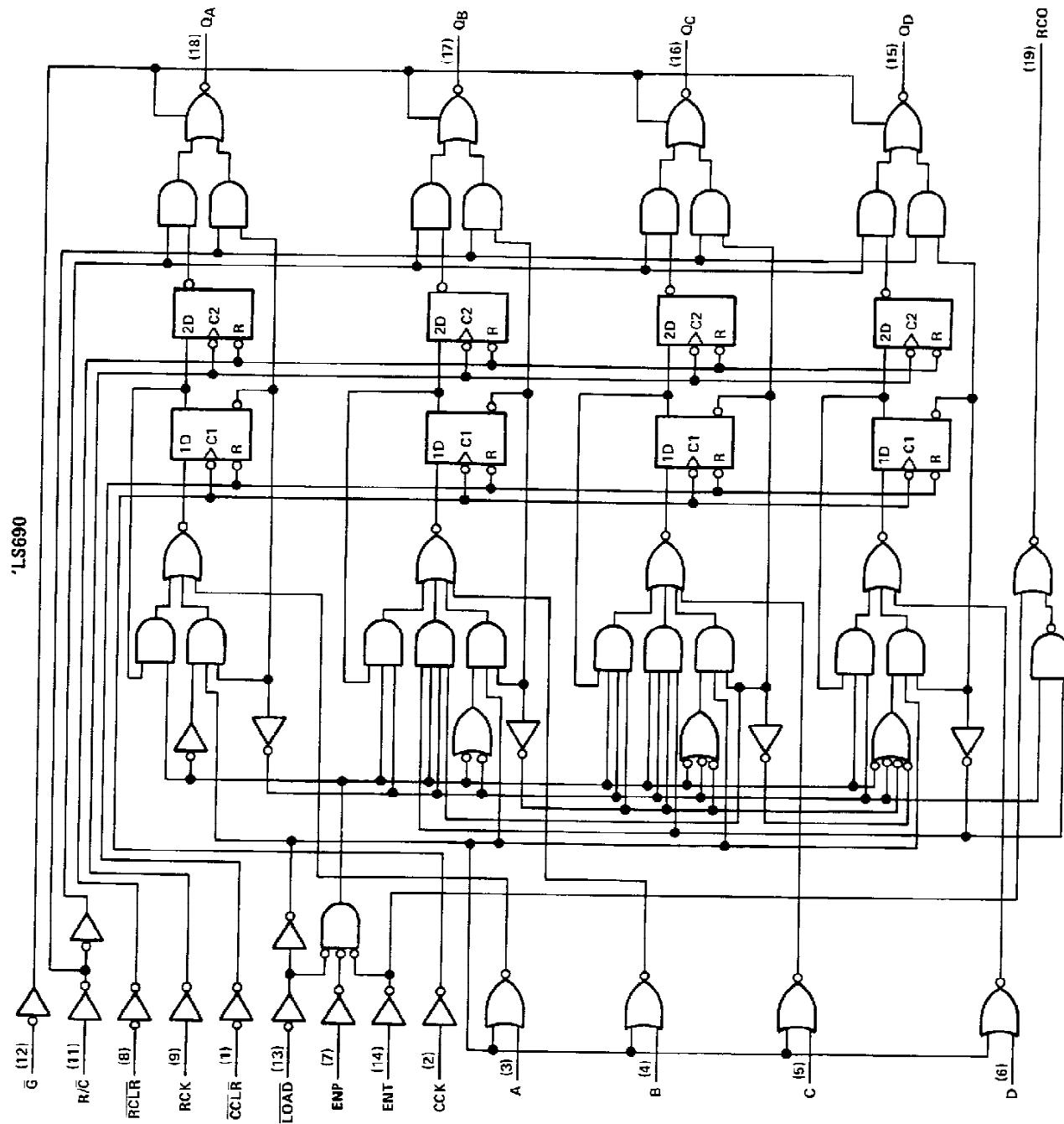
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**SN54LS690, SN74LS690**  
**SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS**  
**AND MULTIPLEXED 3-STATE OUTPUTS**

logic diagrams (positive logic)

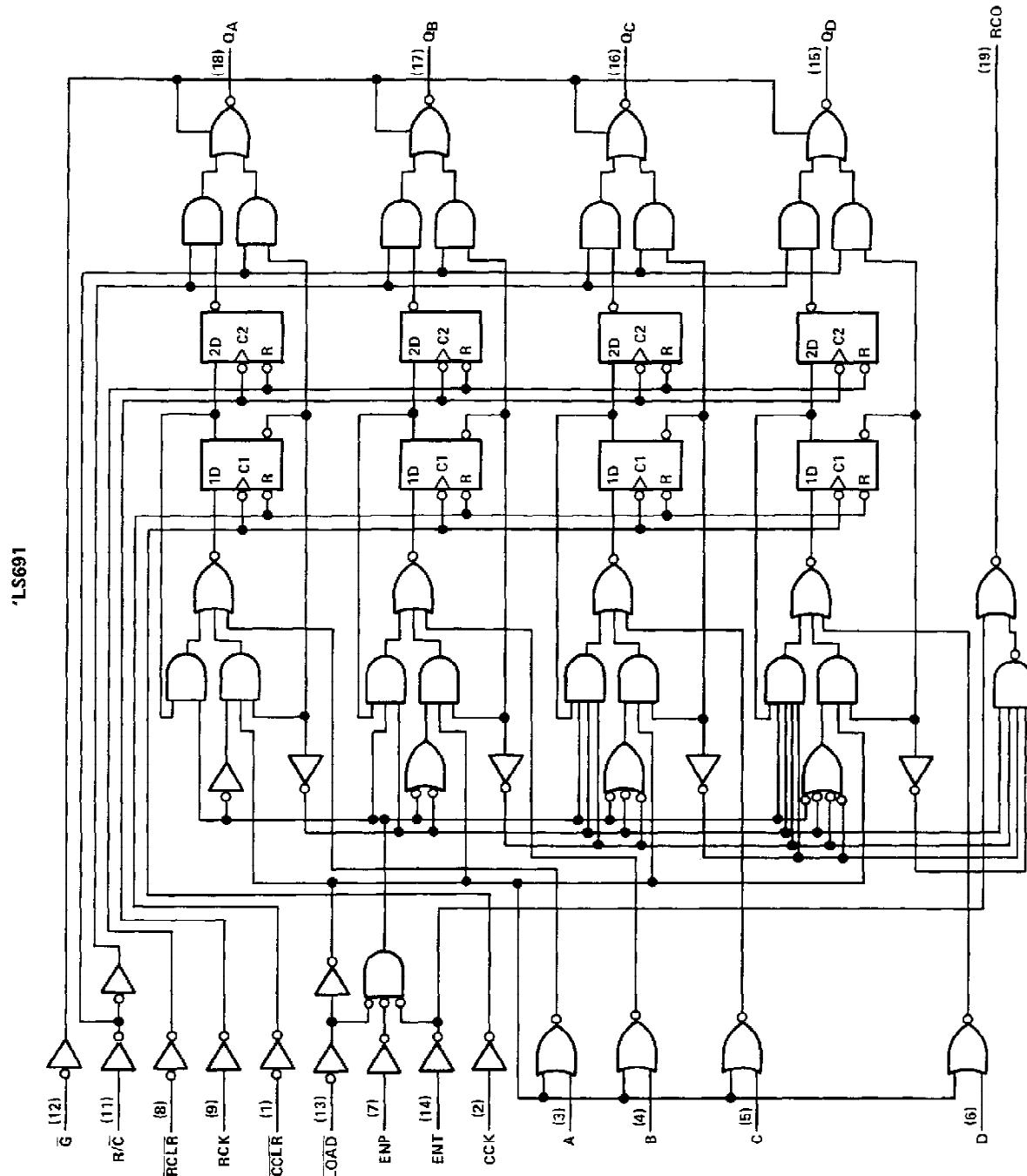


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**SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS**  
**AND MULTIPLEXED 3-STATE OUTPUTS**

logic diagrams (positive logic) (continued)

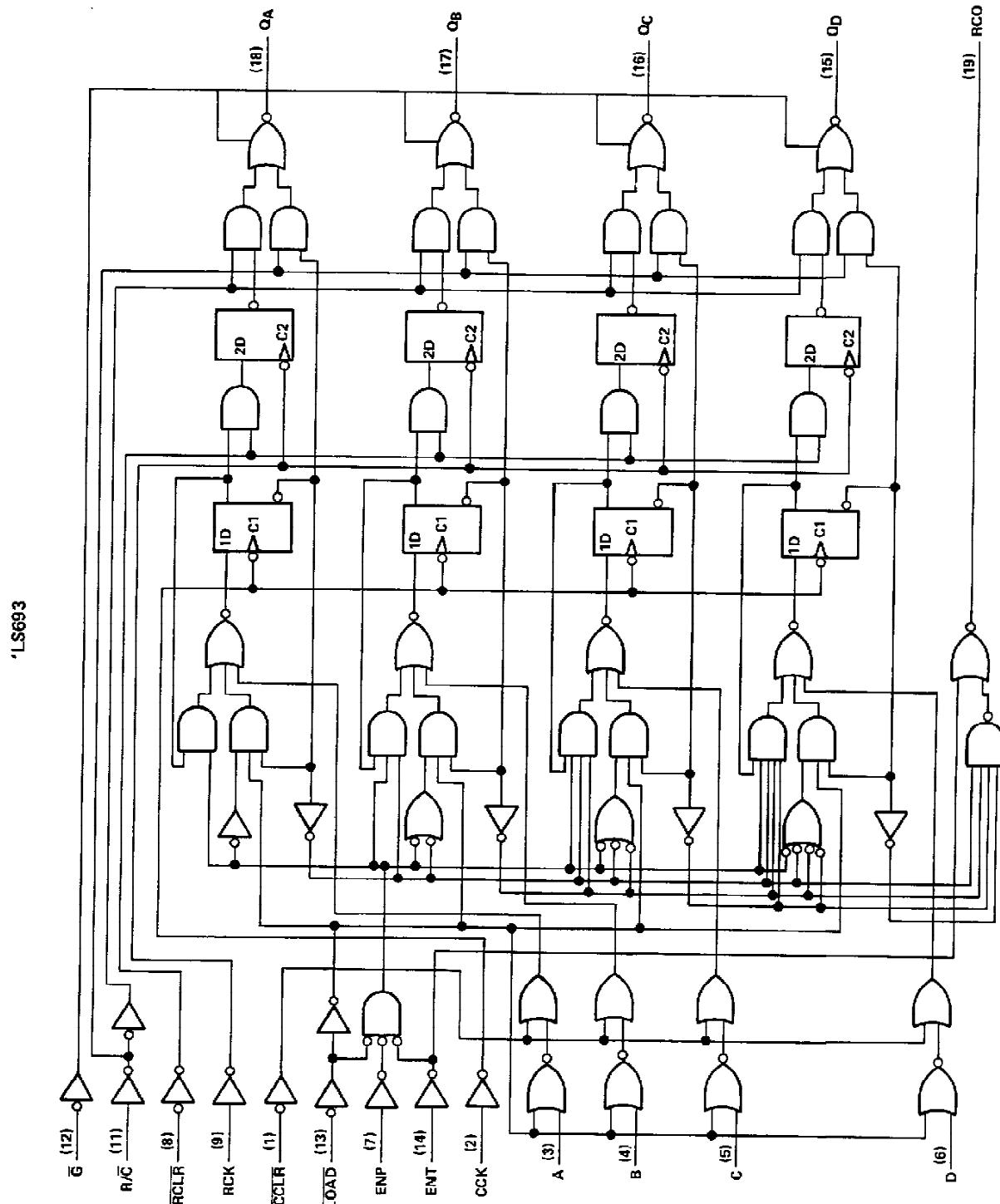


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**SN54LS693, SN74LS693**  
**SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS**  
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logic diagrams (positive logic) (continued)

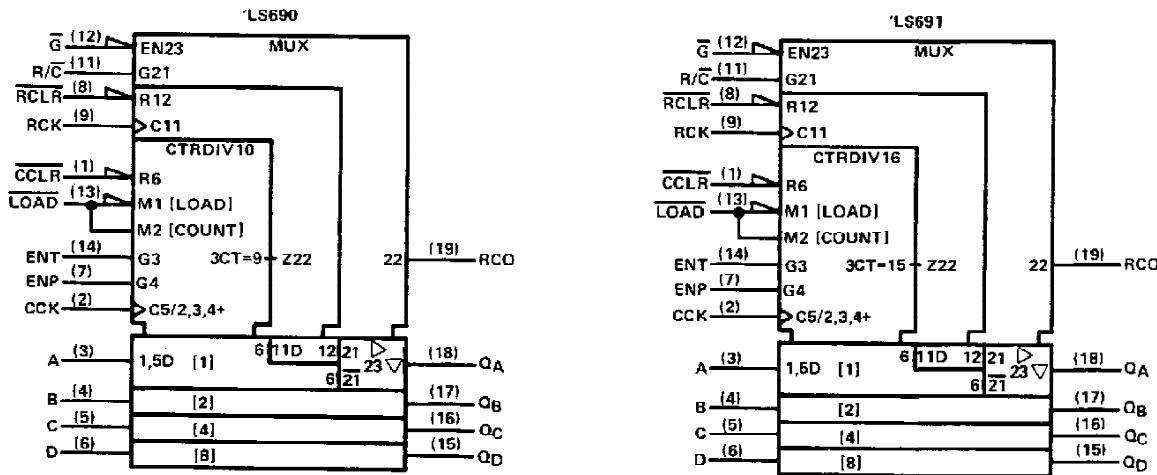


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**SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS**  
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logic symbols <sup>†</sup>



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

**SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693  
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

			SN54LS*			SN74LS*			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
$V_{CC}$	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage			2			2			V
$V_{IL}$	Low-level input voltage					0.7			0.8	V
$I_{OH}$	High-level output current			Q		~1			~2.6	mA
	RCO					~0.4			~0.4	mA
$I_{OL}$	Low-level output current			Q		12			24	mA
	RCO					4			8	mA
$f_{clock}$	Clock frequency			CCK		0	20	0	20	MHz
	RCK					0	20	0	20	MHz
$t_W$	Pulse duration			CCK high or low		25			25	ns
				RCK high or low		25			25	
				RCLR low		20			20	
				CCLR low		20			20	
				A thru D		30			30	
$t_{SU}$	Setup time before CCK $\uparrow$			ENP or ENT		30			30	ns
				LOAD $\downarrow$		30			30	
				'LS693	CCLR $\downarrow$	40			40	
				'LS690, 'LS691	CCLR $\uparrow$ inactive	25			25	
					CCK $\uparrow$ (see Note 2)	30			30	
$t_{SU}$	Setup time before RCK $\uparrow$			'LS690, 'LS691	RCLR $\uparrow$ inactive	25			25	ns
				'LS693	RCLR $\downarrow$	20			20	
						0			0	
$t_H$	Hold time	Any input from CCK $\uparrow$ or RCK $\uparrow$								ns
$T_A$	Operating free-air temperature				-55	125	0	70		°C

**NOTE 2:** This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

**SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693**  
**SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS**  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS'			SN74LS'			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	Any Q	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OH</sub> = -1 mA	2.4	3.1			V
	Any Q		I <sub>OH</sub> = -2.6 mA			2.4	3.1	
	RCO		I <sub>OH</sub> = -0.4 mA	2.5	3.2	2.7	3.2	
V <sub>OL</sub>	Any Q	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V
	Any Q		I <sub>OL</sub> = 24 mA			0.35	0.5	
	RCO		I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4	
	RCO		I <sub>OL</sub> = 8 mA			0.35	0.5	
I <sub>OZH</sub>	Any Q	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, V <sub>O</sub> = 2.7 V			20		20	μA
I <sub>OZL</sub>	Any Q	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, V <sub>O</sub> = 0.4 V			-20		-20	μA
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1		0.1	mA
I <sub>II</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20		20	μA
I <sub>IL</sub>	A thru D	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4		-0.4	mA
	All others				-0.2		-0.2	
I <sub>OS</sub> <sup>§</sup>	Any Q	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0 V		-30	-130	-30	-130	mA
	RCO			-20	-100	-20	-100	
ICCH		V <sub>CC</sub> = MAX, All outputs open	See Note 3		46	65	46	65
ICCL			See Note 4		48	70	48	70
ICCZ			See Note 5		48	70	48	70

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTES: 3. I<sub>CH</sub> is measured after two 4.5 V to 0-V to 4.5-V pulses have been applied to CCK and RCK while G is grounded and all other inputs are at 4.5 V.

4. I<sub>CL</sub> is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while all other inputs are grounded.

5. I<sub>CZ</sub> is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while G is at 4.5 V and all other inputs are grounded.

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**SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS**  
**AND MULTIPLEXED 3-STATE OUTPUTS**

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see note 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS690, 'LS691			'LS693			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	CCK↑	RCO	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$	23	40	23	40			ns	
$t_{PHL}$				23	40	23	40				
$t_{PLH}$				13	20	13	20			ns	
$t_{PHL}$				13	20	13	20				
$t_{PLH}$	CCK↑	Q	$R_L = 667 \Omega, C_L = 45 \text{ pF}$	12	20	12	20			ns	
$t_{PHL}$				17	25	17	25				
$t_{PLH}$				12	20	12	20			ns	
$t_{PHL}$				17	25	17	25				
$t_{PHL}$	$\overline{CCLR} \downarrow$	Q		23	40					ns	
$t_{PHL}$				20	30						
$t_{PLH}$				16	25	16	25			ns	
$t_{PHL}$				16	25	16	25				
$t_{PZH}$	$\overline{G} \downarrow$	Q		19	30	19	30			ns	
$t_{PZL}$				19	30	19	30				
$t_{PHZ}$	$\overline{G} \uparrow$	Q	$R_L = 667 \Omega, C_L = 5 \text{ pF}$	17	30	17	30			ns	
$t_{PLZ}$				17	30	17	30				

NOTE 6: Load circuits and voltage waveforms are shown in Section 1.

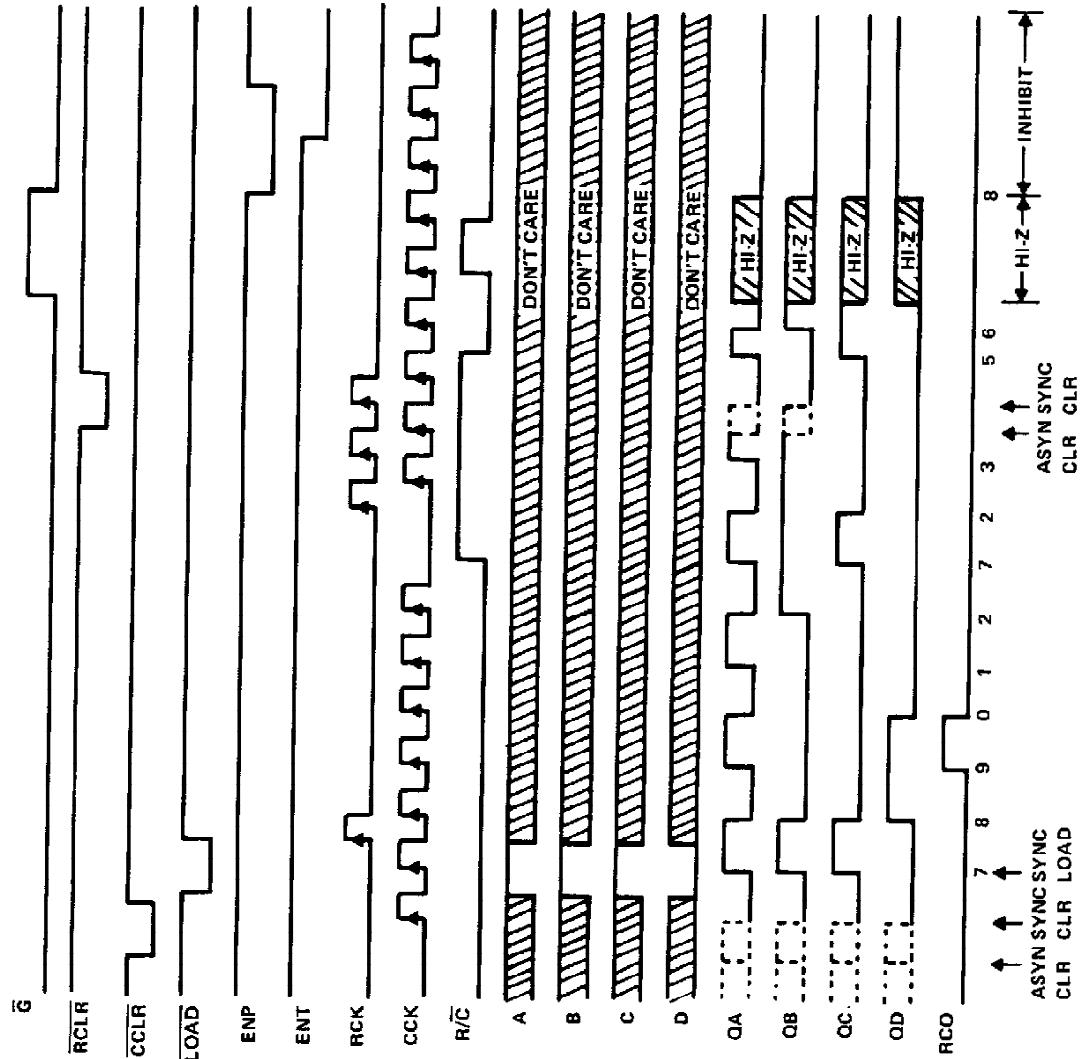
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typical operating sequences

'LS690 DECADE COUNTER, Asynchronous Clear

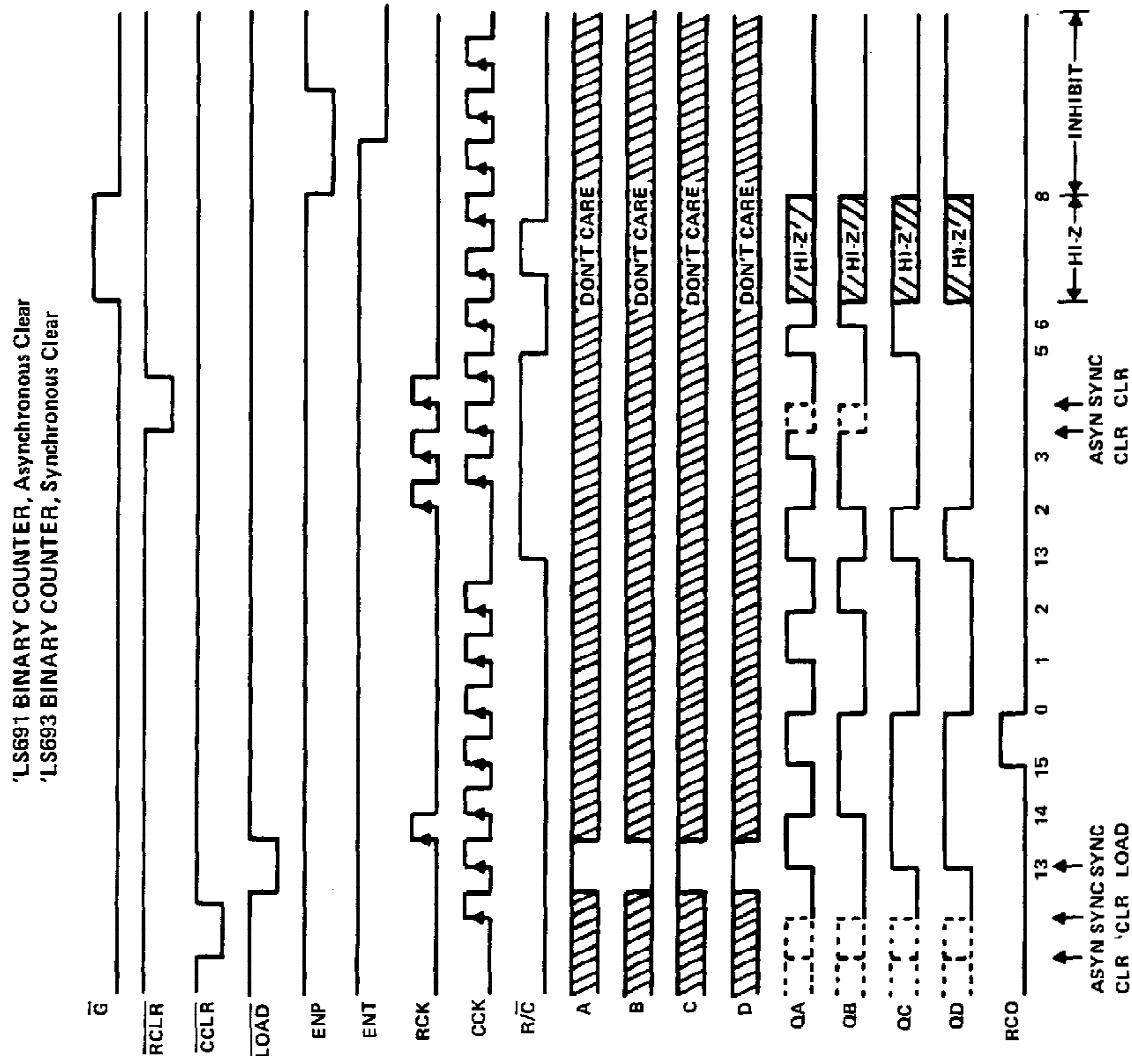


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### **typical operating sequences (continued)**



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