



# ICS8752

## Low SKEW, 1-TO-8

### LVC MOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

## GENERAL DESCRIPTION

The ICS8752 is a low voltage, low skew LVC MOS clock generator. With output frequencies up to 240MHz, the ICS8752 is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS8752 contains frequency configurable outputs and an external feedback input for regenerating clocks with “zero delay”.

Dual clock inputs, CLK0 and CLK1, support redundant clock applications. The CLK\_SEL input determines which reference clock is used. The output divider values of Bank A and B are controlled by the DIV\_SELA0:1, and DIV SELB0:1, respectively.

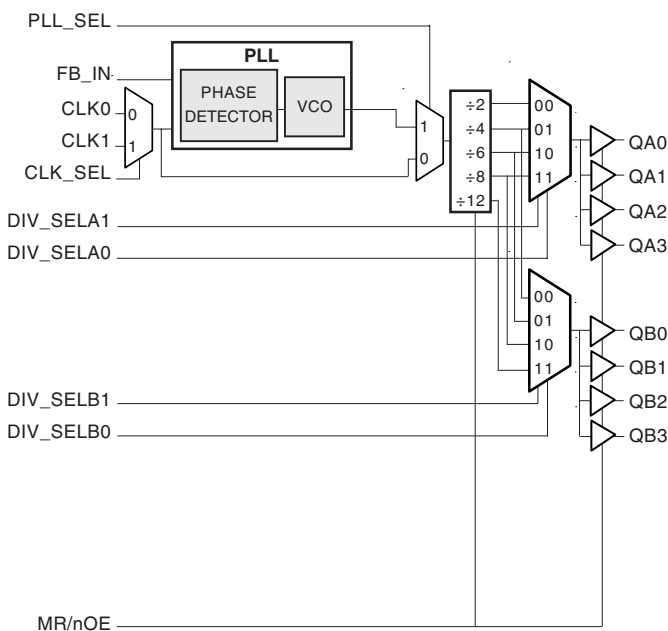
For test and system debug purposes, the PLL\_SEL input allows the PLL to be bypassed. When HIGH, the MR/nOE input resets the internal dividers and forces the outputs to the high impedance state.

The low impedance LVC MOS outputs of the ICS8752 are designed to drive terminated transmission lines. The effective fanout of each output can be doubled by utilizing the ability of each output to drive two series terminated transmission lines.

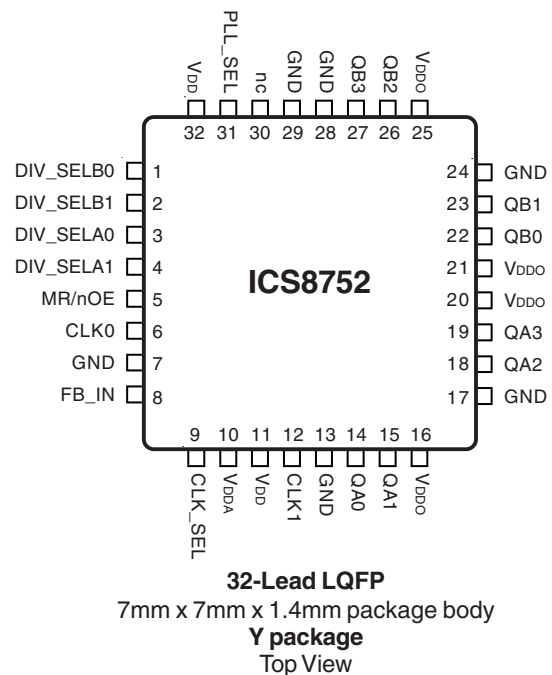
## FEATURES

- Fully integrated PLL
- Eight LVC MOS outputs, 7 $\Omega$  typical output impedance
- Selectable LVC MOS CLK0 or CLK1 inputs for redundant clock applications
- Input/Output frequency range: 18.33MHz to 240MHz at  $V_{CC} = 3.3V \pm 5\%$
- VCO range: 220MHz to 480MHz
- External feedback for “zero delay” clock regeneration
- Cycle-to-cycle jitter: 75ps (maximum), (all outputs are the same frequency)
- Output skew: 100ps (maximum)
- Bank skew: 55ps (maximum)
- Full 3.3V or 2.5V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT





# ICS8752

## Low SKEW, 1-TO-8

### LVC MOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

TABLE 1. PIN DESCRIPTIONS

| Number                | Name                 | Type   |          | Description                                                                                                                                                                                 |
|-----------------------|----------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2                  | DIV_SELB0, DIV_SELB1 | Input  | Pulldown | Determines output divider values for Bank B as described in Table 3. LVC MOS / LV TTL interface levels.                                                                                     |
| 3, 4                  | DIV_SELA0, DIV_SELA1 | Input  | Pulldown | Determines output divider values for Bank A as described in Table 3. LVC MOS / LV TTL interface levels.                                                                                     |
| 5                     | MR/nOE               | Input  | Pulldown | When logic HIGH, the internal dividers are reset and the outputs are disabled. When logic LOW, the master reset is disabled and the outputs are enabled. LVC MOS / LV TTL interface levels. |
| 6                     | CLK0                 | Input  | Pulldown | Clock input. LVC MOS / LV TTL interface levels.                                                                                                                                             |
| 7, 13, 17, 24, 28, 29 | GND                  | Power  |          | Power supply ground.                                                                                                                                                                        |
| 8                     | FB_IN                | Input  | Pulldown | Feedback input to phase detector for generating clocks with "zero delay". LVC MOS / LV TTL interface levels.                                                                                |
| 9                     | CLK_SEL              | Input  | Pulldown | Clock select input. Selects between CLK0 or CLK1 as phase detector reference. When LOW, selects CLK0. When HIGH, selects CLK1. LVC MOS / LV TTL interface levels.                           |
| 10                    | V <sub>DDA</sub>     | Power  |          | Analog supply pin.                                                                                                                                                                          |
| 11, 32                | V <sub>DD</sub>      | Power  |          | Core supply pins.                                                                                                                                                                           |
| 12                    | CLK1                 | Input  | Pulldown | Clock input. LVC MOS / LV TTL interface levels.                                                                                                                                             |
| 14, 15, 18, 19        | QA0, QA1, QA2, QA3   | Output |          | Bank A clock outputs. 7Ω typical output impedance. LVC MOS / LV TTL interface levels.                                                                                                       |
| 16, 20, 21, 25        | V <sub>DDO</sub>     | Power  |          | Output supply pins.                                                                                                                                                                         |
| 22, 23, 26, 27        | QB0, QB1, QB2, QB3   | Output |          | Bank B clock outputs. 7Ω typical output impedance. LVC MOS / LV TTL interface levels.                                                                                                       |
| 30                    | nc                   | Unused |          | No connect.                                                                                                                                                                                 |
| 31                    | PLL_SEL              | Input  | Pullup   | Selects between the PLL and CLK0 or CLK1 as the input to the dividers. When HIGH selects PLL. When LOW selects CLK0 or CLK1. LVC MOS / LV TTL interface levels.                             |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol                | Parameter                                  | Test Conditions                                                | Minimum | Typical | Maximum | Units |
|-----------------------|--------------------------------------------|----------------------------------------------------------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                          |                                                                |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                      |                                                                |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                    |                                                                |         | 51      |         | kΩ    |
| C <sub>PD</sub>       | Power Dissipation Capacitance (per output) | V <sub>DDA</sub> , V <sub>DD</sub> , V <sub>DDO</sub> = 3.465V |         | 23      |         | pF    |
| R <sub>OUT</sub>      | Output Impedance                           |                                                                |         | 7       |         | Ω     |



# ICS8752

Low SKEW, 1-to-8  
LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

TABLE 3. CONTROL INPUT FUNCTION TABLE

| Inputs |         |         |           |           |           |           | Outputs         |                 |
|--------|---------|---------|-----------|-----------|-----------|-----------|-----------------|-----------------|
| MR/nOE | PLL_SEL | CLK_SEL | DIV_SELA1 | DIV_SELA0 | DIV_SELB1 | DIV_SELB0 | QA <sub>x</sub> | QB <sub>x</sub> |
| 1      | X       | X       | X         | X         | X         | X         | Hi-Z            | Hi-Z            |
| 0      | 1       | X       | 0         | 0         | 0         | 0         | fVCO/2          | fVCO/4          |
| 0      | 1       | X       | 0         | 1         | 0         | 1         | fVCO/4          | fVCO/6          |
| 0      | 1       | X       | 1         | 0         | 1         | 0         | fVCO/6          | fVCO/8          |
| 0      | 1       | X       | 1         | 1         | 1         | 1         | fVCO/8          | fVCO/12         |
| 0      | 0       | 0       | 0         | 0         | 0         | 0         | fCLK0/2         | fCLK0/4         |
| 0      | 0       | 0       | 0         | 1         | 0         | 1         | fCLK0/4         | fCLK0/6         |
| 0      | 0       | 0       | 1         | 0         | 1         | 0         | fCLK0/6         | fCLK0/8         |
| 0      | 0       | 0       | 1         | 1         | 1         | 1         | fCLK0/8         | fCLK0/12        |
| 0      | 0       | 1       | 0         | 0         | 0         | 0         | fCLK1/2         | fCLK1/4         |
| 0      | 0       | 1       | 0         | 1         | 0         | 1         | fCLK1/4         | fCLK1/6         |
| 0      | 0       | 1       | 1         | 0         | 1         | 0         | fCLK1/6         | fCLK1/8         |
| 0      | 0       | 1       | 1         | 1         | 1         | 1         | fCLK1/8         | fCLK1/12        |

NOTE: For normal operation, MR/nOE is LOW. When MR/nOE is HIGH, all outputs are disabled.

TABLE 4A. QA OUTPUT FREQUENCY w/FB\_IN = QB

| Inputs |            |            |                                 |                           |         |            |            |                        | Outputs                |
|--------|------------|------------|---------------------------------|---------------------------|---------|------------|------------|------------------------|------------------------|
| FB_IN  | DIV_SEL B1 | DIV_SEL B0 | QB Output Divider Mode (NOTE 2) | CLK0, CLK1 (MHz) (NOTE 1) |         | DIV_SEL A1 | DIV_SEL A0 | QA Output Divider Mode | QA Multiplier (NOTE 2) |
|        |            |            |                                 | Minimum                   | Maximum |            |            |                        |                        |
| QB     | 0          | 0          | ÷4                              | 55                        | 120     | 0          | 0          | ÷2                     | 2                      |
|        |            |            |                                 |                           |         | 0          | 1          | ÷4                     | 1                      |
|        |            |            |                                 |                           |         | 1          | 0          | ÷6                     | 0.667                  |
|        |            |            |                                 |                           |         | 1          | 1          | ÷8                     | 0.5                    |
| QB     | 0          | 1          | ÷6                              | 36.66                     | 80      | 0          | 0          | ÷2                     | 3                      |
|        |            |            |                                 |                           |         | 0          | 1          | ÷4                     | 1.5                    |
|        |            |            |                                 |                           |         | 1          | 0          | ÷6                     | 1                      |
|        |            |            |                                 |                           |         | 1          | 1          | ÷8                     | 0.75                   |
| QB     | 1          | 0          | ÷8                              | 27.5                      | 60      | 0          | 0          | ÷2                     | 4                      |
|        |            |            |                                 |                           |         | 0          | 1          | ÷4                     | 2                      |
|        |            |            |                                 |                           |         | 1          | 0          | ÷6                     | 1.33                   |
|        |            |            |                                 |                           |         | 1          | 1          | ÷8                     | 1                      |
| QB     | 1          | 1          | ÷12                             | 18.33                     | 40      | 0          | 1          | ÷2                     | 6                      |
|        |            |            |                                 |                           |         | 0          | 1          | ÷4                     | 3                      |
|        |            |            |                                 |                           |         | 1          | 0          | ÷6                     | 2                      |
|        |            |            |                                 |                           |         | 1          | 1          | ÷8                     | 1.5                    |

NOTE 1: VCO frequency range is 220MHz to 480MHz.

NOTE 2: QA output frequency equal to CLK<sub>x</sub> frequency times the multiplier;

QB output frequency equal to CLK<sub>x</sub>.



# ICS8752

Low SKEW, 1-TO-8  
LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

TABLE 4B. QB OUTPUT FREQUENCY W/FB\_IN = QA

| Inputs |                       |                       |                                 |                           |              |                       |                       |                        | Outputs                |
|--------|-----------------------|-----------------------|---------------------------------|---------------------------|--------------|-----------------------|-----------------------|------------------------|------------------------|
| FB_IN  | DIV_SEL <sub>A1</sub> | DIV_SEL <sub>A0</sub> | QA Output Divider Mode (NOTE 2) | CLK0, CLK1 (MHz) (NOTE 1) |              | DIV_SEL <sub>B1</sub> | DIV_SEL <sub>B0</sub> | QB Output Divider Mode | QB Multiplier (NOTE 2) |
|        |                       |                       |                                 | Minimum                   | Maximum      |                       |                       |                        |                        |
| QA     | 0                     | 0                     | ÷2                              | 110                       | 240 (NOTE 3) | 0                     | 0                     | ÷4                     | 0.5                    |
|        |                       |                       |                                 |                           |              | 0                     | 1                     | ÷6                     | 0.333                  |
|        |                       |                       |                                 |                           |              | 1                     | 0                     | ÷8                     | 0.25                   |
|        |                       |                       |                                 |                           |              | 1                     | 1                     | ÷12                    | 0.167                  |
| QA     | 0                     | 1                     | ÷4                              | 55                        | 120          | 0                     | 0                     | ÷4                     | 1                      |
|        |                       |                       |                                 |                           |              | 0                     | 1                     | ÷6                     | 0.667                  |
|        |                       |                       |                                 |                           |              | 1                     | 0                     | ÷8                     | 0.5                    |
|        |                       |                       |                                 |                           |              | 1                     | 1                     | ÷12                    | 0.333                  |
| QA     | 1                     | 0                     | ÷6                              | 36.66                     | 80           | 0                     | 0                     | ÷4                     | 1.5                    |
|        |                       |                       |                                 |                           |              | 0                     | 1                     | ÷6                     | 1                      |
|        |                       |                       |                                 |                           |              | 1                     | 0                     | ÷8                     | 0.75                   |
|        |                       |                       |                                 |                           |              | 1                     | 1                     | ÷12                    | 0.5                    |
| QA     | 1                     | 1                     | ÷8                              | 27.5                      | 60           | 0                     | 1                     | ÷4                     | 2                      |
|        |                       |                       |                                 |                           |              | 0                     | 1                     | ÷6                     | 1.333                  |
|        |                       |                       |                                 |                           |              | 1                     | 0                     | ÷8                     | 1                      |
|        |                       |                       |                                 |                           |              | 1                     | 1                     | ÷12                    | 0.667                  |

NOTE 1: VCO frequency range is 220MHz to 480MHz.

NOTE 2: QB output frequency equal to CLKx frequency times the multiplier;

QA output frequency equal to CLKx.

NOTE 3: Maximum frequency of 240MHz valid for  $V_{CC} = 3.3V \pm 5\%$  only.



# ICS8752

## LOW SKEW, 1-TO-8

### LVC MOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

#### ABSOLUTE MAXIMUM RATINGS

|                                          |                           |
|------------------------------------------|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfm)          |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 5A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         |         | 105     | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |         |         | 15      | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         |         | 20      | mA    |

**TABLE 5B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         |         | 100     | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |         |         | 15      | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         |         | 20      | mA    |



# ICS8752

## Low SKEW, 1-TO-8

### LVC MOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

**TABLE 5B. LVC MOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter                   |                                                          | Test Conditions                            | Minimum | Typical | Maximum        | Units   |
|----------|-----------------------------|----------------------------------------------------------|--------------------------------------------|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage          |                                                          | $V_{DD} = 3.3V$                            | 2       |         | $V_{DD} + 0.3$ | V       |
|          |                             |                                                          | $V_{DD} = 2.5V$                            | 1.7     |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage           |                                                          | $V_{DD} = 3.3V$                            | -0.3    |         | 0.8            | V       |
|          |                             |                                                          | $V_{DD} = 2.5V$                            | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current          | DIV_SELx0, DIV_SELx1, CLK0, CLK1, FB_IN, CLK_SEL, MR/nOE | $V_{DD} = V_{IN} = 3.465V$ or 2.625V       |         |         | 150            | $\mu A$ |
|          |                             | PLL_SEL                                                  | $V_{DD} = V_{IN} = 3.465V$ or 2.625V       |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current           | DIV_SELx0, DIV_SELx1, CLK0, CLK1, FB_IN, CLK_SEL, MR/nOE | $V_{DD} = 3.465V$ or 2.625V, $V_{IN} = 0V$ | -5      |         |                | $\mu A$ |
|          |                             | PLL_SEL                                                  | $V_{DD} = 3.465V$ or 2.625V, $V_{IN} = 0V$ | -150    |         |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 |                                                          | $V_{DDO} = V_{IN} = 3.465V$                | 2.6     |         |                | V       |
|          |                             |                                                          | $V_{DDO} = V_{IN} = 2.625V$                | 1.8     |         |                | V       |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |                                                          |                                            |         |         | 0.5            | V       |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section, "Output Load Test Circuit" diagrams.

**TABLE 6A. PLL INPUT REFERENCE CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                                                                                                                | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------------------------------------------------------------------------------------------|-----------------|---------|---------|---------|-------|
| $f_{REF}$ | Input Reference Frequency<br>NOTE: Input reference frequency is limited by the divider selection and the VCO lock range. |                 | 20      |         | 240     | MHz   |

**TABLE 6B. PLL INPUT REFERENCE CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                                                                                                                | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------------------------------------------------------------------------------------------|-----------------|---------|---------|---------|-------|
| $f_{REF}$ | Input Reference Frequency<br>NOTE: Input reference frequency is limited by the divider selection and the VCO lock range. |                 | 20      |         | 120     | MHz   |



# ICS8752

## Low SKEW, 1-TO-8 LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

**TABLE 7A. AC CHARACTERISTICS,**  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

| Symbol         | Parameter                        |                                             | Test Conditions                           | Minimum | Typical | Maximum | Units |
|----------------|----------------------------------|---------------------------------------------|-------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$      | Output Frequency (PLL Mode)      |                                             | $\div 2$                                  | 110     |         | 240     | MHz   |
|                |                                  |                                             | $\div 4$                                  | 55      |         | 120     | MHz   |
|                |                                  |                                             | $\div 6$                                  | 36.67   |         | 80      | MHz   |
|                |                                  |                                             | $\div 8$                                  | 27.5    |         | 60      | MHz   |
|                |                                  |                                             | $\div 12$                                 | 18.33   |         | 40      | MHz   |
| $f_{VCO}$      | PLL VCO Lock Range               |                                             |                                           | 220     |         | 480     | MHz   |
| $t(\emptyset)$ | Static Phase Offset; NOTE 1      |                                             | $f_{VCO} = 400MHz$ ,<br>Feedback $\div 8$ | -30     | 70      | 170     | ps    |
| $t_{sk}(b)$    | Bank Skew; NOTE 2, 4             |                                             | Measured on rising edge<br>at $V_{DDO}/2$ |         |         | 55      | ps    |
| $t_{sk}(o)$    | Output Skew; NOTE 3, 4           |                                             | Measured on rising edge<br>at $V_{DDO}/2$ |         |         | 100     | ps    |
| $f_{jit}(cc)$  | Cycle-to-Cycle<br>Jitter; NOTE 4 | Different Frequencies<br>on Different Banks |                                           |         |         | 400     | ps    |
|                |                                  | All Outputs at<br>Same Frequency            |                                           |         |         | 75      | ps    |
| $t_L$          | PLL Lock Time                    |                                             |                                           |         |         | 1       | mS    |
| $t_R / t_F$    | Output Rise/Fall Time            |                                             | 20% to 80%                                | 400     |         | 950     | ps    |
| odc            | Output Duty Cycle                |                                             |                                           | 47      | 50      | 53      | %     |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Defined as the time difference between the input clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



# ICS8752

## Low SKEW, 1-TO-8

### LVC MOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

**TABLE 7B. AC CHARACTERISTICS,**  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

| Symbol         | Parameter                     | Test Conditions                             | Minimum | Typical | Maximum | Units |
|----------------|-------------------------------|---------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$      | Output Frequency (PLL Mode)   | $\div 2$                                    | 110     |         | 240     | MHz   |
|                |                               | $\div 4$                                    | 55      |         | 120     | MHz   |
|                |                               | $\div 6$                                    | 36.67   |         | 80      | MHz   |
|                |                               | $\div 8$                                    | 27.5    |         | 60      | MHz   |
|                |                               | $\div 12$                                   | 18.33   |         | 40      | MHz   |
| $f_{VCO}$      | PLL VCO Lock Range            |                                             | 220     |         | 480     | MHz   |
| $t(\emptyset)$ | Static Phase Offset; NOTE 1   | $f_{VCO} = 400MHz$<br>Feedback $\div 8$     | -90     | 50      | 190     | ps    |
| $t_{sk}(b)$    | Bank Skew; NOTE 2, 4          | Measured on rising edge<br>at $V_{DDO}/2$   |         |         | 55      | ps    |
| $t_{sk}(o)$    | Output Skew; NOTE 3, 4        | Measured on rising edge<br>at $V_{DDO}/2$   |         |         | 90      | ps    |
| $f_{jit}(cc)$  | Cycle-to-Cycle Jitter; NOTE 4 | Different Frequencies<br>on Different Banks |         |         | 400     | ps    |
|                |                               | All Outputs at<br>Same Frequency            |         |         | 75      | ps    |
| $t_L$          | PLL Lock Time                 |                                             |         |         | 1       | mS    |
| $t_R / t_F$    | Output Rise/Fall Time         | 20% to 80%                                  | 400     |         | 950     | ps    |
| odc            | Output Duty Cycle             |                                             | 45      | 50      | 55      | %     |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Defined as the time difference between the input clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

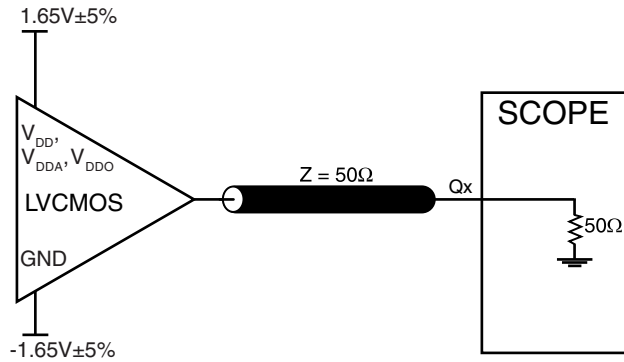
Measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

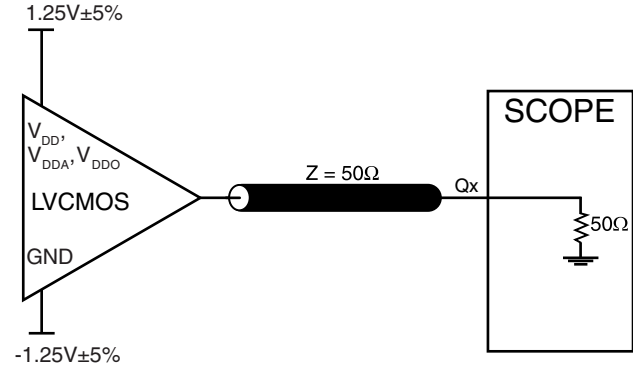




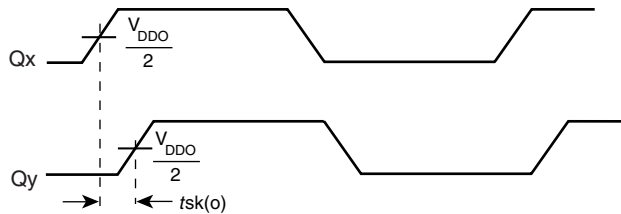
## PARAMETER MEASUREMENT INFORMATION



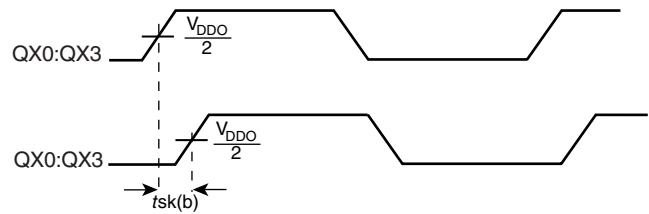
**3.3V OUTPUT LOAD AC TEST CIRCUIT**  
(Where X denotes outputs in the same Bank)



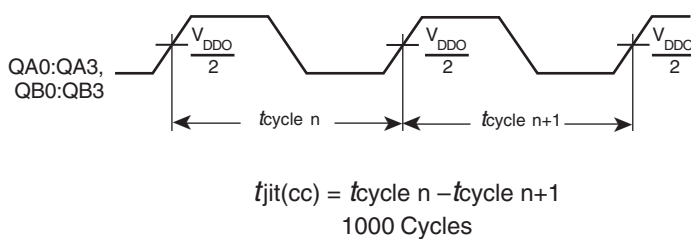
**2.5V OUTPUT LOAD AC TEST CIRCUIT**



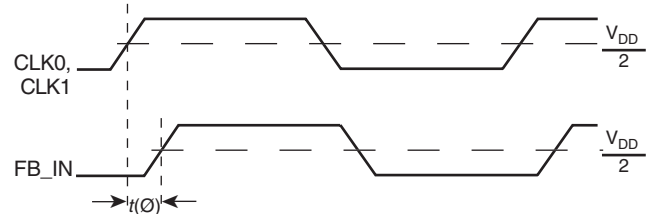
**OUTPUT SKEW**



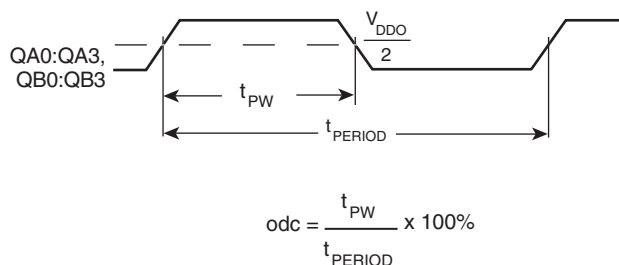
**BANK SKEW**



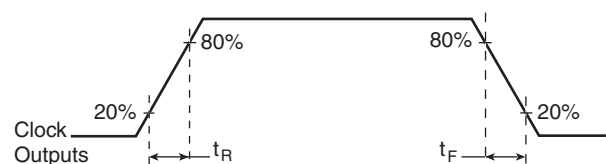
**CYCLE-TO-CYCLE JITTER**



**STATIC PHASE OFFSET**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**OUTPUT RISE/FALL TIME**



## APPLICATION INFORMATION

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### OUTPUTS:

##### LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

---

---

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|----------------------------------------------------|----------|----------|----------|
|                                                    | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

#### TRANSISTOR COUNT

The transistor count for ICS8752 is: 1546



# ICS8752

Low SKEW, 1-TO-8  
LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

## PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

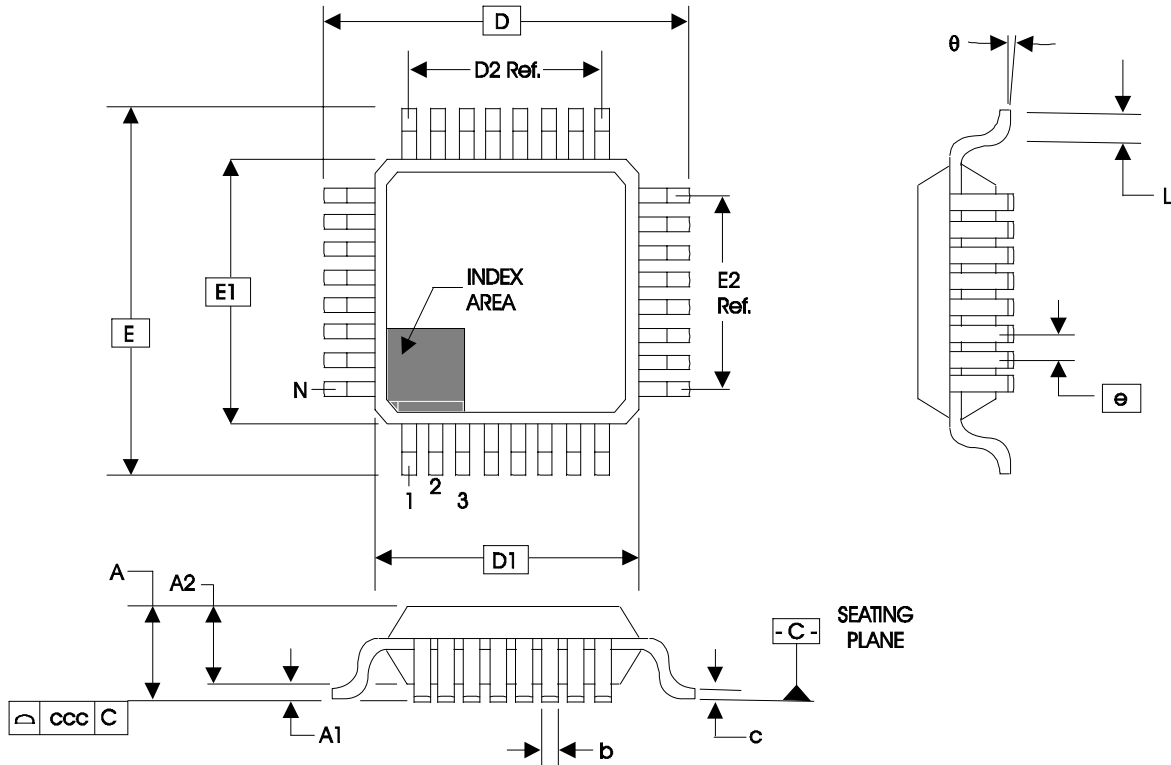


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--------------------------------------------------|------------|---------|---------|
| SYMBOL                                           | BBA        |         |         |
|                                                  | MINIMUM    | NOMINAL | MAXIMUM |
| N                                                | 32         |         |         |
| A                                                | --         | --      | 1.60    |
| A1                                               | 0.05       | --      | 0.15    |
| A2                                               | 1.35       | 1.40    | 1.45    |
| b                                                | 0.30       | 0.37    | 0.45    |
| c                                                | 0.09       | --      | 0.20    |
| D                                                | 9.00 BASIC |         |         |
| D1                                               | 7.00 BASIC |         |         |
| D2                                               | 5.60 Ref.  |         |         |
| E                                                | 9.00 BASIC |         |         |
| E1                                               | 7.00 BASIC |         |         |
| E2                                               | 5.60 Ref.  |         |         |
| e                                                | 0.80 BASIC |         |         |
| L                                                | 0.45       | 0.60    | 0.75    |
| θ                                                | 0°         | --      | 7°      |
| ccc                                              | --         | --      | 0.10    |

Reference Document: JEDEC Publication 95, MS-026



# ICS8752

LOW SKEW, 1-TO-8  
LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking     | Package                  | Shipping Packaging | Temperature |
|-------------------|-------------|--------------------------|--------------------|-------------|
| 8752CY            | ICS8752CY   | 32 Lead LQFP             | tray               | 0°C to 70°C |
| 8752CYT           | ICS8752CY   | 32 Lead LQFP             | 1000 tape & reel   | 0°C to 70°C |
| 8752CYLF          | ICS8752CYLF | 32 Lead "Lead-Free" LQFP | tray               | 0°C to 70°C |
| 8752CYLFT         | ICS8752CYLF | 32 Lead "Lead-Free" LQFP | 1000 tape & reel   | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology, Inc. (IDT) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.



**ICS8752**  
LOW SKEW, 1-TO-8  
LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

| REVISION HISTORY SHEET |          |      |                                                                                                            |          |
|------------------------|----------|------|------------------------------------------------------------------------------------------------------------|----------|
| Rev                    | Table    | Page | Description of Change                                                                                      | Date     |
| A                      | T1       | 2    | Pin Descriptions Table. Revised MR/nOE description.                                                        | 8/19/02  |
| B                      | T2<br>T9 | 1    | Features Section - delete bullet, "Industrial temperature available upon request." Added Lead-Free bullet. | 3/31/05  |
|                        |          | 2    | Pin Characteristics table - changed C <sub>IN</sub> 4pF max. to 4pF typical.                               |          |
|                        |          | 12   | Ordering Information Table -added Lead-Free part number and note.<br>Updated data sheet format.            |          |
| B                      | T1       | 2    | Pin Description Table - correct Pin 5, MR/nOE.                                                             | 5/2/05   |
| B                      | T9       | 10   | Added <i>Recommendations for Unused Input and Output Pins.</i>                                             | 10/19/05 |
|                        |          | 12   | Ordering Information Table - added lead-free marking.                                                      |          |
| C                      | T9       | 12   | Updated datasheet's header/footer with IDT from ICS.                                                       | 7/2/10   |
|                        |          | 14   | Removed ""ICS"" prefix from Part/Order Number column.<br>Added Contact Page.                               |          |



**ICS8752**  
Low SKEW, 1-TO-8  
LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

---

**We've Got Your Timing Solution.**



6024 Silver Creek Valley Road  
San Jose, CA 95138

**Sales**  
800-345-7015 (inside USA)  
+408-284-8200 (outside USA)  
Fax: 408-284-2775

**Tech Support**  
netcom@idt.com