



## 290 x 290 3.5Gb/s Crosspoint Switch with Trace Equalization and Output De-emphasis

### Key Features

- 290 x 290 crosspoint switch architecture supporting broadcast and multi-cast modes
- Supports all data rates up to 3.5Gb/s
- Low power consumption: 34.25W typical (all channels active)
- Sophisticated, dynamic on-chip power management control
- Independent, programmable input trace equalization to reduce deterministic jitter (ISI)
- Independent, programmable output de-emphasis for driving long board traces
- High-speed, video-optimized control for multi-format applications
- Built-in system test features with on-chip PRBS generators and analyzers
- 2.5V analog core voltage, 1.8V digital core voltage
- Input and output voltages support either 1.2V, 1.8V or 2.5V CML
- JTAG-controlled boundary scan
- Selectable parallel/serial host interface
- 50mm x 50mm BGA (2377 ball)
- Operating temperature range: 0°C to +85°C
- RoHS compliant

### Applications

Large m x n cascaded routers/switch fabrics for:

- Professional broadcast applications
- Enterprise and carrier applications
- High-speed automated test equipment
- 10GbE and InfiniBand networks

### Description

The GX3290 is a low-power, high-speed 290 x 290 crosspoint switch, with robust signal conditioning circuits for driving and receiving high-speed signals through backplanes.

The device typically consumes 34.25W of power with all channels operational, and features sophisticated, dynamically scalable power management. Unused portions of the core are automatically turned off without affecting the operation of the remaining channels.

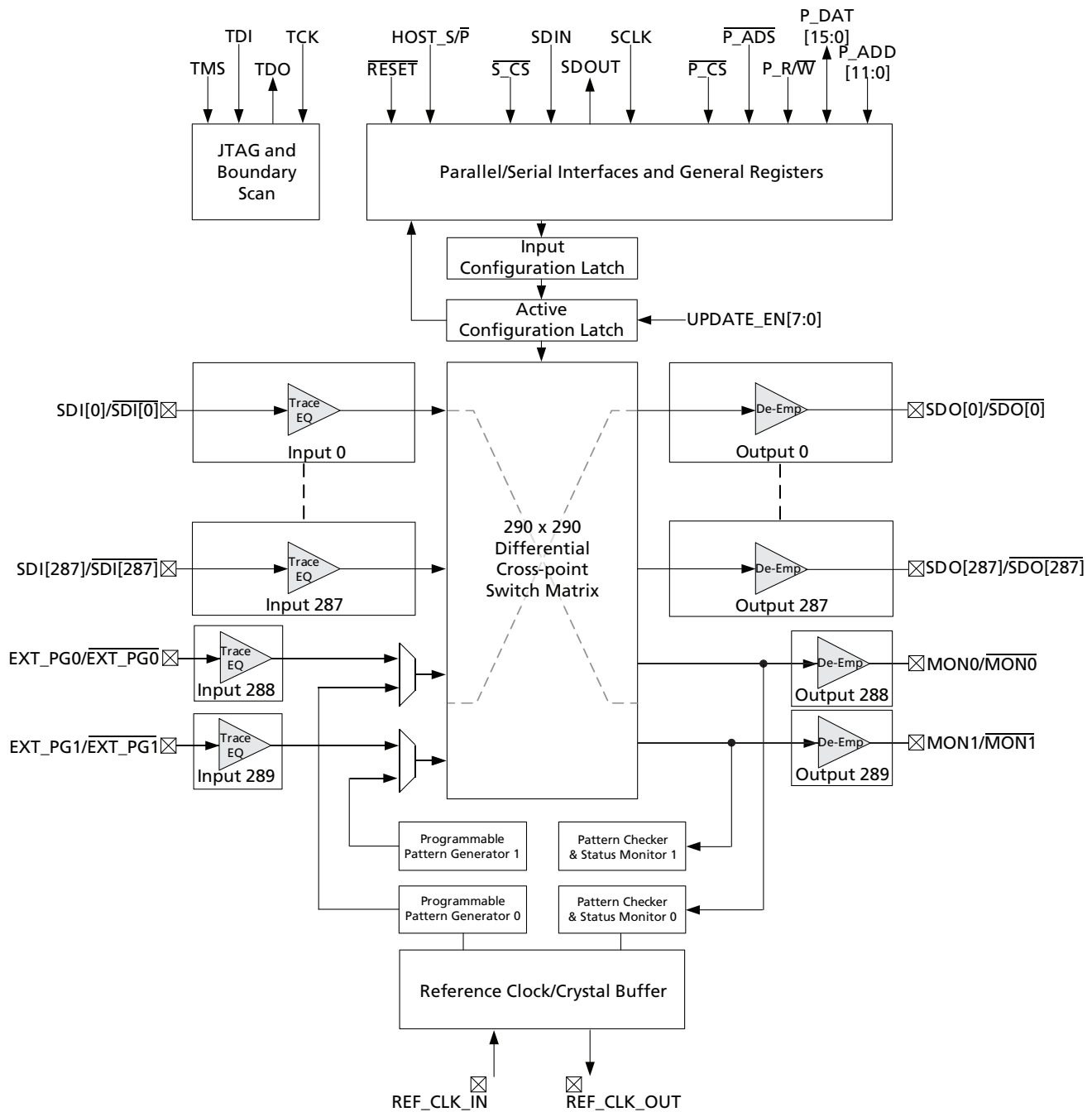
The signal conditioning features of the GX3290 include per-input programmable equalization and per-output programmable de-emphasis. The input equalizer removes ISI jitter—typically caused by PCB trace losses—by opening the input data eye in applications where long PCB traces are used. There are four settings available for the input equalizer, allowing flexibility in adjusting the equalization level on a per-input basis.

Output de-emphasis capability provides a boost of the high-frequency content of the output signal, such that the data eye remains open after passing through a long interconnect of PCB traces and connectors. There are four de-emphasis settings that can be enabled on a per-output basis.

Two integrated programmable pattern generators, and two pattern checkers are provided to assist in system test and configuration.

The pattern generators can each be routed to any output of the device without impacting the normal operation of any other channel. Any input can be routed to each of the pattern checkers.

The chip features eight independent strobe inputs, UPDATE\_EN[7:0], which are used to determine the timing of the output updates. Any output can be linked to any strobe.



**GX3290 Functional Block Diagram**

## Revision History

| Version | ECO    | PCN | Date           | Changes and/or Modifications                                                                                                                                                                                                                                                                                                                             |
|---------|--------|-----|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2       | 011719 | –   | March 2013     | Corrected second bullet in <a href="#">Section 4.7.1</a> , and added a note to <a href="#">Section 4.4</a> .                                                                                                                                                                                                                                             |
| 1       | 158372 | –   | October 2012   | Included ESD Voltage Sensitivity in <a href="#">Table 2-1</a> . Modifications to <a href="#">Table 4-18</a> and <a href="#">Section 4.12.2</a> to include Auto-Increment Timing and functionality. Updates to <a href="#">Appendix - Relevant Documentation</a> with clear reference to correct documents. Converted document to Final Data Sheet.       |
| 0       | 157403 | –   | February 2012  | Converted document to Preliminary Data Sheet. Updates throughout.                                                                                                                                                                                                                                                                                        |
| F       | 157275 | –   | November 2011  | Minor updates through entire document.                                                                                                                                                                                                                                                                                                                   |
| E       | 156342 | –   | July 2011      | Updates throughout entire document. Removed Configuration and Status Registers (transferred to document <a href="#">Crosspoint (GX3290 and family) Reference Manual (for CSRs)</a> ).                                                                                                                                                                    |
| D       | 154735 | –   | September 2010 | Changed maximum data rate to 3.5Gb/s. Updates to <a href="#">Figure 4-10</a> and <a href="#">Figure 4-11</a> , <a href="#">4.12.2 Serial Host Interface Specifications</a> , <a href="#">Package Dimensions</a> and <a href="#">Marking Diagram</a> .                                                                                                    |
| C       | 154303 | –   | July 2010      | Updates throughout entire document. Changes to <a href="#">GX3290 Ball Assignment Overview (Top View)</a> . Addition of multiple sections in <a href="#">Section 4. Detailed Description</a> . Addition of <a href="#">Ball Descriptions</a> . Changes to <a href="#">Input/Output Equivalent Circuits</a> and <a href="#">Application Information</a> . |
| B       | 153176 | –   | January 2010   | Updates to <a href="#">Table 2-3: DC Electrical Characteristics</a> . Updates to <a href="#">Section 4.12 Host Interface</a> . Updates to <a href="#">Figure 1-1: GX3290 Ball Assignment Overview (Top View)</a> . Addition of <a href="#">Section 3. Input/Output Equivalent Circuits</a> .                                                             |
| A       | 152552 | –   | October 2009   | New document.                                                                                                                                                                                                                                                                                                                                            |

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# 1. Ball Out

## 1.1 Ball Assignment

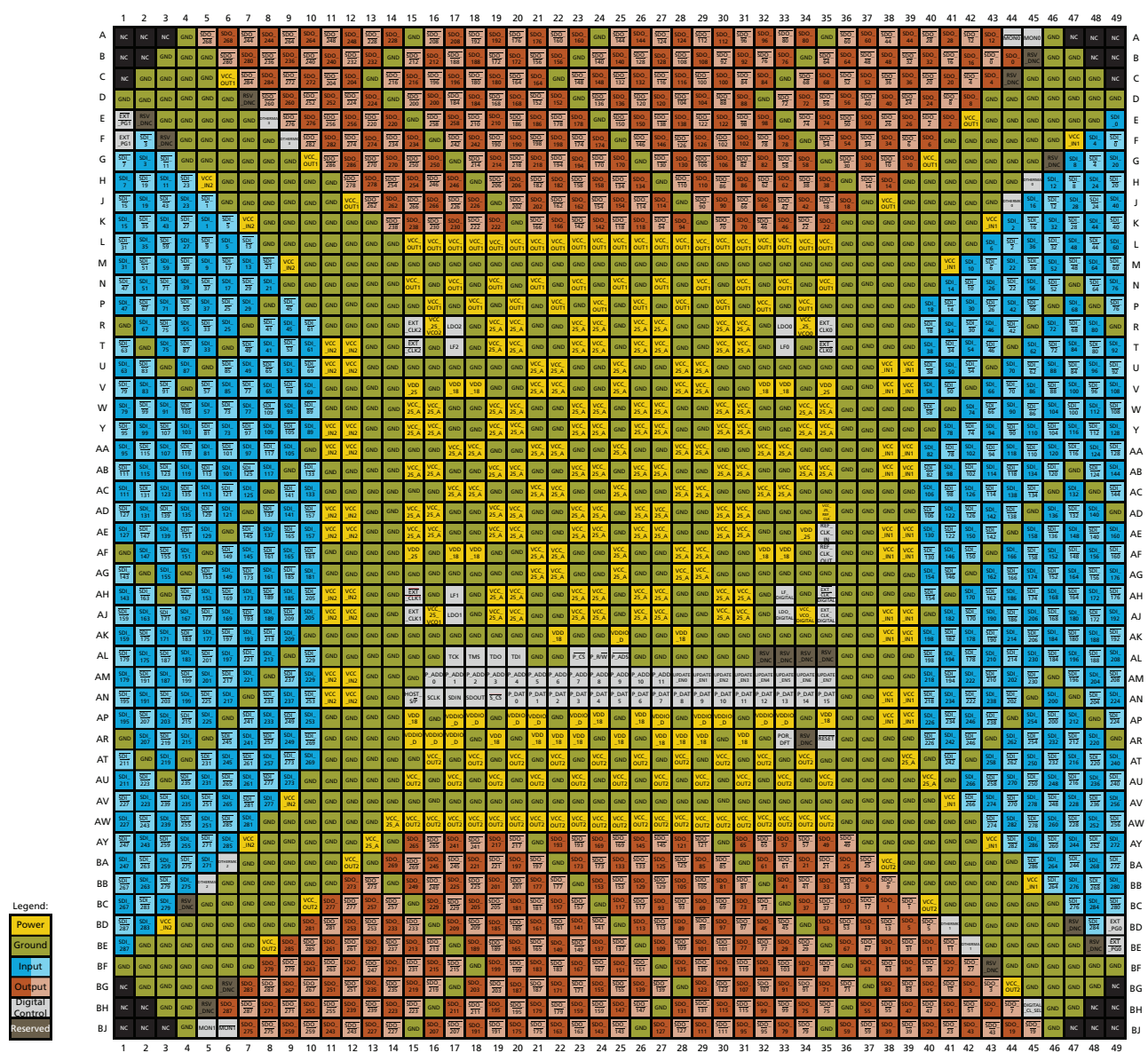


Figure 1-1: GX3290 Ball Assignment Overview (Top View)

## 1.2 Ball Descriptions

Table 1-1 shows the descriptions for selected GX3290 balls. For a comprehensive list of balls from the GX3290 Crosspoint family, please refer to [GX3290 \(and family\) Crosspoint Ball Guide](#).

**Table 1-1: Ball Descriptions**

| Ball #                        | Ball Name              | I/O | Description                                                                                                                                                                                                                      |
|-------------------------------|------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Serial Interface I/O</b>   |                        |     |                                                                                                                                                                                                                                  |
| AN16                          | SCLK                   | I   | Serial Host Interface Clock. If unused, tie to ground.                                                                                                                                                                           |
| AN17                          | SDIN                   | I   | Serial Host Interface Data Input. If unused, tie to ground.                                                                                                                                                                      |
| AN18                          | SDOUT                  | O   | Serial Host Interface Data Output. Leave NC if not used.                                                                                                                                                                         |
| AN19                          | $\overline{S\_CS}$     | I   | Serial Host Interface Chip Select. Active-LOW. Must be tied LOW when HOST_S/ $\overline{P}$ is set LOW.                                                                                                                          |
| <b>Parallel Interface I/O</b> |                        |     |                                                                                                                                                                                                                                  |
| AL23                          | $\overline{P\_CS}$     | I   | Parallel host interface chip select. Active-LOW. Must be tied LOW when HOST_S/ $\overline{P}$ is set HIGH.                                                                                                                       |
| AL24                          | P_R/ $\overline{W}$    | I   | Selects between read and write operations on the parallel host interface. HIGH = Read, LOW = Write. If unused, tie to ground.                                                                                                    |
| AL25                          | $\overline{P\_ADS}$    | I   | Address and Data Strobe. Strobe signal for latching the address and data into the chip. See <a href="#">Section 4.12.1</a> for timing information. If unused, tie to ground.                                                     |
| AM27 - AM16                   | P_ADD[11:0]            | I   | Address bus for the parallel interface. If unused, tie to ground.                                                                                                                                                                |
| AN35 - AN20                   | P_DAT[15:0]            | I/O | Bi-directional data bus for the parallel interface. If $\overline{P\_CS}$ is HIGH, these pins are configured as inputs. If unused, tie to ground.                                                                                |
| <b>General I/O</b>            |                        |     |                                                                                                                                                                                                                                  |
| AN15                          | HOST_S/ $\overline{P}$ | I   | Host Interface Select pin. Selects between serial and parallel host interfaces. Serial host interface is enabled when HIGH, parallel host interface is enabled when LOW. Must assert $\overline{RESET}$ after changing this pin. |
| AM35 - AM28                   | UPDATE_EN [7:0]        | I   | Update Strobes used to update the switch matrix configuration (see <a href="#">Section 4.5</a> ). If unused, weak pull-down to ground.                                                                                           |
| AR33                          | POR_DFT                | I   | This pin disables the Power On Reset circuitry when HIGH. Weak internal pull-down. Leave NC if not used.                                                                                                                         |
| AR35                          | $\overline{RESET}$     | I   | Active-LOW reset for entire chip (see <a href="#">Section 4.11</a> for timing details). Weak internal pull-up. Leave NC if not used.                                                                                             |
| <b>Test Interface</b>         |                        |     |                                                                                                                                                                                                                                  |
| AL17                          | TCK                    | I   | JTAG test clock. Weak pull-up if not used.                                                                                                                                                                                       |
| AL18                          | TMS                    | I   | JTAG test mode start. Weak pull-up if not used.                                                                                                                                                                                  |
| AL19                          | TDO                    | O   | JTAG test data out. Leave NC if not used.                                                                                                                                                                                        |
| AL20                          | TDI                    | I   | JTAG test data in. Weak pull-up if not used.                                                                                                                                                                                     |

**Table 1-1: Ball Descriptions (Continued)**

| Ball #                    | Ball Name                             | I/O | Description                                                                                                                                                                                  |
|---------------------------|---------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Filtering</b>          |                                       |     |                                                                                                                                                                                              |
| R17                       | LDO2                                  | —   | LDO filter capacitor for VCO_2. Connect through a 220nF capacitor to ground. See <a href="#">Figure 3-4</a> for configuration.                                                               |
| R33                       | LDO0                                  | —   | LDO filter capacitor for VCO_0. Connect through a 220nF capacitor to ground. See <a href="#">Figure 3-4</a> for configuration.                                                               |
| T17                       | LF2                                   | —   | PLL loop filter capacitor for VCO_2. See <a href="#">Figure 3-4</a> for configuration. Leave NC if not used.                                                                                 |
| T33                       | LF0                                   | —   | PLL loop filter capacitor for VCO_0. See <a href="#">Figure 3-4</a> for configuration. Leave NC if not used.                                                                                 |
| AH17                      | LF1                                   | —   | PLL loop filter capacitor for VCO_1. See <a href="#">Figure 3-4</a> for configuration. Leave NC if not used.                                                                                 |
| AH33                      | LF_DIGITAL                            | —   | PLL loop filter capacitor for VCO_DIGITAL. Connect through a 47nF capacitor to ground. See <a href="#">Figure 3-4</a> for configuration.                                                     |
| AJ17                      | LDO1                                  | —   | LDO filter capacitor for VCO_1. Connect through a 220nF capacitor to ground. See <a href="#">Figure 3-4</a> for configuration.                                                               |
| AJ33                      | LDO_DIGITAL                           | —   | LDO filter capacitor for VCO_DIGITAL. Connect through a 220nF capacitor to ground. See <a href="#">Figure 3-4</a> for configuration.                                                         |
| <b>Crystal Oscillator</b> |                                       |     |                                                                                                                                                                                              |
| AE35                      | REF_CLK_IN                            | —   | Connect a 27MHz crystal between this ball and REF_CLK_OUT (or connect to a 27MHz clock source). See <a href="#">Section 4.9</a> and <a href="#">Figure 3-6</a> .                             |
| AF35                      | REF_CLK_OUT                           | —   | Connect a 27MHz crystal between this ball and REF_CLK_IN (if a clock source is used, leave floating). See <a href="#">Section 4.9</a> and <a href="#">Figure 3-6</a> . Leave NC if not used. |
| <b>External Clocks</b>    |                                       |     |                                                                                                                                                                                              |
| R15                       | EXT_CLK2                              | I   | External CML clock for Pattern Generator 1 (true). Leave NC if not used.                                                                                                                     |
| R35                       | EXT_CLK0                              | I   | External CML clock for Pattern Checker 0 (true). Leave NC if not used.                                                                                                                       |
| T15                       | $\overline{\text{EXT\_CLK2}}$         | I   | External CML clock for Pattern Generator 1 (complement). Leave NC if not used.                                                                                                               |
| T35                       | $\overline{\text{EXT\_CLK0}}$         | I   | External CML clock for Pattern Checker 0 (complement). Leave NC if not used.                                                                                                                 |
| AH15                      | $\overline{\text{EXT\_CLK1}}$         | I   | External CML clock for Pattern Checker 1 (complement). Leave NC if not used.                                                                                                                 |
| AH35                      | $\overline{\text{EXT\_CLK\_DIGITAL}}$ | I   | External CML clock for Pattern Transmitter 0/Digital Core (complement). Leave NC if not used.                                                                                                |
| AJ15                      | EXT_CLK1                              | I   | External CML clock for Pattern Checker 1 (true). Leave NC if not used.                                                                                                                       |
| AJ35                      | EXT_CLK_DIGITAL                       | I   | External CML clock for Pattern Transmitter 0/Digital Core (true). Leave NC if not used.                                                                                                      |
| BH45                      | DIGITAL_CL_SEL                        | I   | Clock select between external clock source (EXT_CLK_DIGITAL) and internal VCO (VCO_DIGITAL). This pin has a weak internal pull-up, and should be pulled LOW to use an external clock.        |

**Table 1-1: Ball Descriptions (Continued)**

| Ball #                                                                                                            | Ball Name | I/O | Description                                                                            |
|-------------------------------------------------------------------------------------------------------------------|-----------|-----|----------------------------------------------------------------------------------------|
| <b>Temperature Sensors</b>                                                                                        |           |     |                                                                                        |
| E8                                                                                                                | DTHERMA3  | —   | Thermometer 3 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| F9                                                                                                                | DTHERMK3  | —   | Thermometer 3 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| H45                                                                                                               | DTHERMA0  | —   | Thermometer 0 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| J44                                                                                                               | DTHERMK0  | —   | Thermometer 0 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| BA6                                                                                                               | DTHERMK2  | —   | Thermometer 2 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| BB5                                                                                                               | DTHERMA2  | —   | Thermometer 2 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| BD41                                                                                                              | DTHERMK1  | —   | Thermometer 1 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| BE42                                                                                                              | DTHERMA1  | —   | Thermometer 1 diode terminals. See <a href="#">Section 4.8</a> . Leave NC if not used. |
| <b>Monitors</b>                                                                                                   |           |     |                                                                                        |
| A44                                                                                                               | MON0      | O   | Serial monitoring output 0 (complement). Leave NC if not used.                         |
| A45                                                                                                               | MON0      | O   | Serial monitoring output 0 (true). Leave NC if not used.                               |
| BJ5                                                                                                               | MON1      | O   | Serial monitoring output 1 (true). Leave NC if not used.                               |
| BJ6                                                                                                               | MON1      | O   | Serial monitoring output 1 (complement). Leave NC if not used.                         |
| <b>External Pattern Generators</b>                                                                                |           |     |                                                                                        |
| E1                                                                                                                | EXT_PG1   | I   | Serial pattern generator input 1 (complement). Leave NC if not used.                   |
| F1                                                                                                                | EXT_PG1   | I   | Serial pattern generator input 1 (true). Leave NC if not used.                         |
| BD49                                                                                                              | EXT_PG0   | I   | Serial pattern generator input 0 (true). Leave NC if not used.                         |
| BE49                                                                                                              | EXT_PG0   | I   | Serial pattern generator input 0 (complement). Leave NC if not used.                   |
| <b>Reserved - Do Not Connect</b>                                                                                  |           |     |                                                                                        |
| B45, C44, D7,<br>E2, F3, G46,<br>AL32, AL33,<br>AL34, AL35,<br>AR34, BC4,<br>BD47, BE48,<br>BF43, BG6, BH5,       | RSV_DNC   | —   | Reserved. Do not connect.                                                              |
| <b>SDI/SDO</b>                                                                                                    |           |     |                                                                                        |
| Refer to the <a href="#">GX3290 (and family) Crosspoint Ball Guide</a> for a detailed list of SDI and SDO balls.  |           |     |                                                                                        |
| <b>Power</b>                                                                                                      |           |     |                                                                                        |
| Refer to the <a href="#">GX3290 (and family) Crosspoint Ball Guide</a> for a detailed list of power supply balls. |           |     |                                                                                        |
| <b>Ground</b>                                                                                                     |           |     |                                                                                        |
| Refer to the <a href="#">GX3290 (and family) Crosspoint Ball Guide</a> for a detailed list of ground balls.       |           |     |                                                                                        |



## 2. Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

| Parameter                                                                                                                               | Value                                                                               |
|-----------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| Supply Voltage (VDD_18)                                                                                                                 | -0.3V to +2.1V                                                                      |
| Supply Voltage (VCC_IN1, VCC_IN2, VCC_25_A, VDD_25, VDDIO_D, VCC_OUT1, VCC_OUT2, VCC_25_REF_CLK, VCC_25_VCO0, VCC_25_VCO1, VCC_25_VCO2) | -0.3V to +2.8V                                                                      |
| Input Voltage Range                                                                                                                     | -0.3 to (0.3 + min[VCC_IN1, VCC_25_A])V<br>for even numbered SDI inputs and EXT_PG0 |
|                                                                                                                                         | -0.3 to (0.3 + min[VCC_IN2, VCC_25_A])V<br>for odd numbered SDI inputs and EXT_PG1  |
| ESD Voltage (HBM; all balls)                                                                                                            | 1kV                                                                                 |
| ESD Voltage (CDM; all balls)                                                                                                            | 100V                                                                                |
| Storage Temperature Range                                                                                                               | -50°C to +125°C                                                                     |
| Operating Temperature Range                                                                                                             | 0°C to +85°C                                                                        |
| Solder Reflow Temperature                                                                                                               | 245°C                                                                               |

## 2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

| Parameter                          | Symbol                      | Min   | Typ | Max   | Units | Notes |
|------------------------------------|-----------------------------|-------|-----|-------|-------|-------|
| Operating Power Supply             | VCC_25_A,<br>VCC_25_REF_CLK | 2.375 | 2.5 | 2.625 | V     | 1     |
|                                    |                             | 1.14  | 1.2 | 1.26  | V     | 2     |
|                                    | VCC_IN1, VCC_IN2            | 1.71  | 1.8 | 1.89  | V     | 3     |
|                                    |                             | 2.375 | 2.5 | 2.625 | V     | 1     |
|                                    |                             | 1.14  | 1.2 | 1.26  | V     | 2     |
|                                    | VCC_OUT1,<br>VCC_OUT2       | 1.71  | 1.8 | 1.89  | V     | 3     |
|                                    |                             | 2.375 | 2.5 | 2.625 | V     | 1     |
|                                    | VDD_18                      | 1.71  | 1.8 | 1.89  | V     | 3     |
|                                    |                             | 1.71  | 1.8 | 1.89  | V     | 3     |
|                                    | VDDIO_D                     | 2.375 | 2.5 | 2.625 | V     | 1     |
|                                    | VDD_25                      | 2.375 | 2.5 | 2.625 | V     | 1     |
| Operating Temperature Range (case) | T <sub>OP</sub>             | 0     | 25  | 85    | °C    | —     |
| Start-up Temperature Range         | T <sub>SU</sub>             | -40   | —   | 85    | °C    | —     |

**Notes:**

1. 2.5V supply.
2. 1.2V supply.
3. 1.8V supply.

## 2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

| Parameter           | Symbol   | Conditions                                                                                                                                                                                                                | Min | Typ   | Max  | Units | Notes |
|---------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|------|-------|-------|
| System              |          |                                                                                                                                                                                                                           |     |       |      |       |       |
| Power               | P        | All channels active,<br>VCC_IN[1,2] =<br>VCC_OUT[1,2] =<br>1.2V±5%,<br>$\Delta V_{OD} = 200\text{mV}$ ,<br>$\Delta V_{SDI} = 800\text{mVppd}$ ,<br>de-emphasis=6, without<br>Pattern<br>Generator/Checker,<br>AC-coupled  | —   | 34.25 | 43   | W     | 1     |
|                     |          | All channels active,<br>VCC_IN[1,2] =<br>VCC_OUT[1,2] =<br>1.2V±5%,<br>$\Delta V_{OD} = 400\text{mV}$ ,<br>$\Delta V_{SDI} = 800\text{mVppd}$ ,<br>de-emphasis=6, without<br>Pattern<br>Generator/Checker,<br>AC-coupled  | —   | 37.66 | —    | W     | 1     |
|                     |          | All channels active,<br>VCC_IN[1,2] =<br>VCC_OUT[1,2] =<br>2.5V±5%,<br>$\Delta V_{OD} = 800\text{mV}$ ,<br>$\Delta V_{SDI} = 800\text{mVppd}$ ,<br>de-emphasis=6, without<br>Pattern<br>Generator/Checker,<br>AC-coupled  | —   | 44.39 | 54   | W     | 1     |
|                     |          | All channels active,<br>VCC_IN[1,2] =<br>VCC_OUT[1,2] =<br>2.5V±5%,<br>$\Delta V_{OD} = 1200\text{mV}$ ,<br>$\Delta V_{SDI} = 800\text{mVppd}$ ,<br>de-emphasis=6, without<br>Pattern<br>Generator/Checker,<br>AC-coupled | —   | 49.02 | 60   | W     | 1     |
|                     |          | PRBS Generator/Checker                                                                                                                                                                                                    | —   | 1.86  | —    | W     | —     |
| Power in Reset Mode | P        | $\overline{\text{RESET}} = 0$                                                                                                                                                                                             | —   | 0.5   | —    | W     | —     |
| Current - VCC_25_A  | ICC_25_A | With de-emphasis,<br>without Pattern<br>Generator/Checker                                                                                                                                                                 | —   | 13.8  | 16.7 | A     | —     |
|                     |          | Without de-emphasis,<br>without Pattern<br>Generator/Checker                                                                                                                                                              | —   | 13    | —    | A     | —     |

**Table 2-3: DC Electrical Characteristics (Continued)**

| Parameter          | Symbol   | Conditions                                                                                           | Min  | Typ  | Max  | Units | Notes |
|--------------------|----------|------------------------------------------------------------------------------------------------------|------|------|------|-------|-------|
| Current - VCC_IN1  | ICC_IN1  | All inputs active,<br>$\Delta V_{SDI} = 1.2V_{ppd}$ ,<br>DC-coupled                                  | —    | 1.75 | —    | A     | 2     |
|                    |          | All inputs active,<br>$\Delta V_{SDI} = 1.2V_{ppd}$ ,<br>AC-coupled                                  | -0.2 | —    | 0    | A     | 3     |
| Current - VCC_IN2  | ICC_IN2  | All inputs active,<br>$\Delta V_{SDI} = 1.2V_{ppd}$ ,<br>DC-coupled                                  | —    | 1.75 | —    | A     | 2     |
|                    |          | All inputs active,<br>$\Delta V_{SDI} = 1.2V_{ppd}$ ,<br>AC-coupled                                  | -0.2 | —    | 0    | A     | 3     |
| Current - VCC_OUT1 | ICC_OUT1 | VCC_OUT1 = 1.2V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 200mV$ , with<br>De-emphasis  | —    | 0.30 | 0.38 | A     | 4     |
|                    |          | VCC_OUT1 = 1.2V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 400mV$ , with<br>De-emphasis  | —    | 0.60 | —    | A     | 4     |
|                    |          | VCC_OUT1 = 1.2V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 800mV$ , with<br>De-emphasis  | —    | 1.12 | —    | A     | 4, 5  |
|                    |          | VCC_OUT1 = 2.5V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 200mV$ , with<br>De-emphasis  | —    | 0.34 | —    | A     | 4     |
|                    |          | VCC_OUT1 = 2.5V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 400mV$ , with<br>De-emphasis  | —    | 0.60 | —    | A     | 4     |
|                    |          | VCC_OUT1 = 2.5V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 800mV$ , with<br>De-emphasis  | —    | 1.23 | 1.55 | A     | 4     |
|                    |          | VCC_OUT1 = 2.5V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 1200mV$ , with<br>De-emphasis | —    | 1.64 | 2.13 | A     | 4     |
|                    |          | VCC_OUT1 = 2.5V $\pm 5\%$ ,<br>all outputs active,<br>$\Delta V_{OD} = 1200mV$ , with<br>De-emphasis | —    | 1.64 | 2.13 | A     | 4     |

Table 2-3: DC Electrical Characteristics (Continued)

| Parameter                 | Symbol          | Conditions                                                                                        | Min | Typ  | Max  | Units | Notes |
|---------------------------|-----------------|---------------------------------------------------------------------------------------------------|-----|------|------|-------|-------|
| Current - VCC_OUT2        | ICC_OUT2        | VCC_OUT2 = 1.2V $\pm$ 5%,<br>all outputs active,<br>$\Delta V_{OD}$ = 200mV, with<br>De-emphasis  | —   | 0.30 | 0.38 | A     | 4     |
|                           |                 | VCC_OUT2 = 1.2V $\pm$ 5%,<br>all outputs active,<br>$\Delta V_{OD}$ = 400mV, with<br>De-emphasis  | —   | 0.60 | —    | A     | 4     |
|                           |                 | VCC_OUT2 = 1.2V $\pm$ 5%,<br>all outputs active,<br>$\Delta V_{OD}$ = 800mV, with<br>De-emphasis  | —   | 1.12 | —    | A     | 4, 5  |
|                           |                 | VCC_OUT2 = 2.5V $\pm$ 5%,<br>all outputs active,<br>$\Delta V_{OD}$ = 200mV, with<br>De-emphasis  | —   | 0.34 | —    | A     | 4     |
|                           |                 | VCC_OUT2 = 2.5V $\pm$ 5%,<br>all outputs active,<br>$\Delta V_{OD}$ = 400mV, with<br>De-emphasis  | —   | 0.60 | —    | A     | 4     |
|                           |                 | VCC_OUT2 = 2.5V $\pm$ 5%,<br>all outputs active,<br>$\Delta V_{OD}$ = 800mV, with<br>De-emphasis  | —   | 1.23 | 1.55 | A     | 4     |
|                           |                 | VCC_OUT2 = 2.5V $\pm$ 5%,<br>all outputs active,<br>$\Delta V_{OD}$ = 1200mV, with<br>De-emphasis | —   | 1.64 | 2.13 | A     | 4     |
| Current - VCC_25_REF_CLK  | ICC_25_REF_CLK  |                                                                                                   | —   | 20   | 40   | mA    | —     |
| Current - VCC_VCO_DIGITAL | ICC_VCO_DIGITAL |                                                                                                   | —   | 6    | 10   | mA    | —     |
| Current - VCC_25_VCO0     | ICC_25_VCO0     |                                                                                                   | —   | 6    | 10   | mA    | —     |
| Current - VCC_25_VCO1     | ICC_25_VCO1     |                                                                                                   | —   | 6    | 10   | mA    | —     |
| Current - VCC_25_VCO2     | ICC_25_VCO2     |                                                                                                   | —   | 6    | 10   | mA    | —     |
| Current - VDD_18          | IDD_18          | VDD_18 = 1.8V $\pm$ 5%                                                                            | —   | 260  | 750  | mA    | —     |
| Current - VDD_25          | IDD_25          | VDD_25 = 2.5V $\pm$ 5%                                                                            | —   | 20   | 40   | mA    | —     |
| Current - VDDIO_D         | IDDIO_D         | VDDIO_D = 1.8V $\pm$ 5%,<br>all inputs active<br>(15pF load)                                      | —   | 50   | 100  | mA    | —     |
|                           |                 | VDDIO_D = 2.5V $\pm$ 5%,<br>all inputs active<br>(15pF load)                                      | —   | 70   | 140  | mA    | —     |

**Table 2-3: DC Electrical Characteristics (Continued)**

| Parameter                                | Symbol    | Conditions                                                                                                                            | Min                                      | Typ | Max                                      | Units    | Notes       |
|------------------------------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|-----|------------------------------------------|----------|-------------|
| <b>High-speed Inputs/Outputs</b>         |           |                                                                                                                                       |                                          |     |                                          |          |             |
| Serial Input Termination                 |           | Differential                                                                                                                          | —                                        | 100 | —                                        | $\Omega$ | 6           |
|                                          |           | Single-ended                                                                                                                          | —                                        | 50  | —                                        | $\Omega$ |             |
| Serial Output Termination                |           | Differential                                                                                                                          | —                                        | 100 | —                                        | $\Omega$ | —           |
| Serial Input Common Mode Voltage         | $V_{ICM}$ | $VCC\_IN[1,2] = 1.2V \pm 5\%$ ,<br>$VCC\_IN[1,2] = 1.8V \pm 5\%$ ,<br>$VCC\_IN[1,2] = 2.5V \pm 5\%$ ,<br>terminated to $VCC\_IN[1,2]$ | $VCC\_IN[1,2] - (\Delta V_{SDI\_max}/4)$ | —   | $VCC\_IN[1,2] - (\Delta V_{SDI\_min}/4)$ | V        | 7, 8, 9, 10 |
| Serial Output Common Mode Voltage        | $V_{OCM}$ | $VCC\_OUT[1,2] = 1.2V \pm 5\%$ ,<br>$VCC\_OUT[1,2] = 1.8V \pm 5\%$ ,<br>$VCC\_OUT[1,2] = 2.5V \pm 5\%$                                | $VCC\_OUT[1,2] - (\Delta V_{OD\_max}/4)$ | —   | $VCC\_OUT[1,2] - (\Delta V_{OD\_min}/4)$ | V        | —           |
| <b>Host Interface</b>                    |           |                                                                                                                                       |                                          |     |                                          |          |             |
| Logic HIGH voltage on digital input pins | $V_{IH}$  |                                                                                                                                       | $0.7 \times VDDIO\_D$                    | —   | $VDDIO\_D + 0.3$                         | V        | 11          |
| Logic LOW voltage on digital input pins  | $V_{IL}$  |                                                                                                                                       | -0.3                                     | —   | $0.3 \times VDDIO\_D$                    | V        | 11          |
| Output Logic LOW                         | $V_{OL}$  | $I_{OL} = 2mA$ ,<br>2.5V operation                                                                                                    | —                                        | —   | 0.7                                      | V        | 11          |
|                                          |           | $I_{OL} = 2mA$ ,<br>1.8V operation                                                                                                    | —                                        | —   | 0.45                                     | V        | 11          |
| Output Logic HIGH                        | $V_{OH}$  | $I_{OH} = -2mA$ ,<br>2.5V operation                                                                                                   | 1.7                                      | —   | —                                        | V        | 11          |
|                                          |           | $I_{OH} = -2mA$ ,<br>1.8 operation                                                                                                    | 1.35                                     | —   | —                                        | V        | 11          |

**Notes:**

1. Total Maximum Power is lower than individual maximum currents multiplied by individual maximum supply voltages because the individual maximum currents can not occur simultaneously (they occur at different conditions).
2. The  $ICC\_IN1$  and  $ICC\_IN2$  current flows out of the GX3290 and into the input signal source, and is subject to variability in that source. Some variability in input signal source current draw should be assumed, and up to  $\pm 15\%$  is possible.
3. When the common mode termination points for AC-coupled inputs are connected to  $VCC\_IN1$ ,  $VCC\_IN2$ , the GX3290 equalizer input bias currents can lead to current flowing out of the  $VCC\_IN1$ ,  $VCC\_IN2$  supply pins.
4. Currents apply for output DC-coupled applications. When AC-coupled, the current draw may be increased by up to 2x.
5. For DC-coupled applications only.
6. Input termination is selectable between  $100\Omega$  differential and  $50\Omega$  single-ended. See Section 3. [Input/Output Equivalent Circuits](#).
7. DC common mode current into/out of each EQ input differential pair should not exceed 14mA, and the current into/out of each half of the differential pair should not exceed 14mA.
8. No more than  $VCC\_IN[1,2] - \Delta V_{SDI\_actual}/4$ .
9. Where it is understood that  $VCC\_IN[1,2]$  have a  $\pm 5\%$  tolerance.
10. In no case should either side of the input differential pair be allowed to rise above  $VCC\_25\_A + 0.3V$  or fall below  $-0.3V$ .
11. Specifications relate to all host interface pins.

## 2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

| Parameter                                      | Symbol                         | Conditions                                 | Min  | Typ  | Max  | Units             | Notes |
|------------------------------------------------|--------------------------------|--------------------------------------------|------|------|------|-------------------|-------|
| <b>System</b>                                  |                                |                                            |      |      |      |                   |       |
| Serial Input Data Rate                         | DR <sub>SDO</sub>              | —                                          | —    | —    | 3.5  | Gb/s              | —     |
| Propagation Delay                              | t <sub>p</sub>                 | —                                          | —    | —    | 6    | ns                | 1     |
| Propagation Delay Difference                   | Δt <sub>p</sub>                | Between any two channels                   | —    | —    | 5.5  | ns                | 1     |
| <b>High-speed Inputs/Outputs</b>               |                                |                                            |      |      |      |                   |       |
| Output Switch Time using Update Enable Strobes |                                |                                            | 0.9  | —    | 1.8  | μs                | 2     |
| Input Voltage Swing                            | ΔV <sub>SDI</sub>              | —                                          | 100  | —    | 1200 | mVppd             | —     |
| Output Voltage Swing                           | ΔV <sub>OD</sub>               | VCC_OUT[1,2] = 1.2V±5%, Output = 200mVppd  | 150  | 225  | 300  | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 1.2V±5%, Output = 400mVppd  | 300  | 450  | 600  | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 1.2V±5%, Output = 800mVppd  | 600  | 900  | 1200 | mVppd             | 3     |
|                                                |                                | VCC_OUT[1,2] = 1.8V±5%, Output = 200mVppd  | 150  | 225  | 300  | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 1.8V±5%, Output = 400mVppd  | 300  | 450  | 600  | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 1.8V±5%, Output = 800mVppd  | 600  | 900  | 1200 | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 2.5V±5%, Output = 200mVppd  | 150  | 225  | 300  | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 2.5V±5%, Output = 400mVppd  | 300  | 450  | 600  | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 2.5V±5%, Output = 800mVppd  | 600  | 900  | 1200 | mVppd             | —     |
|                                                |                                | VCC_OUT[1,2] = 2.5V±5%, Output = 1200mVppd | 1000 | 1350 | 1700 | mVppd             | —     |
| Output Rise/Fall Time                          | t <sub>r</sub> /t <sub>f</sub> | All output swings. 20% to 80%.             | —    | —    | 150  | ps                | —     |
| Duty Cycle Distortion                          |                                | All data rates, all output swings.         | -50  | —    | +50  | ps                | —     |
| Additive Jitter                                |                                | All inputs active, peak-to-peak (PRBS 31)  | —    | —    | 60   | ps <sub>p-p</sub> | —     |
| Input Trace Equalization                       |                                |                                            | 0    | —    | 12   | dB                | 4     |
| Output De-Emphasis Setting                     | Range                          |                                            | 0    | —    | 11.2 | dB                | 4     |
|                                                | Maximum Setting                |                                            | 9    | —    | —    | dB                |       |

**Table 2-4: AC Electrical Characteristics (Continued)**

| Parameter                        | Symbol | Conditions | Min | Typ | Max   | Units | Notes   |
|----------------------------------|--------|------------|-----|-----|-------|-------|---------|
| <b>Host Interface</b>            |        |            |     |     |       |       |         |
| Parallel Rate of Operation       |        |            | 0.1 | —   | 112.5 | Mop/s | 5, 6, 7 |
| Serial Interface Operating Speed |        |            | 0.1 | —   | 25    | MHz   | 5, 8    |

**Notes:**

1. See [Section 4.4](#) for more details.
2. This parameter is the time it takes for the outputs to change to a new switch matrix configuration when the corresponding strobe signal assigned to that output is asserted.
3. DC-coupled.
4. Selectable, maximum gain occurs at 3Gb/s (or 1.5GHz).
5. Specifications relate to all host interface pins.
6. Millions of operations per second.
7. For detailed timing specifications, see [Section 4.12.1](#).
8. For detailed timing specifications, see [Section 4.12.2](#).



### 3. Input/Output Equivalent Circuits

**Note:** Please refer to the following supplementary documents: [Crosspoint Design Guide](#) and [EB-GX3290 Schematics, PCB Layout and Bill of Materials](#).

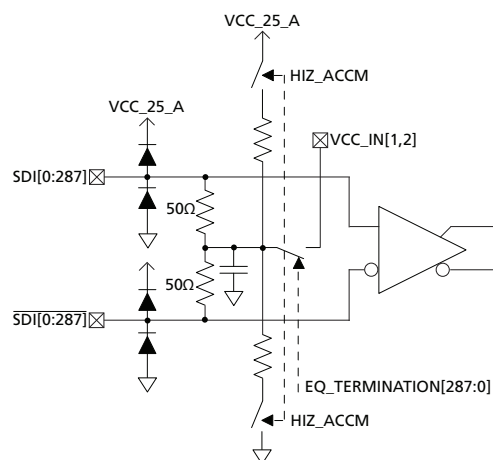


Figure 3-1: Equalizer Input Equivalent Circuit

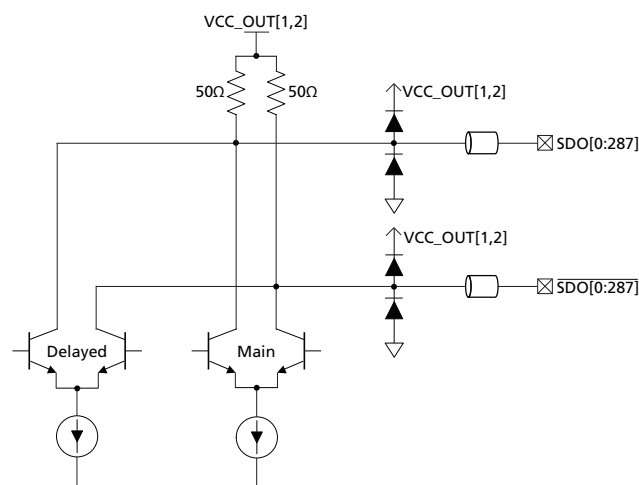


Figure 3-2: Trace Driver Output Equivalent Circuit

**Note:** the MON0 and MON1 outputs are terminated to the VCC\_25\_A supply.

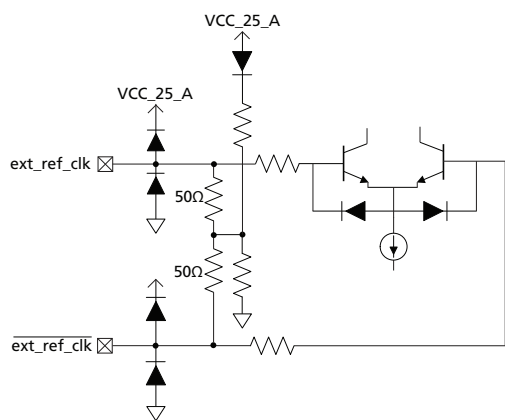
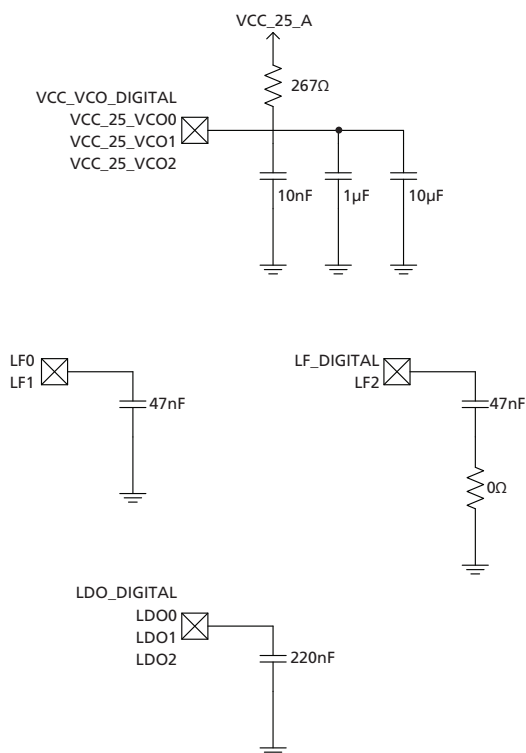
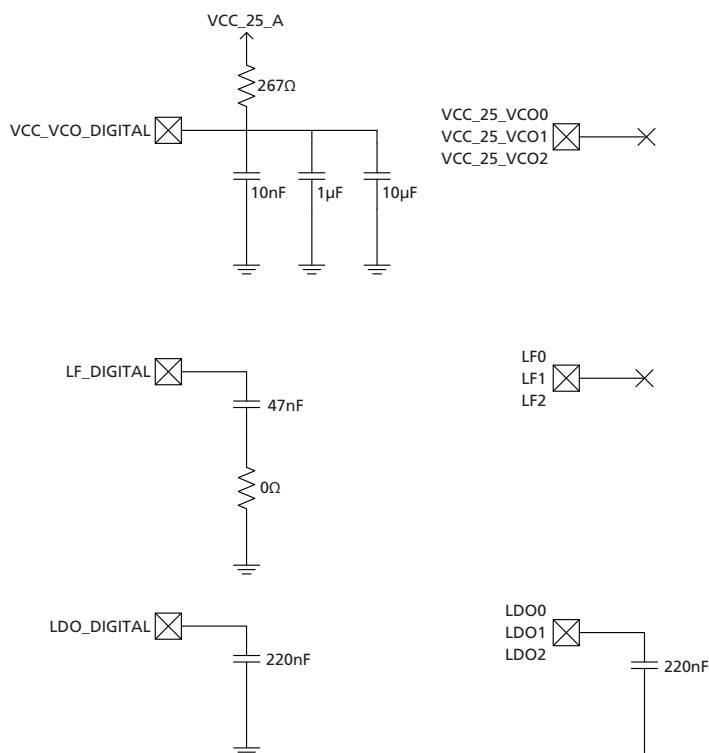


Figure 3-3: External Clock Input Equivalent Circuit

If the internal temperature ADCs, pattern generators, and checkers are used, these connections are required.



If the internal temperature ADCs, pattern generators, and checkers are not used, only these connections are required.



**Note 1:** Each of the VCC\_VCO\_DIGITAL, VCC\_VCO0, VCC\_VCO1, and VCC\_VCO2 pins require an independent RC network.

**Note 2:** The LF\_DIGITAL and LF2 pins each require an independent RC network.

**Note 3:** The LF0 and LF1 pins each require an independent capacitor to ground.

**Note 4:** Each of the LDO\_DIGITAL, LDO0, LDO1, and LDO2 pins require an independent capacitor to ground.

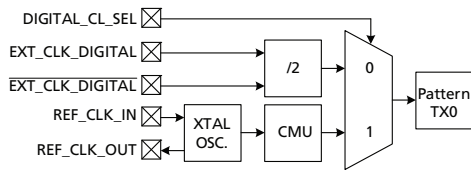
**Note 5:** VCC\_VCO\_DIGITAL, LF\_DIGITAL and LDO\_DIGITAL used for pattern generator TX0, digital communication (GSPI and APPI), and the internal temperature ADC for JNCTN\_TEMP\_1. VCC\_VCO\_DIGITAL, LF\_DIGITAL and LDO\_DIGITAL must always be connected.

**Note 6:** VCC\_25\_VCO0, LF0, LDO0 used for pattern checker RX0 and the internal temperature ADC for JNCTN\_TEMP\_0. If VCC\_25\_VCO0, LF0, and LDO0 are not connected, pattern checker RX0 and the internal temperature ADC for JNCTN\_TEMP\_0 will not operate.

**Note 7:** VCC\_25\_VCO1, LF1, LDO1 used for pattern checker RX1 and the internal temperature ADC for JNCTN\_TEMP\_2. If VCC\_25\_VCO1, LF1, and LDO1 are not connected, pattern checker RX1 and the internal temperature ADC for JNCTN\_TEMP\_2 will not operate.

**Note 8:** VCC\_25\_VCO2, LF2, LDO2 used for pattern generator TX1 and the internal temperature ADC for JNCTN\_TEMP\_3. If VCC\_25\_VCO2, LF2, and LDO2 are not connected, pattern generator TX1 and the internal temperature ADC for JNCTN\_TEMP\_3 will not operate.

Figure 3-4: Required connections for VCC\_VCO\_DIGITAL, VCC\_25\_VCO0, VCC\_25\_VCO1, VCC\_25\_VCO2, LF\_DIGITAL, LF0, LF1, LF2, LDO\_DIGITAL, LDO0, LDO1 and LDO2



**Note:** The clock used to drive Pattern Generator TX0 is also used to derive the clock timing for the digital core. Therefore, GSP/APP interface timing and update timing will track the external clock frequency if one is selected from the EXT\_CLK\_DIGITAL/EXT\_CLK\_DIGITAL pins for Pattern Generator TX0.

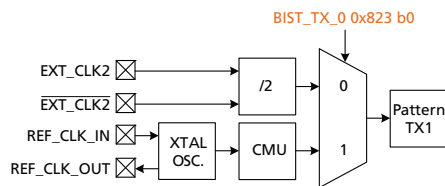
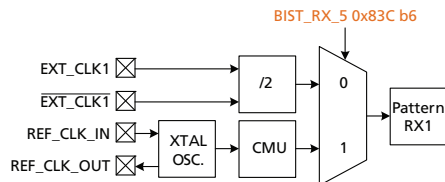
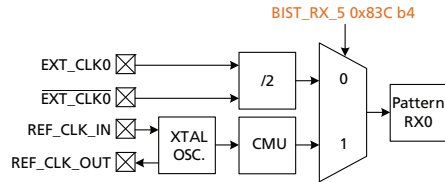
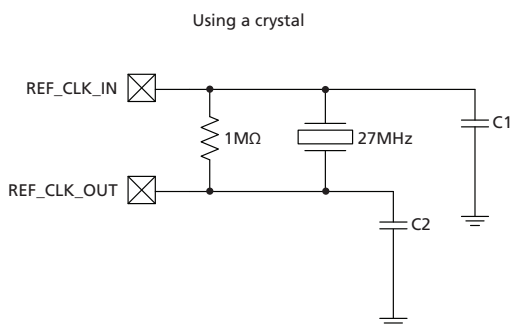


Figure 3-5: PRBS Generator/Checker Clock Selection



**Note:** The value of the C1 and C2 load capacitors are dependent on the chosen crystal.

Using a single-ended 27MHz oscillator

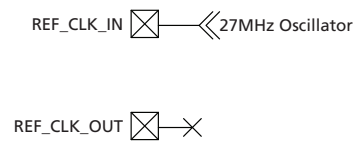


Figure 3-6: Crystal Oscillator

## 4. Detailed Description

### 4.1 Serial Data Input

Each of the GX3290 SDI inputs provide on-chip 100 $\Omega$  differential terminations (or 50 $\Omega$  single-ended). Each is compatible with input differential amplitudes from 100mVppd to 1200mVppd, and input signal sources having CML outputs referred to DC supplies of 1.2V, 1.8V or 2.5V. Note that for AC-coupled inputs, the recommended supply voltage for VCC\_IN1 and VCC\_IN2 is 1.8V.

Each of the 290 SDI input channels include frequency domain equalization, independently-programmable to one of four levels, to compensate from 0 to 47 inches (119 cm) of FR4 trace at 3Gb/s. The boost at the 1.5GHz Nyquist frequency, and recommended trace length range, are shown under EQ\_BOOST[287:0], EXT\_PG0\_EQ\_BOOST, EXT\_PG1\_EQ\_BOOST in Table 4-1. See Figure 3-1.

Each input can be powered-down independently using the corresponding EQ\_POWERDOWN[287:0] or EXT\_PG0\_EQ\_POWERDOWN or EXT\_PG1\_EQ\_POWERDOWN bit.

To accommodate input signal sources with 1.2V supplies and 1200mVppd signal amplitudes, the input common mode point should be terminated to the respective VCC\_IN1 or VCC\_IN2 supply.

The common mode termination connection to the respective VCC\_IN1 or VCC\_IN2 supply of each input can be independently controlled using the EQ\_TERMINATION[287:0] or EXT\_PG0\_EQ\_TERMINATION or EXT\_PG1\_EQ\_TERMINATION bit (see Figure 3-1 and Table 4-1).

**Note 1:** When the HIZ\_ACCM bit is set (register address 0x400h bit 0), inputs with their common mode termination not connected to VCC\_IN1 or VCC\_IN2 are connected to an internal common mode bias.

When an input EQ is powered-down, its common mode termination is automatically disconnected from the corresponding VCC\_IN1 or VCC\_IN2.

For each of the inputs, there are control parameters (register address 0x401h to 0x522h). See Table 4-1 below.

**Note 2:** The EXT\_PG01\_SOURCE\_PIN\_PRBSB and EXT\_PG1\_SOURCE\_PIN\_PRBSB bits in the TEST\_SETUP register must be set to connect the EXT\_PG0 and EXT\_PG1 pins to the matrix.

**Table 4-1: Serial Data Input**

| EQ_BOOST[287:0],<br>EXT_PG0_EQ_BOOST and<br>EXT_PG1_EQ_BOOST bits 1:0<br>(binary) | Boost Applied (@ nominal 1.5GHz) |                                     |
|-----------------------------------------------------------------------------------|----------------------------------|-------------------------------------|
| 00                                                                                | 0dB boost                        | 0" to 6" (15 cm) trace              |
| 01                                                                                | 3.5dB boost                      | 6" (15 cm) to 16"<br>(40 cm) trace  |
| 10                                                                                | 7.6dB boost                      | 16" (40 cm) to 35"<br>(89 cm) trace |

**Table 4-1: Serial Data Input (Continued)**

| EQ_BOOST[287:0],<br>EXT_PG0_EQ_BOOST and<br>EXT_PG1_EQ_BOOST bits 1:0<br>(binary)             |  | Boost Applied (@ nominal 1.5GHz)                                    |                                      |
|-----------------------------------------------------------------------------------------------|--|---------------------------------------------------------------------|--------------------------------------|
| 11                                                                                            |  | 12dB boost                                                          | 35" (89 cm) to 47"<br>(119 cm) trace |
| EQ_TERMINATION[287:0],<br>EXT_PG0_EQ_TERMINATION<br>and<br>EXT_PG1_EQ_TERMINATION<br>bits 3:3 |  | Input Termination Common Mode Point Switch to<br>VCC_IN_1, VCC_IN_2 |                                      |
| 0                                                                                             |  | Open (see <a href="#">Figure 3-1</a> )                              |                                      |
| 1                                                                                             |  | Closed (see <a href="#">Figure 3-1</a> )                            |                                      |
| EQ_POWERDOWN[287:0],<br>EXT_PG0_EQ_POWERDOWN<br>and<br>EXT_PG1_EQ_POWERDOWN<br>bits 4:4       |  | Equalizer Power                                                     |                                      |
| 0                                                                                             |  | On                                                                  |                                      |
| 1                                                                                             |  | Off                                                                 |                                      |

## 4.2 Serial Data Output

Each of the GX3290 SDI outputs have two on-chip 50Ω single-ended terminations, and can be programmed to output differential amplitudes of 200mVppd, 400mVppd or 800mVppd when the corresponding VCC\_OUT1 or VCC\_OUT2 is connected to either 1.2V or 1.8V, or 200mVppd, 400mVppd, 800mVppd, or 1200mVppd when the corresponding VCC\_OUT1 or VCC\_OUT2 is connected to 2.5V. The selection of the output swing is made using the corresponding OUTPUT\_SWING\_SET[287:0], MON0\_OUTPUT\_SWING\_SET or MON1\_OUTPUT\_SWING\_SET bits, shown in [Table 4-3](#).

If the HIGH\_OP\_V bit is set when either the VCC\_OUT1 or VCC\_OUT2 supplies are 1.2V or 1.8V, the 800mVppd swing setting is no longer valid for that output bank. Swing settings for an output bank connected to a 2.5V supply are unaffected.

**Table 4-2: HIGH\_OP\_V Swing Selection**

| VCC_OUTx<br>Supply Voltage<br>(V) | HIGH_OP_V = 0                              | HIGH_OP_V = 1                              | Note |
|-----------------------------------|--------------------------------------------|--------------------------------------------|------|
|                                   | Valid Output Swing<br>Selection<br>(mVppd) | Valid Output Swing<br>Selection<br>(mVppd) |      |
| 1.2                               | 200, 400, 800                              | 200, 400                                   | 1    |
| 1.8                               | 200, 400, 800                              | 200, 400                                   | —    |

**Table 4-2: HIGH\_OP\_V Swing Selection (Continued)**

| VCC_OUTx<br>Supply Voltage<br>(V) | HIGH_OP_V = 0                              | HIGH_OP_V = 1                              | Note |
|-----------------------------------|--------------------------------------------|--------------------------------------------|------|
|                                   | Valid Output Swing<br>Selection<br>(mVppd) | Valid Output Swing<br>Selection<br>(mVppd) |      |
| 2.5                               | 200, 400, 800                              | 200, 400, 800, 1200                        | 2    |

**Notes:**

1. For an 800mVppd output swing when the corresponding VCC\_OUT1 or VCC\_OUT2 is connected to 1.2V, the output must be DC-coupled to a receiving device terminated to 1.2V.
2. When VCC\_OUT1 or VCC\_OUT2 is set to 2.5V, the HIGH\_OP\_V bit must be set to enable 1200mVppd swing selection.

Each of the 290 SDI output channels provide independently programmable de-emphasis, to compensate from 0 to 47 inches (119 cm) of FR4 trace at 3Gb/s. The selection of the amount of output de-emphasis is made using the corresponding OUTPUT\_DEEMPHASIS[287:0], MON0\_OUTPUT\_DEEMPHASIS or MON1\_OUTPUT\_DEEMPHASIS bits, shown in [Table 4-3](#).

Each output can be independently powered-down by the setting of the corresponding bit: ACTIVE\_POWER\_DOWN[287:0], DYNAMIC\_POWER\_DOWN[287:0] together with the assigned strobe, MON0\_POWER\_DOWN, or MON1\_POWER\_DOWN.

The polarity of the signal at each output can be independently inverted by setting the corresponding bit: ACTIVE\_SIGNAL\_INVERT[287:0], DYNAMIC\_SIGNAL\_INVERT[287:0] together with the assigned strobe, MON0\_SIGNAL\_INVERT, or MON1\_SIGNAL\_INVERT.

**Table 4-3: Serial Data Output**

| OUTPUT_SWING_SET[287:0],<br>MON0_OUTPUT_SWING_SET and<br>MON1_OUTPUT_SWING_SET bits 2:0 (binary)    | Output Swing          |
|-----------------------------------------------------------------------------------------------------|-----------------------|
| 000                                                                                                 | 200mVppd              |
| 001                                                                                                 | 400mVppd              |
| 011                                                                                                 | 800mVppd              |
| 110                                                                                                 | 1200mVppd             |
| 111                                                                                                 | Reserved. Do not use. |
| OUTPUT_DEEMPHASIS[287:0],<br>MON0_OUTPUT_DEEMPHASIS and<br>MON1_OUTPUT_DEEMPHASIS bits 5:3 (binary) | Level of De-emphasis  |
| 000                                                                                                 | Off                   |
| 100                                                                                                 | 12" (30 cm) nominal   |
| 101                                                                                                 | 24" (60 cm) nominal   |
| 110                                                                                                 | 36" (90 cm) nominal   |
| 111                                                                                                 | 48" (120 cm) nominal  |

**Table 4-3: Serial Data Output (Continued)**

| ACTIVE_SIGNAL_INVERT[287:0],<br>DYNAMIC_SIGNAL_INVERT[287:0],<br>MON0_SIGNAL_INVERT or MON1_SIGNAL_INVERT |  | Status       |
|-----------------------------------------------------------------------------------------------------------|--|--------------|
| 0                                                                                                         |  | Not inverted |
| 1                                                                                                         |  | Inverted     |
| ACTIVE_POWER_DOWN[287:0],<br>DYNAMIC_POWER_DOWN[287:0], MON0_POWER_DOWN<br>or MON1_POWER_DOWN             |  | Status       |
| 0                                                                                                         |  | On           |
| 1                                                                                                         |  | Off          |

## 4.3 Crosspoint Switch Matrix Operation

The crosspoint switch matrix routes the serial digital input signals (SDI[0:287]/ $\overline{\text{SDI}}[0:287]$ , EXT\_PG0/ $\overline{\text{EXT\_PG0}}$  or EXT\_PG1/ $\overline{\text{EXT\_PG1}}$ ) to one or more serial digital outputs (SDO[0:287]/ $\overline{\text{SDO}}[0:287]$ , MON0/ $\overline{\text{MON0}}$  or MON1/ $\overline{\text{MON1}}$ ). The matrix is configured on a per output basis. Each serial digital output can be configured to accept a signal from one serial digital input. Multiple serial digital outputs can accept input from the same serial digital input.

Updates to the switch matrix take place as soon as they are written to the host interface when controlling the device through the ACTIVE Configuration and Status Registers. These registers are the **ACTIVE[287:0]**, **MON0**, and **MON1** registers found in Section 2 of the [Crosspoint \(GX3290 and family\) Reference Manual \(for CSRs\)](#) document.

Before the **ACTIVE[287:0]**, **MON0**, and **MON1** registers at addresses 0x200h through 0x321h can be directly used to update the crosspoint switch matrix, an initialization procedure is required. One of the UPDATE\_EN[7:0] pins needs be toggled from a low state to a high state, and back to a low state again.

Alternatively, set the **SOFTWARE\_UPDATE\_ENABLE** bit in the **CONTROL\_SETUP** register at address 0xA00h to a value of 1, and then toggle one of the **SOFT\_UPDATE\_EN[7:0]** bits in the **SOFT\_UPDATE\_CONTROL** register at address 0xA01h from a value of 0 to a value of 1, and then back to a value of 0.

If the **ACTIVE[287:0]**, **MON0**, and **MON1** registers are not being directly written by the system controller, this procedure is not required. Reading from the **ACTIVE[287:0]**, **MON0**, and **MON1** registers will work regardless of whether or not the above procedure is executed.

Updating the crosspoint switch matrix using the **DYNAMIC[287:0]** registers (discussed below) does not require the initialization procedure described above.

The switch matrix can also be updated using double-buffering when controlling the device through the DYNAMIC Configuration and Status Registers. These registers are **DYNAMIC[287:0]** in Section 1 of the [Crosspoint \(GX3290 and family\) Reference Manual \(for CSRs\)](#) document.

When using dynamic configuration, updates to the switch matrix are first written to the DYNAMIC[287:0] registers where they are held until the corresponding update strobe signal, selected using the UPDATE\_SELECT[287:0] bits in the DYNAMIC[287:0] registers, changes state from LOW-to-HIGH.

The source for the update strobes can either be via external pins (UPDATE\_EN[7:0]) or register bits (SOFT\_UPDATE\_EN[7:0]) as selected by the setting of the SOFTWARE\_UPDATE\_ENABLE bit in the CONTROL\_SETUP register. Setting the SOFTWARE\_UPDATE\_ENABLE bit LOW causes the device to use the external UPDATE\_EN[7:0] pins as update strobes for the switch matrix. Setting the SOFTWARE\_UPDATE\_ENABLE bit HIGH causes the device to use the SOFT\_UPDATE\_EN[7:0] bits as update strobes for the switch matrix. See Section 6 of the [Crosspoint \(GX3290 and family\) Reference Manual \(for CSRs\)](#) document.

When the selected update strobe signal (or bit) transitions from LOW-to-HIGH, the state of all the outputs configured to respond to that update strobe signal (or bit) are updated at that time.

Regardless of which register set is used to configure the switch matrix, the current configuration of the matrix is always available by reading back the ACTIVE[287:0] registers.

**Note:** The MON0 and MON1 outputs can not be powered up/down, switched, or polarity inverted dynamically (Dynamic Configuration). They can only be configured in the Active Configuration mode described above using the settings in registers 0x320h and 0x321h, respectively. Also, the MON0 and MON1 outputs are terminated to the VCC\_25\_A supply.

## 4.4 Propagation Delay

The propagation delay is dependent on the path that the signal takes through the device. Although the delay difference from the shortest path to the longest path could be up to 5.5ns, this difference is at a minimum for connections from inputs numerically close together and on the same side of the device to outputs that are numerically close together and on the same side of the device. Propagation delay differences of less than 750ps can be expected when the inputs are adjacent in the ballout and the outputs are also adjacent in the ballout.

**Note:** The 750ps propagation delay difference (skew) between physically adjacent channels is guaranteed by simulation.

## 4.5 Using Multiple Strokes

The GX3290 has eight fully-independent update strokes.

Outputs 287 to 0 can be assigned to one of the eight strokes through the setting of the UPDATE\_SELECT bits in the corresponding DYNAMIC[287:0] register. The input signal selection, output power switching and signal inversion will take effect on the LOW-to-HIGH edge of its assigned stroke signal or bit. This allows different portions of the crosspoint to be switched at different points in time. This is particularly useful in systems supporting multiple data or video formats, where the switch point/time varies from format to format.



## 4.6 Pattern Generator and Pattern Checker

### 4.6.1 Pattern Generator

**Note 1:** There are two pattern generator “Tx” blocks in the GX3290. In the following, wherever only TX0 is mentioned, the corresponding is also true for TX1.

**Note 2:** When the PRBS Generator is disabled, the generated signal does not completely terminate. The PRBS polynomial bits must be re-written in order to terminate the signal.

The two pattern generator “Tx” blocks in the GX3290 can each independently generate PRBS  $2^7-1$ , PRBS  $2^{15}-1$ , and PRBS  $2^{23}-1$  data patterns, or alternating 1's and 0's. The built-in clock multiplier PLLs independently synthesize rates of 270Mb/s and 2.97Gb/s from the required, external 27MHz reference clock (see [Section 4.9](#)). Other rates up to 3Gb/s can be generated by providing an external clock signal at 2x, 4x, or 22x the desired bit rate to TX1, with a maximum external clock frequency of 6GHz.

**Table 4-4: Tx External Clocks**

| TX0                                          | TX1                                 |
|----------------------------------------------|-------------------------------------|
| EXT_CLK_DIGITAL (AJ35)                       | EXT_CLK2 (R15)                      |
| $\overline{\text{EXT\_CLK\_DIGITAL}}$ (AH35) | $\overline{\text{EXT\_CLK2}}$ (T15) |

While this facility exists for both TX0 and TX1, the user is cautioned that the digital core clock is derived from the TX0 data clock, and therefore interface and update timing will track the external clock frequency if one is provided to TX0.

The pattern generators are enabled by the TX0\_PRBS\_GEN\_ENABLE and TX1\_PRBS\_GEN\_ENABLE bits (register address 0x802h, bits [1:0] respectively).

The PRBS generating polynomials used are:

1. PRBS7:  $x^7 + x^6 + 1$
2. PRBS15:  $x^{15} + x^{14} + 1$
3. PRBS23:  $x^{23} + x^{18} + 1$

The pattern generated is selected via the TX0\_PRBS\_POLYNOMIAL and TX1\_PRBS\_POLYNOMIAL bits (register address 0x800h and 0x801h respectively).

**Table 4-5: Generated Patterns**

| TX0_PRBS_POLYNOMIAL[1:0] (binary) | Pattern Generated |
|-----------------------------------|-------------------|
| 00                                | PRBS7             |
| 01                                | PRBS15            |
| 10                                | PRBS23            |
| 11                                | Square Wave       |

## 4.6.2 Pattern Checker

The pattern checkers de-serialize incoming serial data before checking for errors in the parallel domain. Three comparison modes are supported:

1. **Neutral Phase Comparison Mode.** The incoming data is re-timed in a CDR, and sampled at the neutral (eye center) phase recovered by the CDR before de-serialization. Errors with respect to the supported PRBS sequences can be counted.
2. **Offset Phase Comparison Mode.** The phase at which the incoming data is sampled with respect to the recovered clock is adjustable over a full UI. Errors with respect to the supported PRBS sequences can be counted. By sweeping the sampling phase and counting errors at each phase, an error rate “bathtub curve” can be recorded, and the horizontal eye opening evaluated.
3. **Arbitrary Data Comparison Mode.** This mode can operate on arbitrary data patterns. The incoming serial data is sampled at both the neutral phase and the adjustable phase, and each of the two sampled data streams is de-serialized and the two streams are compared in the parallel domain.

The pattern checker allows a true measurement of bit error rate for the supported PRBS sequences in the first two modes above. The third, arbitrary data comparison mode, gives an indication of the degree of eye closure at a given sampling phase offset, but cannot detect bit errors in the incident data. See [Figure 4-1](#) and [Figure 4-2](#) below.

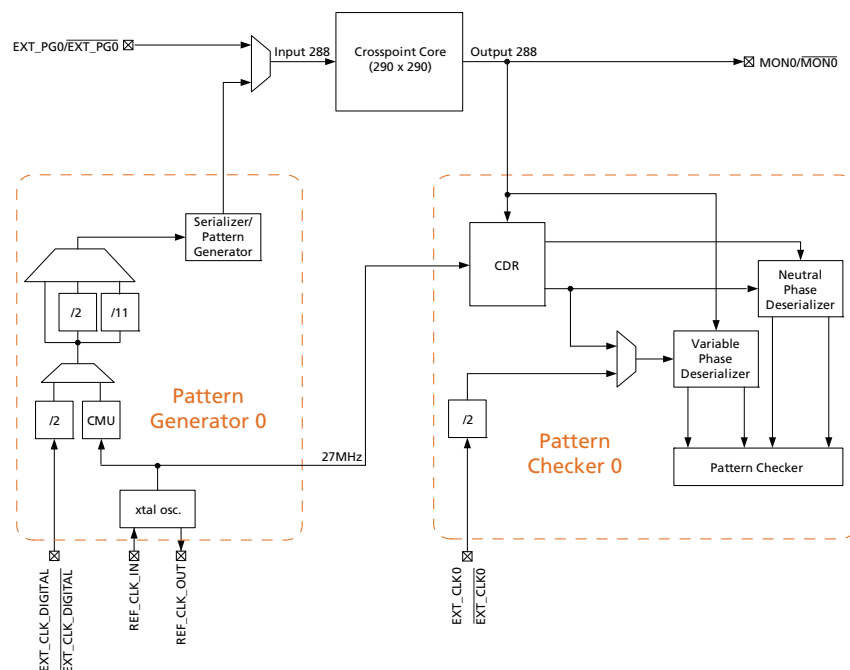


Figure 4-1: Simplified Pattern Generator/Checker Zero Block Diagram

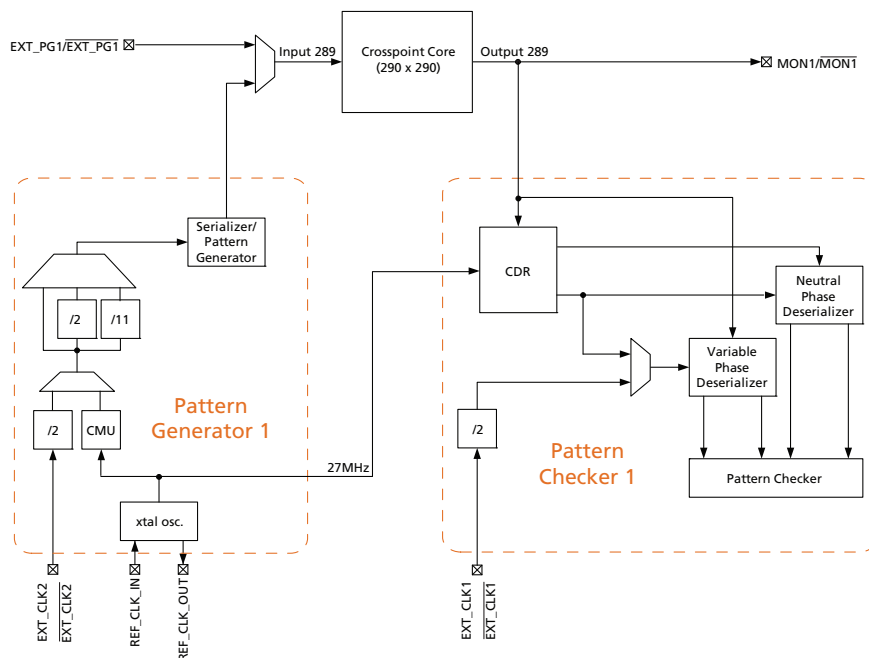


Figure 4-2: Simplified Pattern Generator/Checker One Block Diagram

**Note 1:** There are two pattern checker “Rx” blocks in the GX3290. In the following, wherever only RX0 is mentioned, the corresponding is also true for RX1.

The CDR integrated in each Rx block can independently lock to data at rates of 270Mb/s, 1.485Gb/s and 2.97Gb/s. Other rates up to 3Gb/s can be analyzed by providing an external clock signal of 2x, 4x, or 22x the desired bit rate, with a maximum external clock frequency of 6GHz. Note that retiming is not possible when using an external clock signal for the Rx block. The external clock must be synchronous with any data to be checked and the `RX0_PRBS_CHK_MODE` bits must be set to a value of '01'. The two pattern checker “Rx” blocks in the GX3290 can each independently check PRBS  $2^7-1$ , PRBS  $2^{15}-1$ , and PRBS  $2^{23}-1$  data patterns.

Table 4-6: Rx External Clocks

| RX0                                 | RX1                                  |
|-------------------------------------|--------------------------------------|
| EXT_CLK0 (R35)                      | EXT_CLK1 (AJ15)                      |
| $\overline{\text{EXT\_CLK0}}$ (T35) | $\overline{\text{EXT\_CLK1}}$ (AH15) |

The error checking modes are selected by the `RX0_PRBS_CHK_MODE` bits and the `RX1_PRBS_CHK_MODE` bits (addresses 0x804h and 0x810h respectively).

**Table 4-7: Checking Modes**

| RX0_PRBS_CHK_MODE[1:0] (binary) | Input Mode                                                                                          |
|---------------------------------|-----------------------------------------------------------------------------------------------------|
| 00                              | Check data sampled at neutral phase                                                                 |
| 01                              | Check data sampled at adjustable phase                                                              |
| 10 or 11                        | Compare nominally sampled data with phase offset data (allows eye monitoring of arbitrary patterns) |

The pattern checker will check for the PRBS pattern specified by the RX0\_PRBS\_POLYNOMIAL and RX1\_PRBS\_POLYNOMIAL bits (addresses 0x803h and 0x811h respectively).

The PRBS checkers are enabled by the RX0\_PRBS\_ENABLE and RX1\_PRBS\_ENABLE bits (register address 0x81Dh[1:0]).

**Table 4-8: Checked Patterns**

| RX0_PRBS_POLYNOMIAL[1:0] (binary) | Pattern Checked |
|-----------------------------------|-----------------|
| 00                                | PRBS7           |
| 01                                | PRBS15          |
| 10                                | PRBS23          |

The incident data can be inverted before checking by setting the corresponding RX0\_INVERT\_PRBS\_IN or RX1\_INVERT\_PRBS\_IN bit (address 0x803h[2:2] and 0x811h[2:2]) to '1'.

The number of words to be compared is selectable via the corresponding RX0\_PRBS\_BER\_TIME and RX1\_PRBS\_BER\_TIME bits (registers 0x80Ah and 0x817h).

**Table 4-9: Compared Words**

| RX0_PRBS_BER_TIME[3:0] (binary) | Number of words* compared (decimal) |
|---------------------------------|-------------------------------------|
| 0000                            | Infinite                            |
| 0001                            | 13                                  |
| 0010                            | 26                                  |
| 0011                            | 3277                                |
| 0100                            | 6554                                |
| 0101                            | 838861                              |
| 0110                            | 1677722                             |

**\*Note:** Each word is comprised of 10 bits, therefore the actual number of samples compared is 10 times the number of words compared.

The status of the two pattern checking blocks is available in the RX0\_PRBS\_LOCK and RX1\_PRBS\_LOCK, RX0\_PRBS\_PASS and RX1\_PRBS\_PASS, RX0\_PRBS\_FAIL and RX1\_PRBS\_FAIL, and RX0\_PRBS\_ERROR\_COUNT and RX1\_PRBS\_ERROR\_COUNT read-only bits (see register addresses 0x81Eh to 0x821h).

- **RX0\_PRBS\_LOCK [0]** - When HIGH, indicates that the pattern checker has acquired the pattern
- **RX0\_PRBS\_PASS [1]** - When HIGH, indicates that the pattern was locked, and the specified number of words have been compared with fewer detected errors than specified by the **RX0\_PRBS\_BER\_THRESH** parameter
- **RX0\_PRBS\_FAIL [2]** - Indicates that the test terminated in a failure condition. There are three possible failure conditions:
  1. The pattern generator failed to lock in the number of attempts specified by **RX0\_PRBS\_LOCK\_ATTEMPTS** (in which case **RX0\_PRBS\_LOCK** would still be '0').
  2. The pattern generator locked, but over the period of time indicated by the **RX0\_PRBS\_LOL\_TIME** bits, a greater number of errors were detected than allowed by the **RX0\_PRBS\_LOL\_THRESH** setting. In this error condition, the device determines that it has "lost lock", and terminates the test. This error condition is detectable if both **RX0\_PRBS\_LOCK** and **RX0\_PRBS\_FAIL** bits are HIGH, and the value of **RX0\_PRBS\_ERROR\_COUNT** is less than **RX0\_PRBS\_BER\_THRESH** (the same applies for **RX1\_PRBS\_LOCK**, **RX1\_PRBS\_FAIL** and **RX1\_PRBS\_ERROR\_COUNT**).
  3. The pattern generator locked, but the number of errors observed exceeded the value indicated by the **RX0\_PRBS\_BER\_THRESH** bits. This error is detectable if **RX0\_PRBS\_LOCK** and **RX0\_PRBS\_FAIL** are both HIGH, and the value of **RX0\_PRBS\_ERROR\_COUNT** is equal or greater than the value in **RX0\_PRBS\_BER\_THRESH**.

Note that the values of **RX0\_PRBS\_LOCK** and **RX1\_PRBS\_LOCK**, **RX0\_PRBS\_PASS** and **RX1\_PRBS\_PASS**, **RX0\_PRBS\_FAIL** and **RX1\_PRBS\_FAIL**, **RX0\_PRBS\_ERROR\_COUNT** and **RX1\_PRBS\_ERROR\_COUNT** are reset whenever any of the corresponding test parameters for the RX0 and RX1 pattern checkers are updated as well as whenever the corresponding **RX0\_PRBS\_ENABLE** or **RX1\_PRBS\_ENABLE** bits are set to '1' when previously set to '0'. To start a new PRBS test when the previous one has already been run, either re-write **RX0\_PRBS\_BER\_TIME/RX1\_PRBS\_BER\_TIME** or toggle **RX0\_PRBS\_ENABLE/RX1\_PRBS\_ENABLE**.

**Note 2:** The pattern checkers will count zero errors if the incident data is simply a static zero.

## 4.7 Horizontal Eye Measurement

As explained above, the GX3290 enables the measurement of bit error “bathtub” curves at the video rates of 1485Mb/s and 2970Mb/s to assist in evaluating how much margin there is in the system.

See [Using the Monitoring Features of the GX3290 Application Note](#) for more information.

### 4.7.1 Configuration for Horizontal Eye Measurement

- Route the input signal of interest to the MON0 or MON1 of the matrix
- Route the monitor output of matrix to pattern checker Rx, (RX0 in the notes below) by changing the RX0\_CHECK\_KEY\_D2A word from its default value of 512 (decimal) to 288 (decimal)
- For a PRBS pattern, select a pattern length with a value of the RX0\_PRBS\_POLYNOMIAL bits set to match the source pattern, and set the RX0\_PRBS\_CHK\_MODE bits to 1 to select the phase interpolator path
- For an arbitrary pattern, set the RX0\_PRBS\_CHK\_MODE bits to 2 to select the direct data comparison mode
- Set initial sampling phase with the RX0\_PHASE\_INTERPOLATOR\_PHASE\_SEL\_D2A bits (in the BIST\_RX\_4 register)
- Initiate error counting as described in [Section 4.6.2](#) above
- Increment the sampling phase
- Count errors
- Repeat last two steps to cover one UI

## 4.8 Temperature Sensors

The GX3290 has twelve on-chip temperature sensors comprised of four junction diode temperature sensors and four ADCs, each with two selectable temperature sensors. Analog output voltages can be used to determine the temperature of the chip at the junction diode temperature sensors in four different locations. An external test current is applied to each sensor, and the voltage across the sensor is measured.

Note that the “A” and “K” of the pin names indicate the preferred direction of the test current, but other junctions are present internally. Test currents should be limited to 10mA or less.

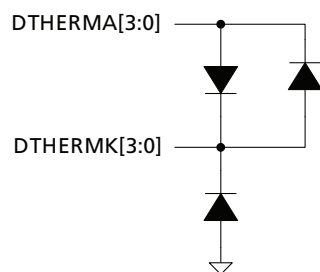


Figure 4-3: Temperature Sensors

In addition to the diode temperature sensors, four ADCs, each with two selectable temperature sensors, are also provided. Digitized temperatures can be read through the device's host interface.

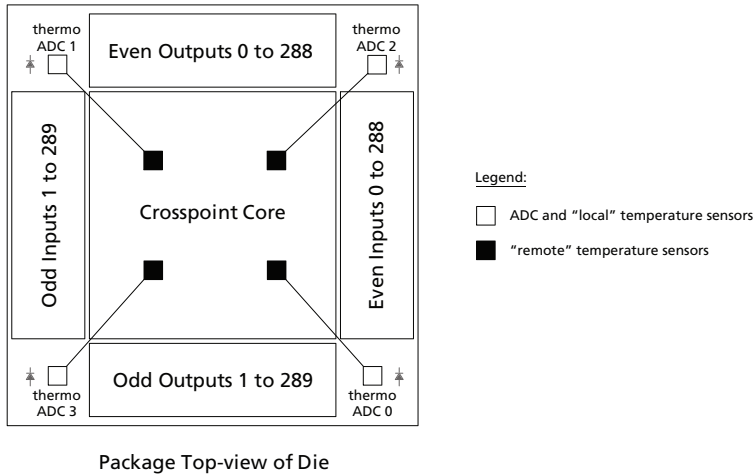


Figure 4-4: Map of Thermometer ADC Positions on Die

Table 4-10: Junction Temperature Registers

| Thermometer ADC | Sensor Location Select Register | Result Register |
|-----------------|---------------------------------|-----------------|
| 0               | ADC_IN_0                        | JNCTN_TEMP_0    |
| 1               | ADC_IN_1                        | JNCTN_TEMP_1    |
| 2               | ADC_IN_2                        | JNCTN_TEMP_2    |
| 3               | ADC_IN_3                        | JNCTN_TEMP_3    |

Digitized 10-bit temperature values can be read through the host interface from registers **JNCTN\_TEMP\_0** (register 0xA08h[9:0]) through **JNCTN\_TEMP\_3** (register 0xA0Bh[9:0]). The temperature word in each register will be updated every  $2^{13}$  clock cycles, provided the value of the respective **COUNT\_PD\_[3:0]** bit remains LOW. When a **COUNT\_PD\_[3:0]** bit goes HIGH, the ADC is reset and the corresponding **JNCTN\_TEMP\_[3:0]** register retains its last updated value. The clock rate can be selected between 211kHz or 844kHz through the corresponding **ADC\_CTRL\_CLK\_SEL\_[3:0]** bits (registers 0xA04h, 0xA05h, 0xA06h and 0xA07h).

The junction temperature at each temperature sensor in terms of the ADC output code is given by:

$$T_j = 0.5489 \times \text{JNCTN\_TEMP\_}[3:0] - 263 + \delta_3$$

Where  $\delta_3$  is the temperature uncertainty. The accuracy of the temperature sensors can be improved by calibrating the GX3290 at a known junction temperature. Without calibration, the temperature uncertainty, due to process variations and component mismatch, can be as high as  $\pm 27^\circ\text{C}$ . After calibration, the uncertainty can be reduced to about  $\pm 2^\circ\text{C}$ .

See [Using the Monitoring Features of the GX3290 Application Note](#) for more information.

**Table 4-11: Nominal Temperature-to-Code Conversion**

| T <sub>j</sub> (°C) | JNCTN_TEMP_<br>[3:0] | T <sub>j</sub> (°C) | JNCTN_TEMP_<br>[3:0] | T <sub>j</sub> (°C) | JNCTN_TEMP_<br>[3:0] | T <sub>j</sub> (°C) | JNCTN_TEMP_<br>[3:0] |
|---------------------|----------------------|---------------------|----------------------|---------------------|----------------------|---------------------|----------------------|
| -40                 | 406                  | 2                   | 483                  | 44                  | 559                  | 86                  | 636                  |
| -38                 | 410                  | 4                   | 486                  | 46                  | 563                  | 88                  | 639                  |
| -36                 | 414                  | 6                   | 490                  | 48                  | 567                  | 90                  | 643                  |
| -34                 | 417                  | 8                   | 494                  | 50                  | 570                  | 92                  | 647                  |
| -32                 | 421                  | 10                  | 497                  | 52                  | 574                  | 94                  | 650                  |
| -30                 | 424                  | 12                  | 501                  | 54                  | 578                  | 96                  | 654                  |
| -28                 | 428                  | 14                  | 505                  | 56                  | 581                  | 98                  | 658                  |
| -26                 | 432                  | 16                  | 508                  | 58                  | 585                  | 100                 | 661                  |
| -24                 | 435                  | 18                  | 512                  | 60                  | 588                  | 102                 | 665                  |
| -22                 | 439                  | 20                  | 516                  | 62                  | 592                  | 104                 | 669                  |
| -20                 | 443                  | 22                  | 519                  | 64                  | 596                  | 106                 | 672                  |
| -18                 | 446                  | 24                  | 523                  | 66                  | 599                  | 108                 | 676                  |
| -16                 | 450                  | 26                  | 527                  | 68                  | 603                  | 110                 | 680                  |
| -14                 | 454                  | 28                  | 530                  | 70                  | 607                  | 112                 | 683                  |
| -12                 | 457                  | 30                  | 534                  | 72                  | 610                  | 114                 | 687                  |
| -10                 | 461                  | 32                  | 538                  | 74                  | 614                  | 116                 | 690                  |
| -8                  | 465                  | 34                  | 541                  | 76                  | 618                  | 118                 | 694                  |
| -6                  | 468                  | 36                  | 545                  | 78                  | 621                  | 120                 | 698                  |
| -4                  | 472                  | 38                  | 548                  | 80                  | 625                  | 122                 | 701                  |
| -2                  | 475                  | 40                  | 552                  | 82                  | 629                  | 124                 | 705                  |
| 0                   | 479                  | 42                  | 556                  | 84                  | 632                  | 126                 | 709                  |



## 4.9 27MHz Reference Clock

The GX3290 requires an external 27MHz reference clock for correct operation. This clock is multiplied to generate the digital core and interface clocks, and is also used to synthesize video rate clocks in the pattern generation blocks, and to acquire video rate signals in the pattern checker blocks. The reference clock has no impact on the jitter measurement performance when the pattern checker blocks are locked to external data sources, but has a direct impact on jitter performance within the loop bandwidth of the CMU PLL in the pattern generation blocks.

The 27MHz reference clock can be generated by connecting a crystal between the REF\_CLK\_IN and REF\_CLK\_OUT balls, along with appropriate loading capacitors and a feedback resistor (see Figure 3-6). Alternatively, an LVCMOS 27MHz external clock source can be connected to the REF\_CLK\_IN ball with the REF\_CLK\_OUT ball left floating. The frequency variation of the crystal (including aging, supply and temperature variation) should be less than  $\pm 100\text{ppm}$  if the PRBS checking and generation features are to be used in video applications.

## 4.10 Device Power-Up

**Note 1:** No power supply sequencing is required (see Section 4.11).

There is a  $50\mu\text{s}$  delay ( $t_{\text{idle}}$ ) between the power supplies reaching their nominal value and the device becoming operational. During this time, there should be no host interface activity, and the UPDATE\_EN[7:0] pins must be held LOW.

The RC filter, shown in Figure 3-4, on each of the four VCO supplies—VCC\_25\_VCO0, VCC\_25\_VCO1, VCC\_25\_VCO2 and VCC\_VCO\_DIGITAL—is required to minimize the phase noise of the PLLs in pattern generation/detection modes, but the rise time of the filter on VCC\_VCO\_DIGITAL in particular can impact the start-up time of the device internal clock.

**Note 2:** In applications where power supplies reach their final voltage in under 1ms (the time for the internal clock to start), approximately two time constants of the RC filter on VCC\_VCO\_DIGITAL, can dominate the time for the GX3290 to emerge from reset upon power-up. In such cases, the time for VCC\_VCO\_DIGITAL can be traded-off against supply filtering and hence low-frequency jitter of patterns generated by Pattern Generator Zero.

**Note 3:**  $\overline{\text{RESET}}$  must be held LOW until all power supplies have stabilized.

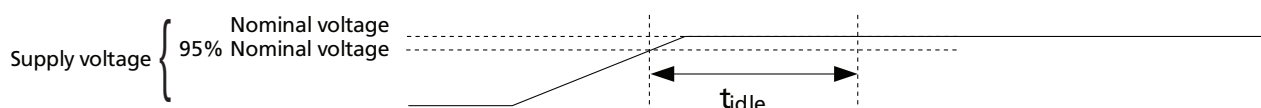


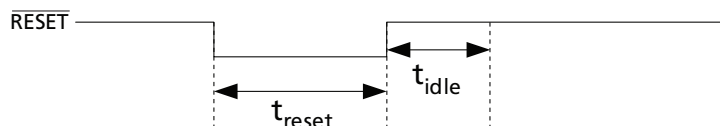
Figure 4-5: Power-Up Timing Diagram

## 4.11 Device Reset

The  $\overline{\text{RESET}}$  pin is an active-LOW asynchronous reset for the device. Assertion of the  $\overline{\text{RESET}}$  pin sets the device in its minimum power state. The minimum pulse width of the  $\overline{\text{RESET}}$  signal is 10ms ( $t_{\text{reset}}$ ). There is a 50 $\mu$ s delay ( $t_{\text{idle}}$ ) between the  $\overline{\text{RESET}}$  signal going HIGH (inactive) and the device becoming operational. During this time (all of  $t_{\text{reset}} + t_{\text{idle}}$ ), there should be no host interface activity and the UPDATE\_EN[7:0] pins must be held LOW.

**Note 1:**  $\overline{\text{RESET}}$  must be held LOW until all power supplies have stabilized.

**Note 2:** Upon emerging from reset, all SDI inputs and SDO outputs are powered-down, pattern generation and checking is inactive, and all registers assume their reset values as noted in the Semtech [Crosspoint \(GX3290 and family\) Reference Manual \(for CSRs\)](#).



Reset Timing Diagram

## 4.12 Host Interface

### 4.12.1 Parallel Host Interface Specifications

The Asynchronous Parallel Peripheral Interface (APPI) on the GX3290 device allows an external host to access internal registers using parallel read and write operations.

The GX3290 APPI is selected by setting the HOST\_S/ $\overline{\text{P}}$  pin LOW.

**Note:** The  $\overline{\text{S\_CS}}$  pin must be pulled LOW when HOST\_S/ $\overline{\text{P}}$  is set LOW for parallel port communication.

The host interface communicates with the Control and Status Registers (CSR) over an APPI bridge. It is possible to write one register every 10ns (100MHz write update rate). It is also possible to read one register every 20ns (50MHz read update rate).

The parallel interface is asynchronous. During writes, an active-LOW  $\overline{\text{P\_CS}}$  (Chip Select) enables the interface and  $\overline{\text{ADS}}$  (Address/Data Strobe) latches 12-bit write address and 16-bit write data into the device. During reads, the same  $\overline{\text{P\_CS}}$  signal is used, and the  $\overline{\text{ADS}}$  signal latches the 12-bit read address and then clocks out the 16-bit read data. The  $\text{P\_R}/\overline{\text{W}}$  signal is used to differentiate between the two access types.

An auto-increment mode exists for both reads and writes. This mode is configured by way of the APPI\_AUTO\_INCREMENT bit in the HOST\_SETUP register. See Section 6 in the Semtech [Crosspoint \(GX3290 and family\) Reference Manual \(for CSRs\)](#).

**Table 4-12: APPI Inputs/Outputs**

| Signal Name         | I/O | Description                                                                                                                        |
|---------------------|-----|------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{P\_CS}$  | I   | Chip Select from the host.                                                                                                         |
| $\overline{P\_ADS}$ | I   | Address/Data Strobe from the host; used to “clock” address and write data into the chip, and to “clock” read data out of the chip. |
| $P\_R/\overline{W}$ | I   | Read/Write indication from the host; HIGH for read, LOW for write.                                                                 |
| $P\_ADD[11:0]$      | I   | Address from the host.                                                                                                             |
| $P\_DAT[15:0]$      | I/O | Write data from the host, or read data to the host.                                                                                |

#### 4.12.1.1 APPI External Timing for Normal Write

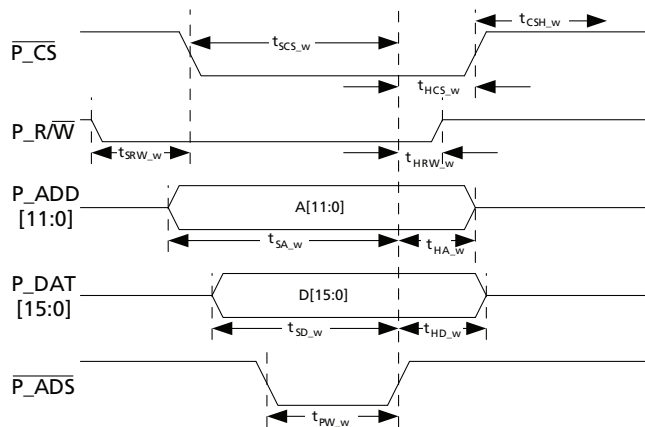


Figure 4-6: External Timing for Normal Write Cycle

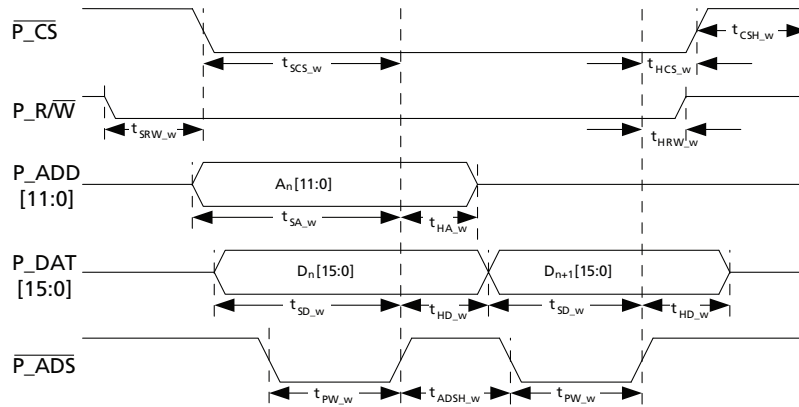
**Table 4-13: APPI External Timing Specifications for Normal Write**

| Parameter                                                             | Symbol       | Equiv. Cycles | Min  | Typ | Max | Units |
|-----------------------------------------------------------------------|--------------|---------------|------|-----|-----|-------|
| $\overline{P\_CS}$ LOW before $\overline{P\_ADS}$ positive edge       | $t_{SCS\_w}$ | —             | 10.0 | —   | —   | ns    |
| $\overline{P\_CS}$ hold time after $\overline{P\_ADS}$ positive edge  | $t_{HCS\_w}$ | 2             | 14.8 | —   | —   | ns    |
| $P\_R/\overline{W}$ low before $\overline{P\_ADS}$ negative edge      | $t_{SRW\_w}$ | —             | 1.5  | —   | —   | ns    |
| $P\_R/\overline{W}$ hold time after $\overline{P\_ADS}$ positive edge | $t_{HRW\_w}$ | 2             | 14.8 | —   | —   | ns    |
| $P\_ADD[11:0]$ setup before $\overline{P\_ADS}$ positive edge         | $t_{SA\_w}$  | —             | 10.0 | —   | —   | ns    |
| $P\_ADD[11:0]$ hold after $\overline{P\_ADS}$ positive edge           | $t_{HA\_w}$  | —             | 5.0  | —   | —   | ns    |
| $P\_DAT[15:0]$ setup before $\overline{P\_ADS}$ positive edge         | $t_{SD\_w}$  | —             | 5.0  | —   | —   | ns    |
| $P\_DAT[15:0]$ hold after $\overline{P\_ADS}$ positive edge           | $t_{HD\_w}$  | —             | 5.0  | —   | —   | ns    |
| $\overline{P\_ADS}$ LOW pulse width                                   | $t_{PW\_w}$  | 0.6           | 4.4  | —   | —   | ns    |

**Table 4-13: APPI External Timing Specifications for Normal Write (Continued)**

| Parameter                                            | Symbol       | Equiv. Cycles | Min  | Typ | Max   | Units |
|------------------------------------------------------|--------------|---------------|------|-----|-------|-------|
| $\overline{P\_CS}$ HIGH before next read/write cycle | $t_{CSH\_w}$ | 5             | 37.0 | —   | —     | ns    |
| Frequency for back-to-back single writes             | —            | —             | —    | —   | 16.17 | MHz   |

#### 4.12.1.2 APPI External Timing for Auto-Increment Write



**Figure 4-7: External Timing for Auto-Increment Write Cycle**

**Table 4-14: APPI External Timing Specifications for Auto-Increment Write**

| Parameter                                                                 | Symbol        | Equiv. Cycles | Min  | Typ | Max   | Units |
|---------------------------------------------------------------------------|---------------|---------------|------|-----|-------|-------|
| $\overline{P\_CS}$ LOW before $\overline{P\_ADS}$ positive edge           | $t_{SCS\_w}$  | —             | 10.0 | —   | —     | ns    |
| $\overline{P\_CS}$ hold time after last $\overline{P\_ADS}$ positive edge | $t_{HCS\_w}$  | 2             | 14.8 | —   | —     | ns    |
| $\overline{P\_R/W}$ LOW before $\overline{P\_CS}$ negative edge           | $t_{SRW\_w}$  | —             | 1.5  | —   | —     | ns    |
| $\overline{P\_R/W}$ hold time after $\overline{P\_ADS}$ positive edge     | $t_{HRW\_w}$  | 2             | 14.8 | —   | —     | ns    |
| $P\_ADD[11:0]$ setup before $\overline{P\_ADS}$ positive edge             | $t_{SA\_w}$   | —             | 10.0 | —   | —     | ns    |
| $P\_ADD[11:0]$ hold after $\overline{P\_ADS}$ positive edge               | $t_{HA\_w}$   | —             | 5.0  | —   | —     | ns    |
| $P\_DAT[15:0]$ setup before $\overline{P\_ADS}$ positive edge             | $t_{SD\_w}$   | —             | 4.0  | —   | —     | ns    |
| $P\_DAT[15:0]$ hold after $\overline{P\_ADS}$ positive edge               | $t_{HD\_w}$   | —             | 4.0  | —   | —     | ns    |
| $\overline{P\_ADS}$ LOW pulse width                                       | $t_{PW\_w}$   | 0.6           | 4.4  | —   | —     | ns    |
| $\overline{P\_ADS}$ HIGH before next pulse                                | $t_{ADSH\_w}$ | 0.6           | 4.4  | —   | —     | ns    |
| $\overline{P\_CS}$ HIGH before next read/write cycle                      | $t_{CSH\_w}$  | 5             | 37.0 | —   | —     | ns    |
| Frequency during auto-increment write                                     | —             | —             | —    | —   | 112.5 | MHz   |

### 4.12.1.3 APPI External Timing for Normal Read

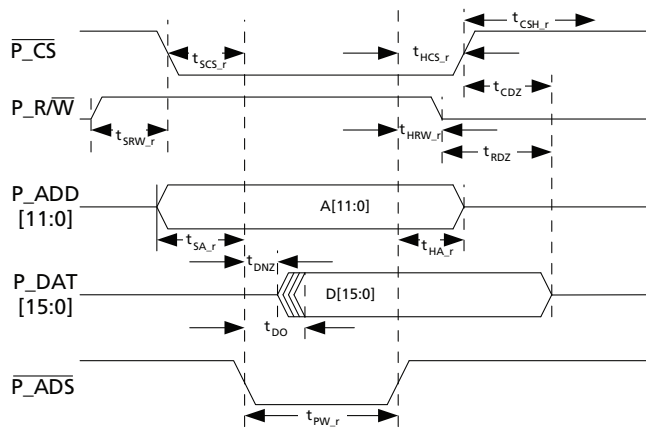


Figure 4-8: External Timing for Normal Read Cycle

Table 4-15: APPI External Timing Specifications for Normal Read

| Parameter                                                              | Symbol       | Equiv. Cycles | Min  | Typ | Max   | Units |
|------------------------------------------------------------------------|--------------|---------------|------|-----|-------|-------|
| Internal read pipeline delay (0 if one-cycle read)                     | —            | 1             | —    | —   | —     | —     |
| $\overline{P\_CS}$ LOW before $\overline{P\_ADS}$ negative edge        | $t_{SCS\_r}$ | —             | 5.0  | —   | —     | ns    |
| $\overline{P\_CS}$ hold time after $\overline{P\_ADS}$ positive edge   | $t_{HCS\_r}$ | —             | 5.0  | —   | —     | ns    |
| $P\_R/\overline{W}$ HIGH before $\overline{P\_CS}$ negative edge       | $t_{SRW\_r}$ | —             | 1.5  | —   | —     | ns    |
| $P\_R/\overline{W}$ hold time after $\overline{P\_ADS}$ positive edge  | $t_{HRW\_r}$ | —             | 5.0  | —   | —     | ns    |
| $P\_ADD[11:0]$ setup before $\overline{P\_ADS}$ negative edge          | $t_{SA\_r}$  | —             | 0.0  | —   | —     | ns    |
| $P\_ADD[11:0]$ hold after $\overline{P\_ADS}$ positive edge            | $t_{HA\_r}$  | —             | 0.0  | —   | —     | ns    |
| $P\_DAT[15:0]$ out of tristate after $\overline{P\_ADS}$ negative edge | $t_{DNZ}$    | 2             | 14.8 | —   | —     | ns    |
| $P\_DAT[15:0]$ becomes valid after $\overline{P\_ADS}$ negative edge   | $t_{DO}$     | —             | —    | —   | 65.0  | ns    |
| $P\_DAT[15:0]$ goes tristate after $\overline{P\_CS}$ positive edge    | $t_{DZ}$     | —             | —    | —   | 45.0  | ns    |
| $P\_DAT[15:0]$ goes tristate after $\overline{P\_ADS}$ positive edge   | $t_{DZ}$     | —             | —    | —   | 45.0  | ns    |
| $\overline{P\_ADS}$ LOW pulse width                                    | $t_{PW}$     | —             | 65.0 | —   | —     | ns    |
| $\overline{P\_CS}$ HIGH before next read/write cycle                   | $t_{CSH\_r}$ | 3             | 22.2 | —   | —     | ns    |
| Frequency for back-to-back single reads                                | —            | —             | —    | —   | 10.29 | MHz   |

#### 4.12.1.4 APPI External Timing for Auto-Increment Read

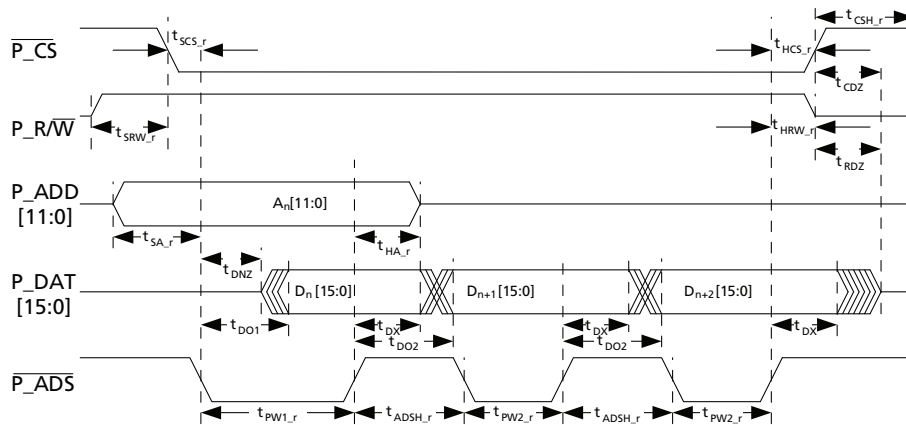


Figure 4-9: External Timing for Auto-Increment Read Cycle

Table 4-16: APPI External Timing Specifications for Auto-Increment Read

| Parameter                                                                  | Symbol        | Equiv. Cycles | Min  | Typ | Max   | Units |
|----------------------------------------------------------------------------|---------------|---------------|------|-----|-------|-------|
| Internal read pipeline delay (0 if one-cycle read)                         | —             | 1             | —    | —   | —     | —     |
| $\overline{P\_CS}$ LOW before first $\overline{P\_ADS}$ positive edge      | $t_{SCS\_r}$  | —             | 5.0  | —   | —     | ns    |
| $\overline{P\_CS}$ hold time after last $\overline{P\_ADS}$ positive edge  | $t_{HCS\_r}$  | —             | 5.0  | —   | —     | ns    |
| $\overline{P\_R/W}$ HIGH before $\overline{P\_CS}$ negative edge           | $t_{SRW\_r}$  | —             | 1.5  | —   | —     | ns    |
| $\overline{P\_R/W}$ hold time after last $\overline{P\_ADS}$ positive edge | $t_{HRW\_r}$  | —             | 5.0  | —   | —     | ns    |
| $P\_ADD[11:0]$ setup before $\overline{P\_ADS}$ negative edge              | $t_{SA\_r}$   | —             | 0.0  | —   | —     | ns    |
| $P\_ADD[11:0]$ hold after $\overline{P\_ADS}$ positive edge                | $t_{HA\_r}$   | —             | 0.0  | —   | —     | ns    |
| $P\_DAT[15:0]$ out of tristate after $\overline{P\_ADS}$ negative edge     | $t_{DNZ}$     | 2             | 14.8 | —   | —     | ns    |
| $P\_DAT[15:0]$ becomes valid after first $\overline{P\_ADS}$ negative edge | $t_{DO1}$     | —             | —    | —   | 70.0  | ns    |
| $P\_DAT[15:0]$ becomes valid after $\overline{P\_ADS}$ positive edge       | $t_{DO2}$     | —             | —    | —   | 13.0  | ns    |
| $P\_DAT[15:0]$ becomes invalid after $\overline{P\_ADS}$ positive edge     | $t_{DX}$      | —             | 3.0  | —   | —     | ns    |
| $P\_DAT[15:0]$ goes tristate after $\overline{P\_CS}$ positive edge        | $t_{DZ}$      | —             | 12.0 | —   | 45.0  | ns    |
| $P\_DAT[15:0]$ goes tristate after $\overline{P\_ADS}$ positive edge       | $t_{DZ}$      | —             | 12.0 | —   | 45.0  | ns    |
| $\overline{P\_ADS}$ first LOW pulse width                                  | $t_{PW1\_r}$  | —             | 70.0 | —   | —     | ns    |
| $\overline{P\_ADS}$ subsequent LOW pulse widths                            | $t_{PW2\_r}$  | 1.2           | 8.9  | —   | —     | ns    |
| $\overline{P\_ADS}$ HIGH between pulses                                    | $t_{ADSH\_r}$ | 1.2           | 8.9  | —   | —     | ns    |
| $\overline{P\_CS}$ HIGH before next read/write cycle                       | $t_{CSH\_r}$  | 5             | 37.0 | —   | —     | ns    |
| Frequency during auto-increment read                                       | —             | —             | —    | —   | 56.25 | MHz   |
| Frequency for back-to-back single reads in auto-increment mode             | —             | —             | —    | —   | 8.54  | MHz   |

# 4.12.2 Serial Host Interface Specifications

The Gennum Serial Peripheral Interface (GSPI) handles the communication with an external host over the SPI port. It allows configuration of the Control and Status Registers (CSR) using serial read and write operations.

The GX3290 GSPI is selected by setting the  $\overline{\text{HOST\_S/P}}$  pin HIGH.

**Note 1:** The  $\overline{\text{P\_CS}}$  pin must be pulled LOW when  $\overline{\text{HOST\_S/P}}$  is set HIGH for serial port communication.

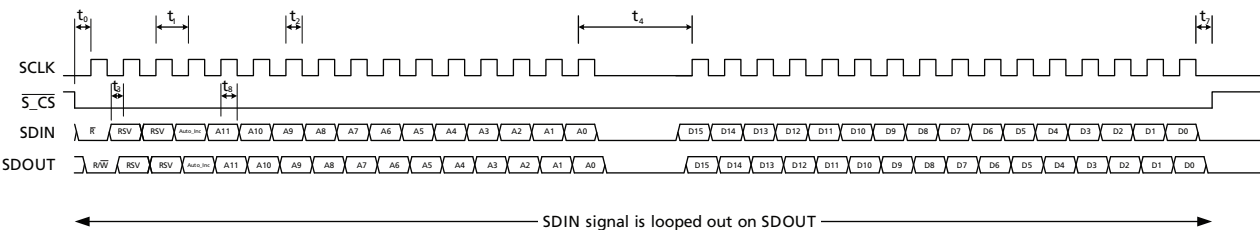
The GX3290 uses a four-wire protocol, with serial communication via the input SDIN pin, the output SDOUT pin, clock input signal (SCLK), and the chip select signal ( $\overline{\text{S\_CS}}$ ). The signalling rate can be up to 25Mb/s. The interface uses 16-bit data and a 16-bit address/control. The 16-bit address and control consists of a 12-bit address, one read/write bit ('1' for read, '0' for write), one bit for auto-increment and two unused bits. The four-wire protocol is implemented as shown in Figure 4-10 and Figure 4-11.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation.

If the Auto-Increment bit is set HIGH, the following Data Word is written into the address specified in the Command Word, and subsequent Data Words are written into incremental addresses from the first Data Word. This facilitates multiple address reads or writes without sending a Command Word for each Data Word.

**Table 4-17: GSPI Inputs/Outputs**

| Signal Name               | I/O | Reference Clock | Description                                            |
|---------------------------|-----|-----------------|--------------------------------------------------------|
| SCLK                      | I   | —               | GSPI clock                                             |
| SDIN                      | I   | SCLK            | GSPI serial data input                                 |
| SDOUT                     | O   | SCLK            | GSPI serial data output (on the negative edge of SCLK) |
| $\overline{\text{S\_CS}}$ | I   | —               | GSPI Chip Select                                       |



**Figure 4-10: Serial Host Interface Timing Diagram - Write Mode**

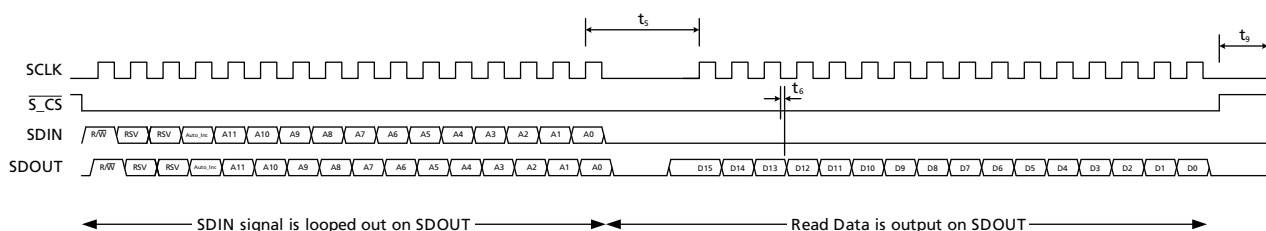


Figure 4-11: Serial Host Interface Timing Diagram - Read Mode

Table 4-18: Serial Host Interface Timing

| Parameter                                                                                                                                   | Symbol | Conditions                            | Equiv. Cycles | Min  | Typ  | Max    | Units |
|---------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------|---------------|------|------|--------|-------|
| $\overline{S\_CS}$ LOW before SCLK positive edge                                                                                            | t0     |                                       | —             | 7.0  | —    | —      | ns    |
| SCLK frequency                                                                                                                              | —      |                                       | —             | 0.1  | —    | 25.0   | MHz   |
| SCLK period                                                                                                                                 | t1     |                                       | —             | 40.0 | —    | 10,000 | ns    |
| SCLK duty cycle                                                                                                                             | t2     |                                       | —             | 40.0 | 50.0 | 60.0   | %     |
| Input data setup time                                                                                                                       | t3     |                                       | —             | 7.0  | —    | —      | ns    |
| Time between end of Command Word (or previous data word in Auto-Increment mode) and the first SCLK of the following Data Word - write cycle | t4     | 50% levels;<br>3.3V or 1.8V operation | —             | 40.0 | —    | —      | ns    |
| Time between end of Command Word (or previous data word in Auto-Increment mode) and the first SCLK of the following Data Word - read cycle  | t5     |                                       | —             | 70.0 | —    | —      | ns    |
| SDO hold time after SCLK negative edge                                                                                                      | t6     |                                       | —             | 5.0  | —    | 16.0   | ns    |
| $\overline{S\_CS}$ HIGH after last SCLK negative edge                                                                                       | t7     |                                       | 1.2           | 9.0  | —    | —      | ns    |
| Input data hold time                                                                                                                        | t8     |                                       | —             | 5.0  | —    | —      | ns    |
| $\overline{S\_CS}$ HIGH time                                                                                                                | t9     |                                       | 2.5           | 18.5 | —    | —      | ns    |

70ns (t5) = 5 clock cycles at 135MHz plus SCLK and SDO signal propagation.

18.5ns (t9) = 2.5 clock cycles at 135MHz.

Max t6 (16ns) represents the latest time by which the SDO will be stable after the SCLK negative edge. As SDO must be sampled on the SCLK positive edge, this determines the minimum SCLK period, and therefore the maximum SCLK frequency.

SDO maximum transition time with 15pF load: 2ns.

SDO maximum transition time with 50pF load: 5ns.

**Note 2:** The GSPI and APPI are mutually exclusive (they can not both be used at the same time).



## 5. Application Information

**Note:** Please refer to the following supplementary documents:

- [Crosspoint Design Guide](#)
- [EB-GX3290 Schematics, PCB Layout and Bill of Materials](#)

### 5.1 Power Supply Filtering and Recommendations

One of the most important steps that PCB designers can take to ensure power supply integrity for the GX3290 device is to design the PCB layer stack-up to minimize power plane pair inductance. Locating supply planes adjacent to ground planes, and separated by minimum thickness dielectrics in the stack-up, will minimize plane-pair inductance, and incidentally maximize the plane pair capacitance. Holes and cuts in the planes should be avoided as much as possible. While such closely spaced plane pairs allow the lowest inductance connections to supply pins of the GX3290 when they are closest to the device mounting surface of the PCB, the need to balance PCB stack-ups will lead to closely spaced layers on the far side of the PCB.

The supply currents drawn from the VDD\_18 and VDDIO\_D supplies are noisy and activity dependent, and the corresponding supply/ground plane pairs should be treated as for FPGA or CPU devices. Supply currents drawn from the VCC\_25\_A, VCC\_IN1, VCC\_IN2, VCC\_OUT1 and VCC\_OUT2 supplies are continuous except under changes of the high speed signal path configuration. The VCC\_OUT1 and VCC\_OUT2 supplies in particular are subject to rapid steps in current under some configuration changes: the maximum combined current draw of the VCC\_OUT1 and VCC\_OUT2 supplies, 8.52A, can be switched in as little as 10ns. This current step may be reduced by appropriate programming of the device.

Locating point of use voltage regulators close to the GX3290 device on the PCB will maximize the regulation roll-off frequency. At the highest frequencies, the GX3290 package and mounting parasitics will limit the effectiveness of any measures on the PCB to suppress voltage ripple on the device supplies. In between the voltage regulator roll off frequencies and the frequencies where parasitics on each supply domain within the GX3290 isolate the die from the PCB, decoupling capacitors on the PCB are effective. PCB layout effort should be spent on details of the decoupling capacitor mounting layout. Some simple layout measures can help to reduce the inductance of capacitor mounting.

See the [Crosspoint Design Guide](#) for more detailed recommendations.

## 5.2 Estimated Worst-Case Load Current Steps

Under normal operation, the power supply networks need to minimize voltage transients due to configuration change related load current steps. When the device reset is asserted while the device is drawing significant current, the load on power supplies could be shed fast enough to raise concerns about the board level voltage regulator dynamics, and the impact of any power supply network inductance.

### 5.2.1 VCC\_25\_A Supply

The tail currents of CML blocks (the high-speed signal paths) in the matrix switch relatively slowly, with worst case switching times of 30ns and typical times ~50ns. The matrix supply current of ~9.4A could in principle switch in 30ns, but in practice the propagation delay of UPDATE\_EN[7:0] signals across the matrix will increase the switching time somewhat.

The VCC\_25\_A supply current drawn by individual EQs takes more than 10ns to rise upon application of control signals. The VCC\_25\_A supply current drops in as little as 5ns upon assertion of reset, though, and the reset signal arrival times at EQs in a bank are roughly uniformly distributed over an interval of 0.8ns. This means that the VCC\_25\_A current drawn by all EQs together, ~3.2A, could be shed in 5.8ns.

The trace drivers draw significant current from the VCC\_25\_A supply, up to ~4.1A total for all trace drivers together, and this current can rise in as little as 20ns upon the de-assertion of power-down signals, or fall in as little as 1ns upon the assertion of power-down or reset signals. The arrival times of power-down or reset signals within the bottom trace driver bank are nearly uniformly distributed over an interval of 0.8ns, while the arrival time of power-down or reset signals within the top trace driver bank are nearly uniformly distributed over an interval of 4.4ns.

The worst case total load current slew rate on the VCC\_25\_A supply is estimated from the above to be ~2.2GA/s.

### 5.2.2 VCC\_OUT1, VCC\_OUT2 Supplies

In simulation, the tail currents of trace driver output stages turn on in as little as 10ns. Should all outputs be configured for maximum swing and enabled simultaneously, the load current step on each of VCC\_OUT1, VCC\_OUT2 would be as high as 4.26A (for AC-coupled applications) in ~14ns, 11ns respectively (including the propagation delay spread noted above). That large dI/dt can be reduced by appropriate programming of updates. The VCC\_OUT1 and VCC\_OUT2 supply current drawn by each trace driver drops in as little as 1ns upon the assertion of device reset. The greater spread of signal arrival times in the top bank leads to a significantly smaller magnitude of dI/dt on the VCC\_OUT1 supply than on the VCC\_OUT2 supply.

### 5.2.3 VCC\_IN1, VCC\_IN2 Supplies

The controls for the equalizers are serialized, and hence power switching of the equalizers in mission mode is staggered in time. Assertion of reset will however lead to more nearly synchronous shedding of load. The typical current drawn from the VCC\_IN1 and VCC\_IN2 supplies is 1.75A each, and this can be shed in 1ns, including the reset signal propagation delay.

**Table 5-1: Summary**

| Supply   | Maximum Current (A) | Maximum Positive $di/dt$ | Maximum Negative $di/dt$<br>(reset/simultaneous power-down) |
|----------|---------------------|--------------------------|-------------------------------------------------------------|
| VCC_25_A | 16.7                | 0.81GA/s                 | -2.2GA/s                                                    |
| VCC_OUT1 | 4.26                | 0.42GA/s                 | -1.4GA/s                                                    |
| VCC_OUT2 | 4.26                | 0.54GA/s                 | -3.6GA/s                                                    |
| VCC_IN1  | 1.75(typ)           | <0.1GA/s                 | -1.8GA/s                                                    |
| VCC_IN2  | 1.75(typ)           | <0.1GA/s                 | -1.8GA/s                                                    |

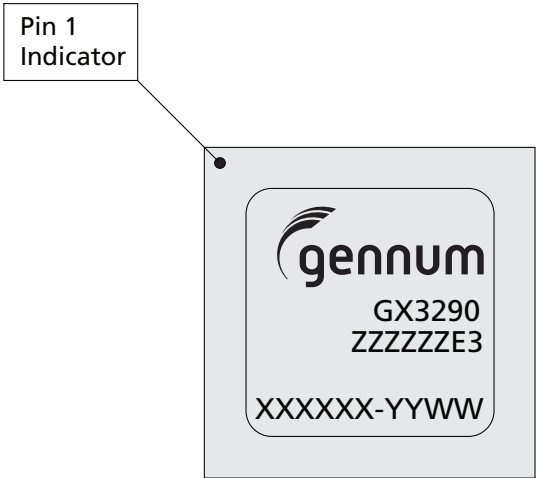


# 6.2 Package Thermal Data and Information

Table 6-1: Package Thermal Data and Information

| Parameter                                                            | Value                                                                                          |
|----------------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| Package Type                                                         | 50mm x 50mm HFC BGA                                                                            |
| Moisture Sensitivity Level                                           | 3                                                                                              |
| Junction to Case Thermal Resistance, $\theta_{j-c}$                  | 0.31°C/W                                                                                       |
| Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow) | N/A. This device requires a heat sink. See Semtech's <a href="#">Crosspoint Design Guide</a> . |
| Junction to Board Thermal Resistance, $\theta_{j-b}$                 | 2.1°C/W                                                                                        |
| Pb-free and RoHS Compliant                                           | Yes                                                                                            |

# 6.3 Marking Diagram



|               |                                       |
|---------------|---------------------------------------|
| Instructions: |                                       |
| GX3290        | Package Mark                          |
| ZZZZZ         | Marking batch work order information  |
| E3            | Pb-free & Green indicator             |
| XXXXXX        | Assembly batch work order information |
| YYWW          | Date Code                             |

Figure 6-2: Marking Diagram

# 6.4 Solder Reflow Profile

The GX3290 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-3.

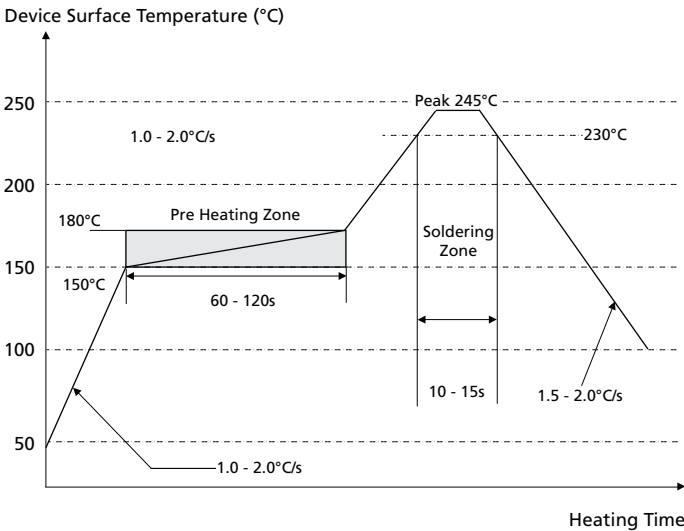


Figure 6-3: Maximum Pb-free Solder Reflow Profile

# 6.5 Ordering Information

Table 6-2: Ordering Information

| Part Number | Package         | Temperature Range |
|-------------|-----------------|-------------------|
| GX3290-CBE3 | 50x50mm HFC-BGA | 0°C to 85°C       |

# Appendix - Relevant Documentation

Table 6-3: Relevant Documentation

| Document Description                                         | Document Identification |
|--------------------------------------------------------------|-------------------------|
| EB-GX3290 Schematics, PCB Layout and Bill of Materials       | GENDOC-056057           |
| GX3290 Host Control Software User Manual                     | GENDOC-055970           |
| Using the Monitoring Features of the GX3290 Application Note | GENDOC-058329           |
| GX3290 (and family) Crosspoint Ball Guide                    | GENDOC-056697           |
| Crosspoint Design Guide                                      | GENDOC-056004           |
| Crosspoint (GX3290 and family) Reference Manual (for CSRs)   | GENDOC-056832           |



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