

DS3486 Quad RS-422, RS-423 Line Receiver

Check for Samples: [DS3486](#)

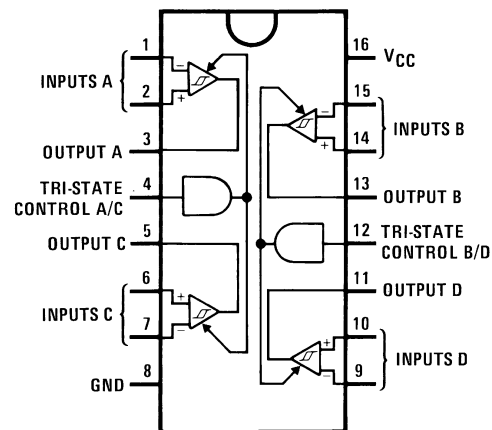
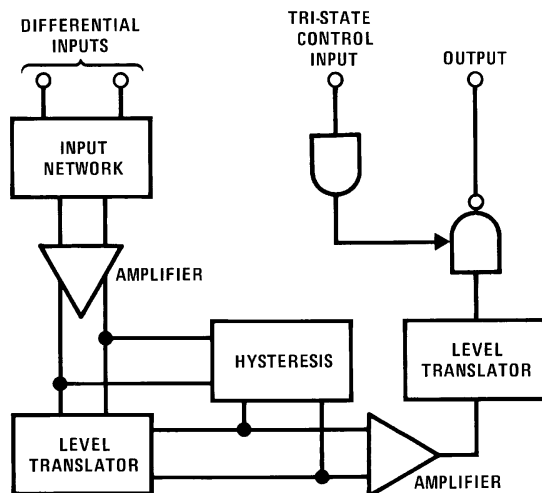
FEATURES

- Four Independent Receivers
- TRI-STATE Outputs
- Internal Hysteresis –140 mV (typ)
- Fast Propagation Times –19 ns (typ)
- TTL Compatible Outputs
- 5V Supply
- Pin Compatible and Interchangeable with MC3486

DESCRIPTION

Texas Instruments' quad RS-422, RS-423 receiver features four independent receivers which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

Block and Connection Diagrams



**Figure 1. Dual-In-Line Package
Top View
D-16 (SOIC) Package or NFG0016E (PDIP)
Package**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Power Supply Voltage, V_{CC}	8V
Input Common-Mode Voltage, V_{ICM}	$\pm 25V$
Input Differential Voltage, V_{ID}	$\pm 25V$
TRI-STATE Control Input Voltage, V_I	8V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	$-65^{\circ}C$ to $+150^{\circ}C$
Maximum Power Dissipation ⁽³⁾ at $25^{\circ}C$	
Molded PDIP Package	1362 mW
SOIC Package	1002 mW
SOIC Package Thermal Resistance	
θ_{JA}	$+124.5^{\circ}C/W$
θ_{JC}	$+41.2^{\circ}C/W$

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Derate PDIP molded package 10.2 mW/ $^{\circ}C$ above $25^{\circ}C$. Derate SOIC package 8.01 mW/ $^{\circ}C$ above $25^{\circ}C$.

Operating Conditions

	Max	Min	Units
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	$^{\circ}C$
Input Common-Mode Voltage Range, V_{ICR}	-7.0	7.0	V

Electrical Characteristics⁽¹⁾

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^{\circ}C$, $V_{CC} = 5V$ and $V_{IC} = 0V$.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage—High Logic State (TRI-STATE Control)		2.0			V
V_{IL}	Input Voltage—Low Logic State (TRI-STATE Control)				0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage	$-7V \leq V_{IC} \leq 7V$, V_{IH} TRI-STATE = 2V $I_O = -0.4$ mA, $V_{OH} \geq 2.7V$		0.070	0.2	V
		$I_O = 8$ mA, $V_{OL} \geq 0.5V$		0.070	-0.2	V
$I_{IB(D)}$	Input Bias Current	$V_{CC} = 0V$ or $5.25V$, Other Inputs at $0V$				
		$V_I = -10V$			-3.25	mA
		$V_I = -3V$			-1.50	mA
		$V_I = 3V$			1.50	mA
		$V_I = 10V$			3.25	mA
	Input Balance	$-7V \leq V_{IC} \leq 7V$, $V_{IH(3C)} = 2V$, (2)				
		V_{OH} $I_O = -0.4$ mA, $V_{ID} = 0.4V$	2.7			V
		V_{OL} $I_O = 8$ mA, $V_{ID} = -0.4V$			0.5	V

- (1) All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
- (2) Refer to EIA RS-422/3 for exact conditions.

Electrical Characteristics ⁽¹⁾ (continued)

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$ and $V_{IC} = 0\text{V}$.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OZ}	Output TRI-STATE Leakage Current	$V_{I(D)} = 3\text{V}$, $V_{IL} = 0.8\text{V}$, $V_{OL} = 0.5\text{V}$			-40	μA
		$V_{I(D)} = -3\text{V}$, $V_{IL} = 0.8\text{V}$, $V_{OH} = 2.7\text{V}$			40	μA
I_{OS}	Output Short-Circuit Current	$V_{I(D)} = 3\text{V}$, $V_{IH\text{TRI-STATE}} = 2\text{V}$, $V_O = 0\text{V}$, ⁽³⁾	-15		-100	mA
I_{IL}	Input Current—Low Logic State (TRI-STATE Control)	$V_{IL} = 0.5\text{V}$			-100	μA
I_{IH}	Input Current—High Logic State (TRI-STATE Control)	$V_{IH} = 2.7\text{V}$			20	μA
		$V_{IH} = 5.25\text{V}$			100	μA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	$I_{IN} = -10\text{ mA}$			-1.5	V
I_{CC}	Power Supply Current	All Inputs $V_{IL} = 0\text{V}$			85	mA

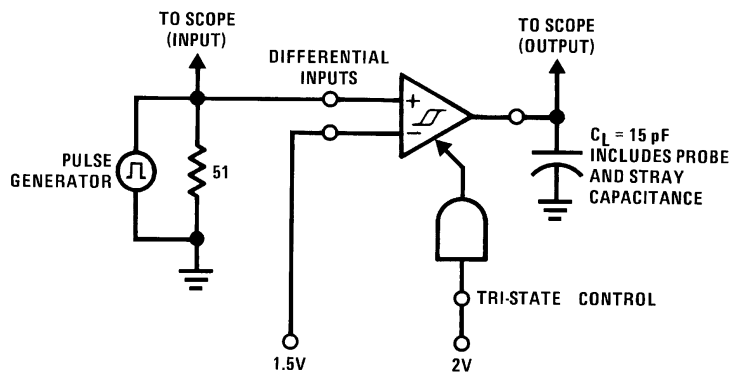
(3) Only one output at a time should be shorted.

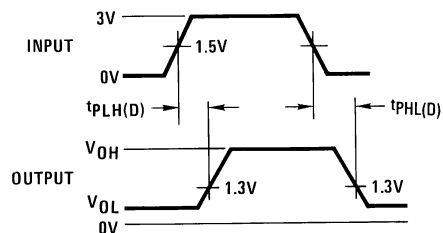
Switching Characteristics

(Unless otherwise noted, $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.)

Symbol	Parameter	Min	Typ	Max	Units
$t_{PHL(D)}$	Propagation Delay Time—Differential Inputs to Output Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
t_{PLZ}	TRI-STATE Control to Output Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

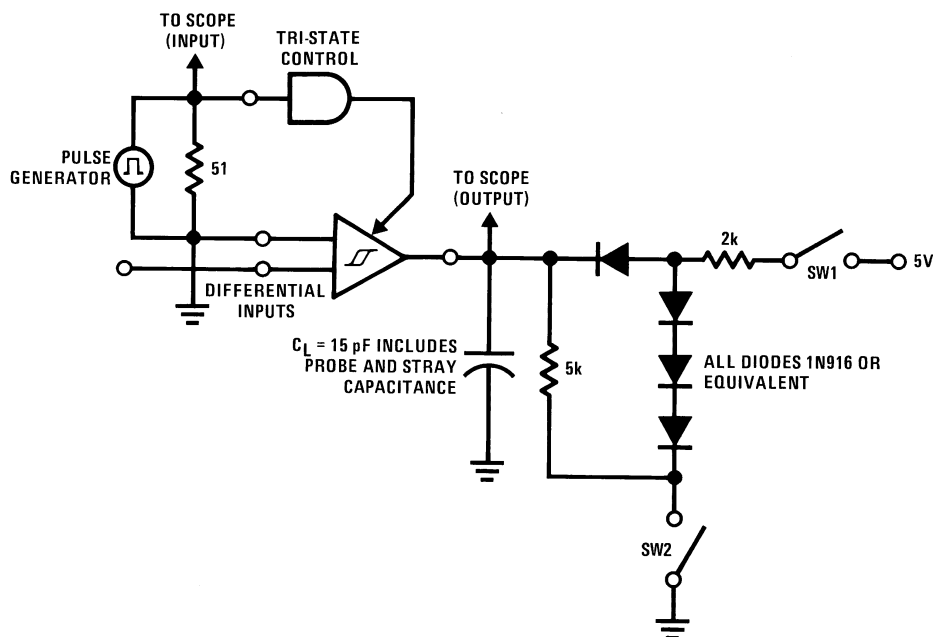
AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



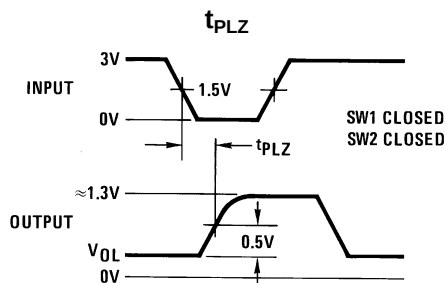


Input pulse characteristics:
 $t_{TLH} = t_{THL} = 6 \text{ ns}$ (10% to 90%)
 PRR = 1 MHz, 50% duty cycle

Figure 2. Propagation Delay Differential Input to Output



1.5V for t_{PHZ} and t_{PLZ}
 1.5V for t_{PLZ} and t_{PZL}
 Input pulse characteristics:
 $t_{TLH} = t_{THL} = 6 \text{ ns}$ (10% to 90%)
 PRR = 1 MHz, 50% duty cycle



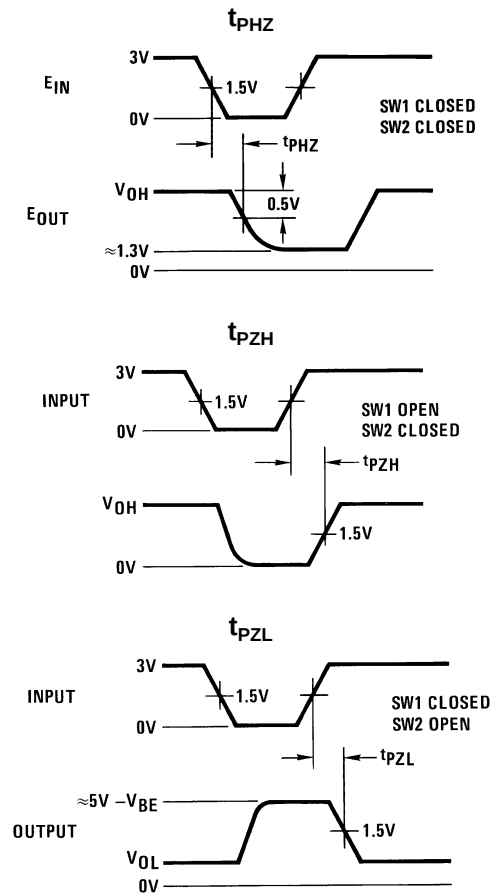


Figure 3. Propagation Delay TRI-STATE Control Input to Output

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D

Page

- Changed layout of National Data Sheet to TI format [5](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS3486M/NOPB	Active	Production	SOIC (D) 16	48 TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS3486M
DS3486M/NOPB.B	Active	Production	SOIC (D) 16	48 TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS3486M
DS3486MX/NOPB	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS3486M
DS3486MX/NOPB.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS3486M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

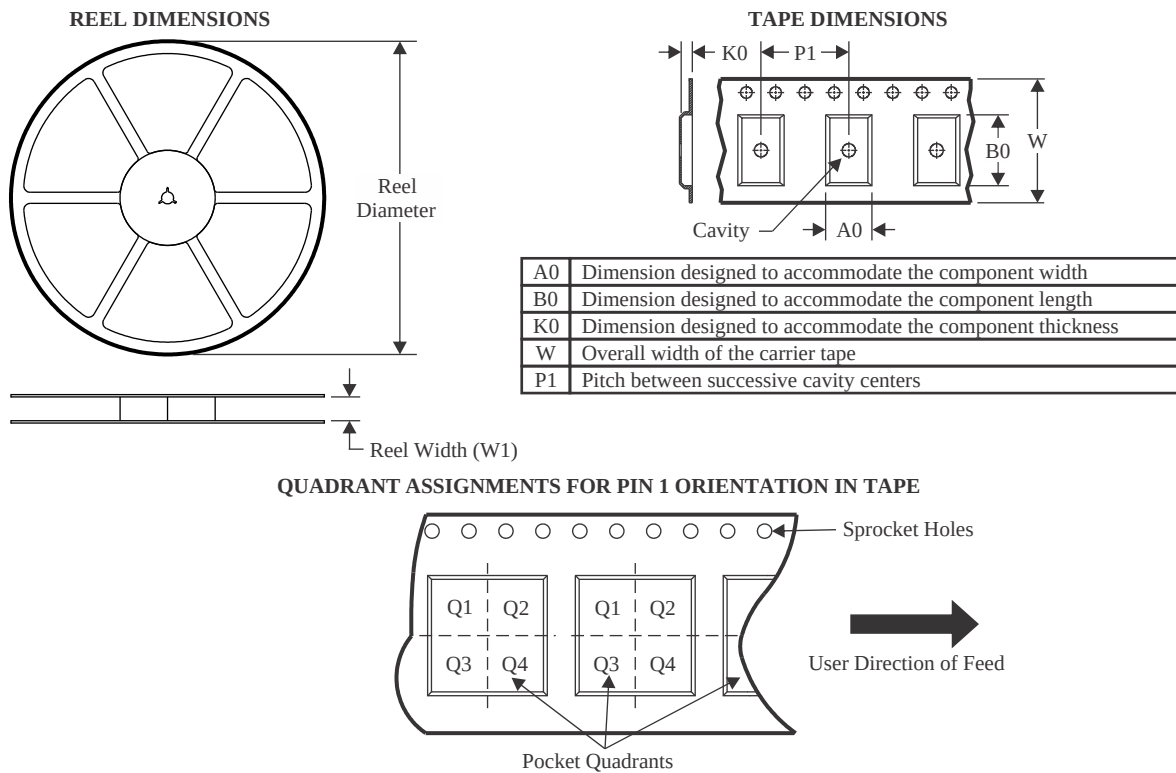
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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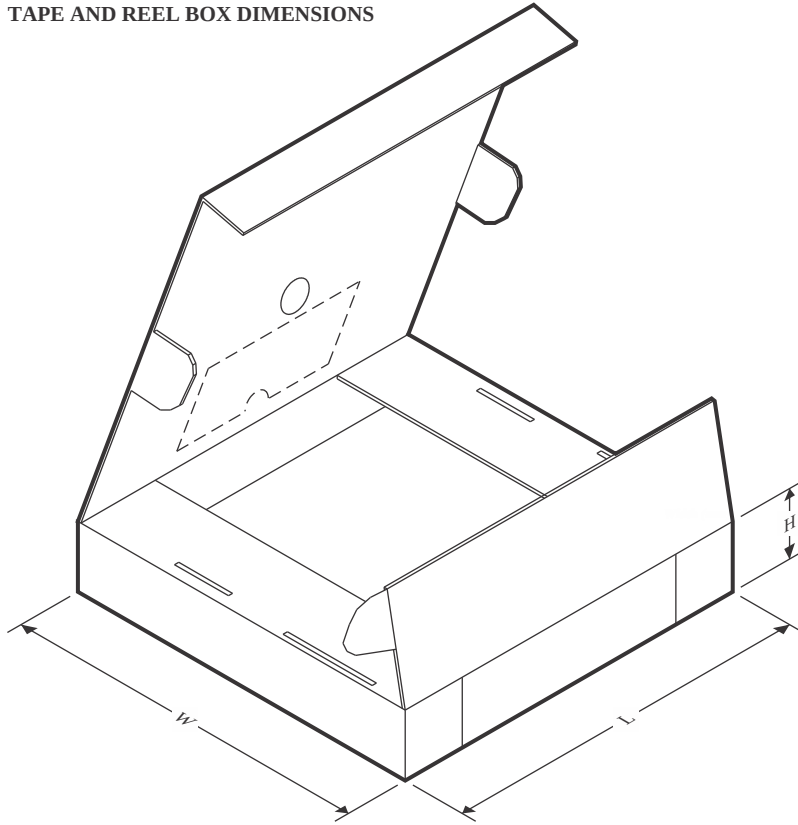
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3486MX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

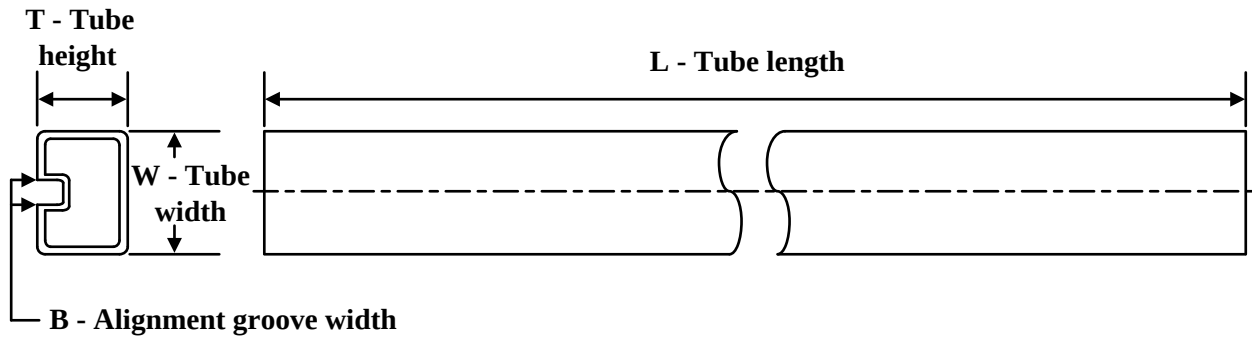
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3486MX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

TUBE

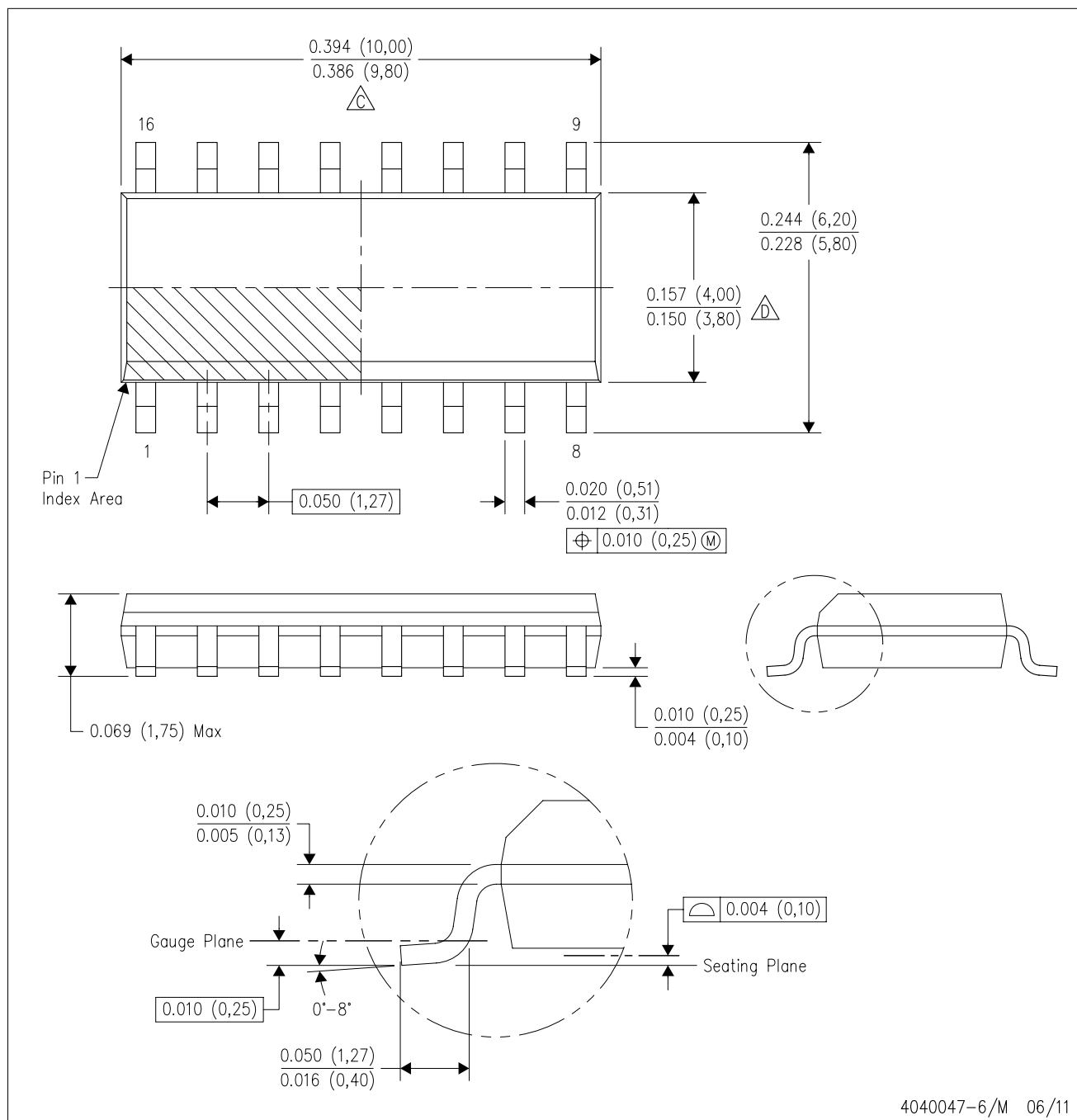


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS3486M/NOPB	D	SOIC	16	48	495	8	4064	3.05
DS3486M/NOPB.B	D	SOIC	16	48	495	8	4064	3.05

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

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