

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

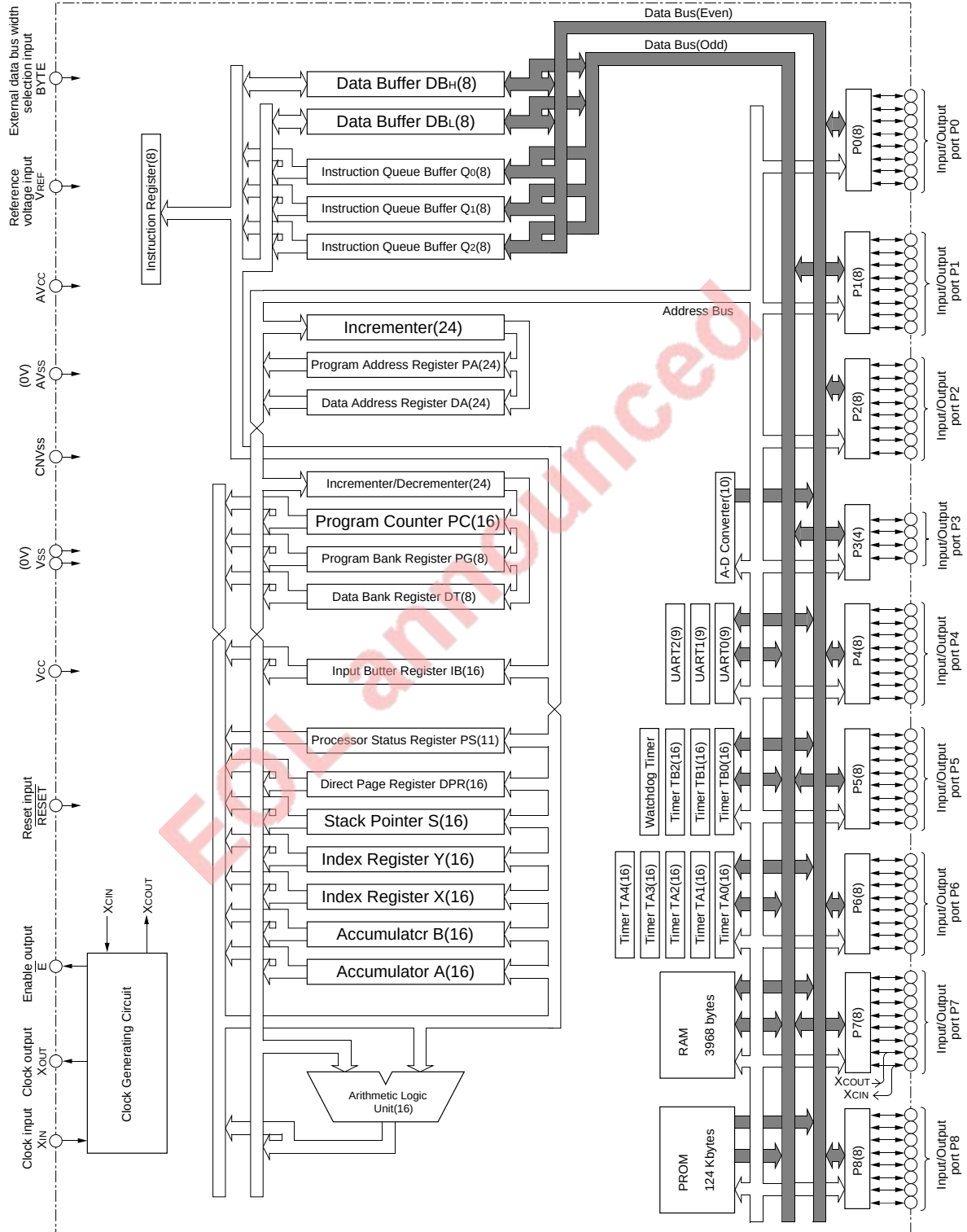
Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M37735EBXXXXFP
M37735EBBFS

PROM VERSION OF M37735MHBXXXXFP

M37735EBXXXXFP BLOCK DIAGRAM



M37735EHBXXXFP
M37735EHBFS

PROM VERSION OF M37735MHBXXXFP

FUNCTIONS OF M37735EHBXXXFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		160 ns (the fastest instruction at external clock 25 MHz frequency)
Memory size	PROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit X 8
	P3	4-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		5 V $\pm$ 10%
Power dissipation		47.5 mW (at external clock 25 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 1 Mbytes
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package	M37735EHBXXXFP	80-pin plastic molded QFP (80P6N-A)
	M37735EHBFS	80-pin ceramic LCC (with a window) (80D0)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 5 V $\pm$ 10% to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
$\bar{E}$	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the memory expansion mode or the microprocessor mode, this pin functions as the RDE signal output pin.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P0 ₀ – P0 ₇	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output $\overline{CS_0}$ – $\overline{CS_4}$, $\overline{RSM}$ signals, and address (A ₁₆ , A ₁₇).
P1 ₀ – P1 ₇	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D ₈ – D ₁₅) is input/output or an address (A ₈ – A ₁₅) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A ₈ – A ₁₅) is output.
P2 ₀ – P2 ₇	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D ₀ – D ₇) is input/output or an address (A ₀ – A ₇) is output.
P3 ₀ – P3 ₃	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, $\overline{WEL}$, $\overline{WEH}$, ALE, and HLDA signals are output.
P4 ₀ – P4 ₇	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P4 ₀ , P4 ₁ , and P4 ₂ become $\overline{HOLD}$ and $\overline{RDY}$ input pins, and a clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P4 ₂ can be selected as an I/O port.
P5 ₀ – P5 ₇	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ($\overline{KI_0}$ – $\overline{KI_3}$).
P6 ₀ – P6 ₇	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT_0}$ – $\overline{INT_2}$) and input pins for timers B0 to B2. P6 ₇ also functions as a sub-clock ϕ_{SUB} output pin.
P7 ₀ – P7 ₇	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. P7 ₂ to P7 ₅ also function as I/O pins for UART2. Additionally, P7 ₆ and P7 ₇ have the function as the output pin (Xc _{OUT}) and the input pin (Xc _{IN}) of the sub-clock (32 kHz) oscillation circuit, respectively. When P7 ₆ and P7 ₇ are used as the Xc _{OUT} and Xc _{IN} pins, connect a resonator or an oscillator between the both.
P8 ₀ – P8 ₇	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
VCC, VSS	Power supply		Supply 5V±10% to Vcc and 0V to Vss.
CNVSS	VPP input	Input	Connect to VPP when programming or verifying.
BYTE	VPP input	Input	Connect to VPP when programming or verifying.
RESET	Reset input	Input	Connect to Vss.
XIN	Clock input	Input	Connect a ceramic resonator between XIN and XOUT.
XOUT	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AVCC, AVSS	Analog supply input		Connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	Connect to Vss.
P00 – P07	Address input (A0 – A7)	Input	Port P0 functions as the lower 8 bits address input (A0 – A7).
P10 – P17	Address input (A8 – A15)	Input	Port P1 functions as the higher 8 bits address input (A8 – A15).
P20 – P27	Data I/O (D0 – D7)	I/O	Port P2 functions as the 8 bits data bus (D0 – D7).
P30	Address input (A16)	Input	P30 functions as the most significant bit address input (A16).
P31 – P33	Input port P3	Input	Connect to Vss.
P40 – P47	Input port P4	Input	Connect to Vss.
P50 – P57	Control signal input	Input	P50, P51 and P52 function as PGM, $\overline{OE}$ and $\overline{CE}$ input pins respectively. Connect P53, P54, P55 and P56 to Vcc. Connect P57 to Vss.
P60 – P67	Input port P6	Input	Connect to Vss.
P70 – P77	Input port P7	Input	Connect to Vss.
P80 – P87	Input port P8	Input	Connect to Vss.

BASIC FUNCTION BLOCKS

The M37735EBXXXXFP has the same functions as the M37735MHBXXXXFP except for the following:

- (1) The built-in ROM is PROM.
- (2) The status of bit 3 of the oscillation circuit control register 1 (address 6F₁₆) at a reset is different.
- (3) The usage condition of bit 3 of the oscillation circuit control register 1 is different.
- (4) Part of the processor mode selection method is different.

Accordingly, refer to the basic function blocks description in the M37735MHBXXXXFP except for Figure 1 (bit configuration of oscillation circuit control register 1), Figure 3 (microcomputer internal status during reset), and Table 1 (microprocessor mode selection method).

In the M37735EBXXXXFP, bit 3 of the oscillation circuit control register 1 must be "0". (Refer to Figure 1.) Bit 3 is "1" at a reset. Accordingly,

write "0" to bit 3 in the single-chip mode after reset.

Figure 2 shows how to write data in oscillation circuit control register 1.

In the M37735EBXXXXFP, the microprocessor mode cannot be selected by connecting the CNVss pin to Vcc. Connect the CNVss pin to Vss and start the microcomputer's operating from the single-chip mode.

Table 1. Relationship between CNVss pin input level and processor modes

CNVss	Mode	Description
Vss	· Single-chip · Memory expansion · Microprocessor	Single-chip mode upon starting after reset. Each mode can be selected by changing the processor mode bits by software.

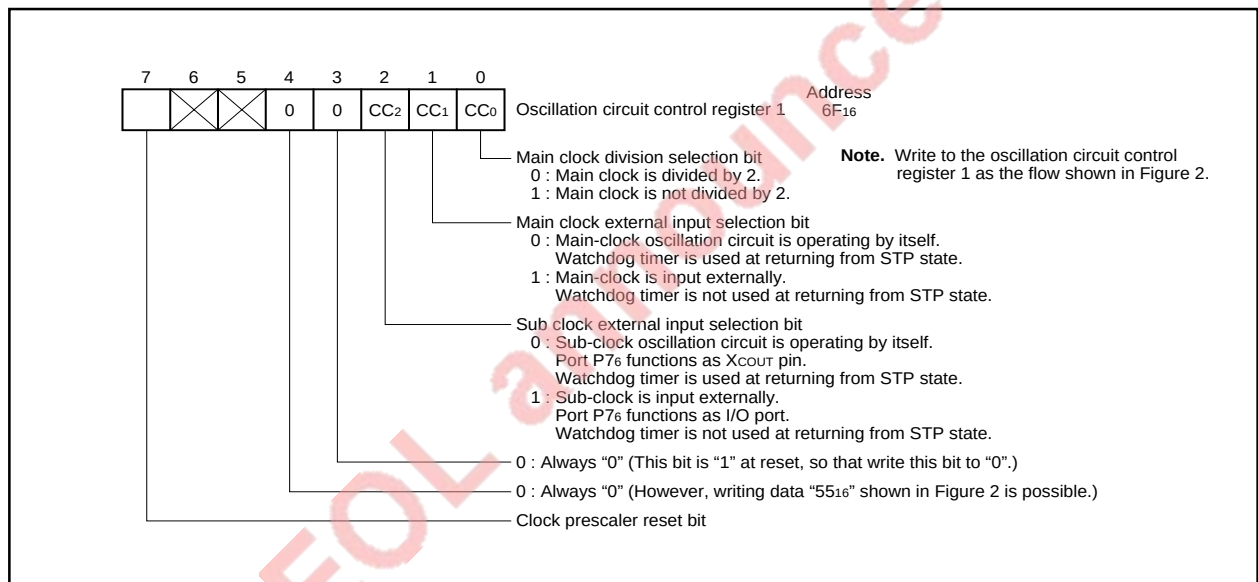


Fig. 1 Bit configuration of oscillation circuit control register 1 (corresponding to Figure 63 in data sheet "M37735MHBXXXXFP")

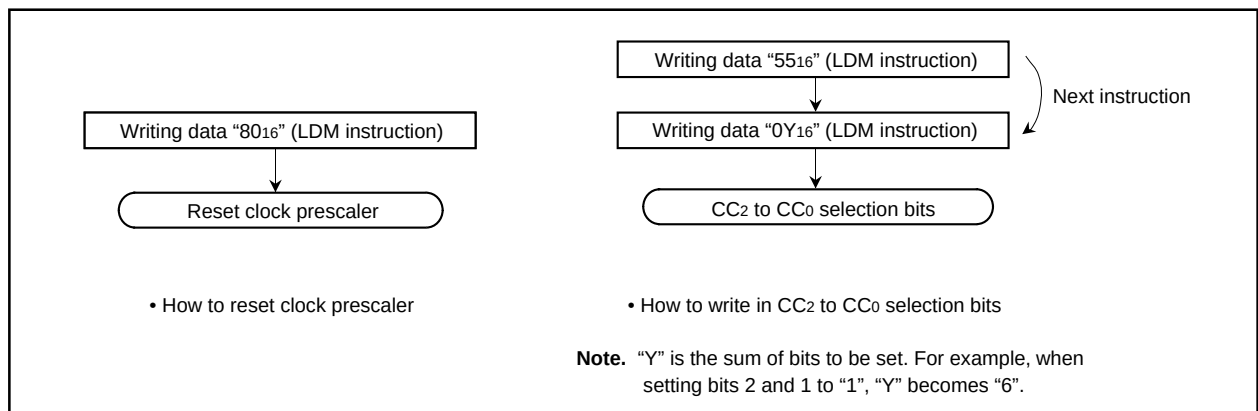


Fig. 2 How to write data in oscillation circuit control register 1 (identical with Figure 64 in data sheet "M37735MHBXXXXFP")

	Address		Address
Port P0 direction register	(04 ₁₆)... 00 ₁₆	Watchdog timer frequency selection flag	(61 ₁₆)...         0
Port P1 direction register	(05 ₁₆)... 00 ₁₆	Memory allocation control register	(63 ₁₆)...    0 0 0 0 0
Port P2 direction register	(08 ₁₆)... 00 ₁₆	UART2 transmit/receive mode register	(64 ₁₆)...  0 0 0 0 0 0 0
Port P3 direction register	(09 ₁₆)...     0 0 0 0	UART2 transmit/receive control register 0	(68 ₁₆)...     1 0 0 0
Port P4 direction register	(0C ₁₆)... 00 ₁₆	UART2 transmit/receive control register 1	(69 ₁₆)... 0 0 0 0 0 0 1 0
Port P5 direction register	(0D ₁₆)... 00 ₁₆	Oscillation circuit control register 0	(6C ₁₆)...  0 0 0 0 0  1
Port P6 direction register	(10 ₁₆)... 00 ₁₆	Port function control register	(6D ₁₆)... 00 ₁₆
Port P7 direction register	(11 ₁₆)... 00 ₁₆	Serial transmit control register	(6E ₁₆)...   0 0    
Port P8 direction register	(14 ₁₆)... 00 ₁₆	Oscillation circuit control register 1	(6F ₁₆)... 0   0 1 0 0 0
A-D control register 0	(1E ₁₆)... 0 0 0 0 0 ? ? ?	A-D/UART2 trans./rece. interrupt control register	(70 ₁₆)...     0 0 0 0
A-D control register 1	(1F ₁₆)...   0 0 0  1 1	UART 0 transmission interrupt control register	(71 ₁₆)...     0 0 0 0
UART 0 transmit/receive mode register	(30 ₁₆)... 00 ₁₆	UART 0 receive interrupt control register	(72 ₁₆)...     0 0 0 0
UART 1 transmit/receive mode register	(38 ₁₆)... 00 ₁₆	UART 1 transmission interrupt control register	(73 ₁₆)...     0 0 0 0
UART 0 transmit/receive control register 0	(34 ₁₆)... 0 0 0 0 1 0 0 0	UART 1 receive interrupt control register	(74 ₁₆)...     0 0 0 0
UART 1 transmit/receive control register 0	(3C ₁₆)... 0 0 0 0 1 0 0 0	Timer A0 interrupt control register	(75 ₁₆)...     0 0 0 0
UART 0 transmit/receive control register 1	(35 ₁₆)... 0 0 0 0 0 0 1 0	Timer A1 interrupt control register	(76 ₁₆)...     0 0 0 0
UART 1 transmit/receive control register 1	(3D ₁₆)... 0 0 0 0 0 0 1 0	Timer A2 interrupt control register	(77 ₁₆)...     0 0 0 0
Count start flag	(40 ₁₆)... 00 ₁₆	Timer A3 interrupt control register	(78 ₁₆)...     0 0 0 0
One-shot start flag	(42 ₁₆)...    0 0 0 0 0	Timer A4 interrupt control register	(79 ₁₆)...     0 0 0 0
Up-down flag	(44 ₁₆)... 00 ₁₆	Timer B0 interrupt control register	(7A ₁₆)...     0 0 0 0
Timer A0 mode register	(56 ₁₆)... 00 ₁₆	Timer B1 interrupt control register	(7B ₁₆)...     0 0 0 0
Timer A1 mode register	(57 ₁₆)... 00 ₁₆	Timer B2 interrupt control register	(7C ₁₆)...     0 0 0 0
Timer A2 mode register	(58 ₁₆)... 00 ₁₆	INT0 interrupt control register	(7D ₁₆)...  0 0 0 0 0 0
Timer A3 mode register	(59 ₁₆)... 00 ₁₆	INT1 interrupt control register	(7E ₁₆)...  0 0 0 0 0 0
Timer A4 mode register	(5A ₁₆)... 00 ₁₆	INT2/Key input interrupt control register	(7F ₁₆)...  0 0 0 0 0 0
Timer B0 mode register	(5B ₁₆)... 0 0 1 0 0 0 0 0	Processor status register (PS)	0 0 0 ? ? 0 0 0 1 ? ?
Timer B1 mode register	(5C ₁₆)... 0 0 1  0 0 0 0	Program bank register (PG)	00 ₁₆
Timer B2 mode register	(5D ₁₆)... 0 0 1  0 0 0 0	Program counter (PC _H)	Content of FFFF ₁₆
Processor mode register 0	(5E ₁₆)... 00 ₁₆	Program counter (PC _L)	Content of FFFE ₁₆
Processor mode register 1	(5F ₁₆)...       0	Direct page register (DPR)	0000 ₁₆
Watchdog timer register	(60 ₁₆)... FFF ₁₆	Data bank register (DT)	00 ₁₆

Contents of other registers and RAM are undefined during reset. Initialize them by software.

Fig. 3 Microcomputer internal status during reset

EPROM MODE

The M37735EBXXXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 2 list the correspondence between pins and Figure 4 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, P30, P50, P51, P52, CNVss, and BYTE are used for the EPROM (equivalent to the

M5M27C101K).

When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 01000₁₆ – 1FFFF₁₆.

Connect the clock which is either ceramic resonator or external clock to XIN pin and XOUT pin.

Table 2 Pin function in EPROM mode

	M37735EBXXXXFP	M5M27C101K
VCC	VCC	VCC
VPP	CNVss, BYTE	VPP
VSS	VSS	VSS
Address input	Ports P0, P1, P30	A0 – A16
Data I/O	Port P2	D0 – D7
CE	P52	CE
OE	P51	OE
PGM	P50	PGM

EOL announced

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37735EHBXXXFP M37735EHBFS

PROM VERSION OF M37735MHBXXXFP

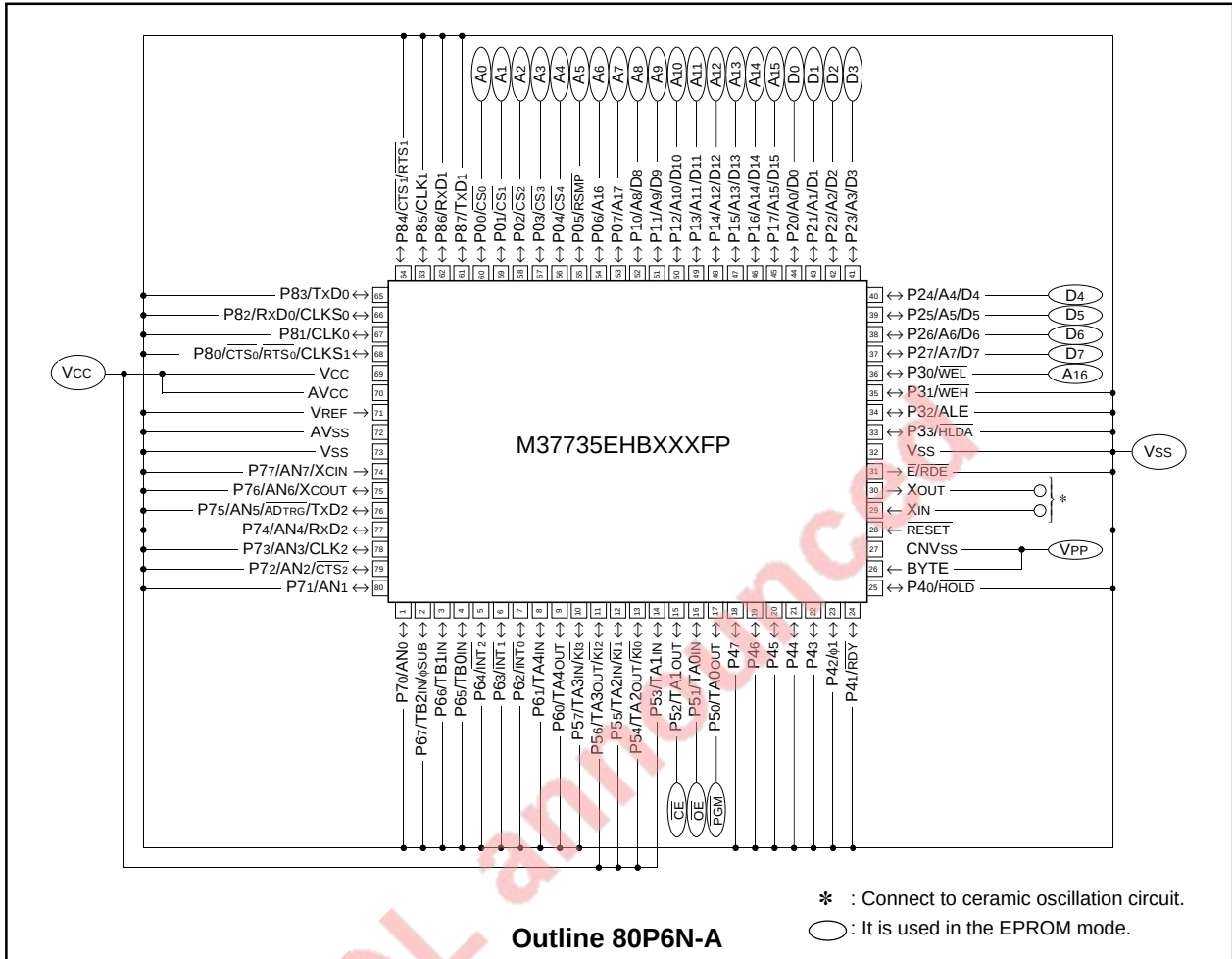


Fig. 4 Pin connection in EPROM mode

FUNCTION IN EPROM MODE 1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins to a "L" level. Input the address of the data ($A_0 - A_{16}$) to be read, and the data will be output to the I/O pins $D_0 - D_7$. The data I/O pins will be floating when either the $\overline{\text{CE}}$ or $\overline{\text{OE}}$ pins are in the "H" state.

Programming

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the $\overline{\text{CE}}$ pin to a "L" level and the $\overline{\text{OE}}$ pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the V_{PP} pin. The address to be programmed to is selected with pins $A_0 - A_{16}$, and the data to be programmed is input to pins $D_0 - D_7$. Set the $\overline{\text{PGM}}$ pin to a "L" level to being programming.

Erasing

To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15 J/cm².

Programming operation

To program the M37735EHBXXXFP, first set $V_{CC} = 6 \text{ V}$, $V_{PP} = 12.5 \text{ V}$, and set the address to 0100016. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 X X ms).

When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been programmed, read with $V_{CC} = V_{PP} = 5 \text{ V}$ (or $V_{CC} = V_{PP} = 5.5 \text{ V}$).

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	V_{PP}	V_{CC}	Data I/O
Read-out	V _{IL}	V _{IL}	X	5 V	5 V	Output
Output	V _{IL}	V _{IH}	X	5 V	5 V	Floating
Disable	V _{IH}	X	X	5 V	5 V	Floating
Programming	V _{IL}	V _{IH}	V _{IL}	12.5 V	6 V	Input
Programming Verify	V _{IL}	V _{IL}	V _{IH}	12.5 V	6 V	Output
Program Disable	V _{IH}	V _{IH}	V _{IH}	12.5 V	6 V	Floating

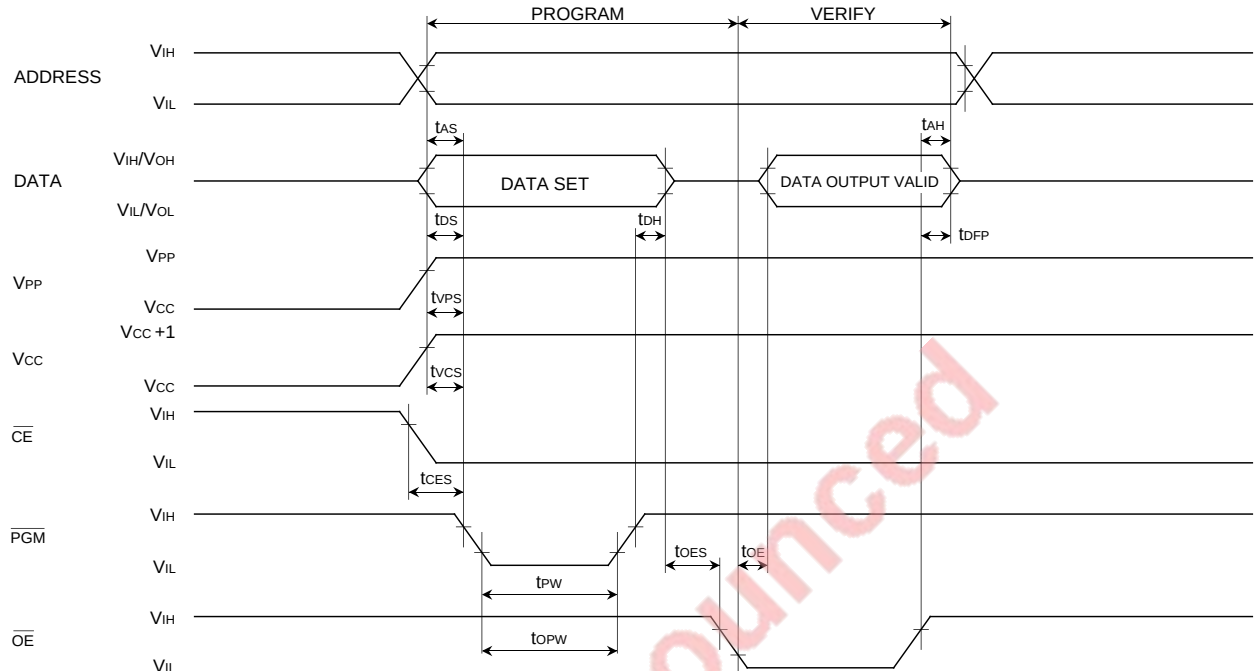
Note 1 : An X indicates either V_{IL} or V_{IH}.

Programming operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \pm 0.3 \text{ V}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{AS}	Address setup time		2			μs
t _{OES}	$\overline{\text{OE}}$ setup time		2			μs
t _{DS}	Data setup time		2			μs
t _{AH}	Address hold time		0			μs
t _{DH}	Data hold time		2			μs
t _{DFP}	Output enable to output float delay		0		130	ns
t _{VCS}	V_{CC} setup time		2			μs
t _{VPS}	V_{PP} setup time		2			μs
t _{PW}	$\overline{\text{PGM}}$ pulse width		0.19	0.2	0.21	ms
t _{OPW}	$\overline{\text{PGM}}$ over program pulse width		0.19		5.25	ms
t _{CES}	$\overline{\text{CE}}$ setup time		2			μs
t _{OE}	Data valid from $\overline{\text{OE}}$				150	ns

AC waveforms



Test conditions for A.C. characteristics

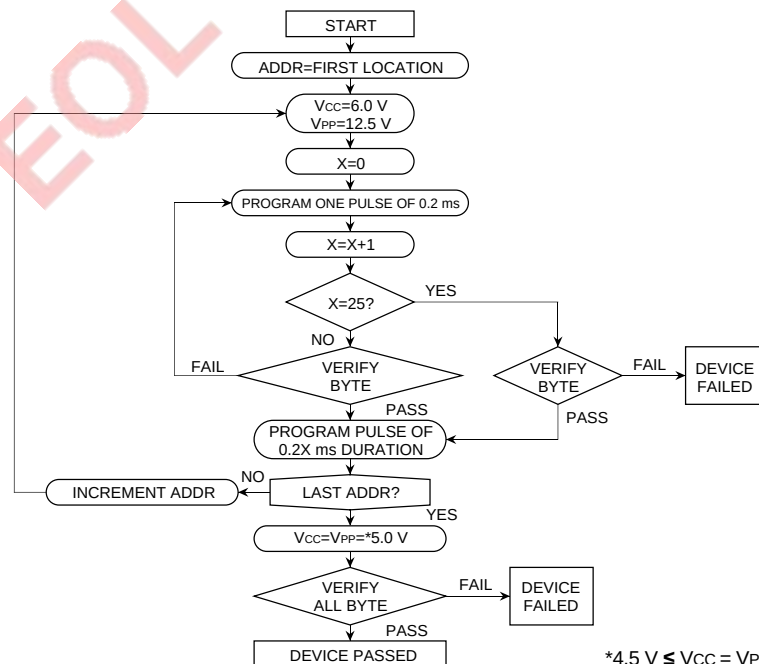
Input voltage : $V_{IL} = 0.45 \text{ V}$, $V_{IH} = 2.4 \text{ V}$

Input rise and fall times (10 % – 90 %) : $\leq 20 \text{ ns}$

Reference voltage at timing measurement : Input, Output

"L" = 0.8 V, "H" = 2 V

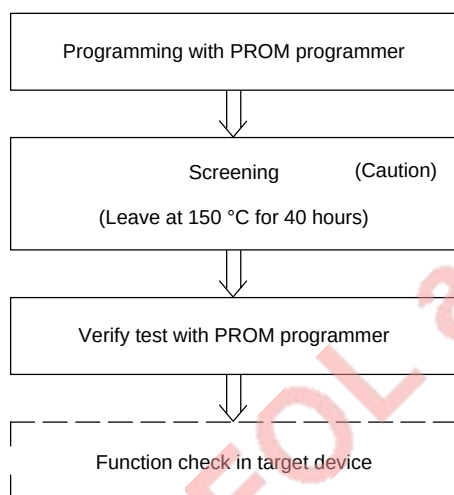
Programming algorithm flow chart



*4.5 V $\leq$ VCC = VPP $\leq$ 5.5 V

SAFETY INSTRUCTIONS

- (1) Sunlight and fluorescent lamp contain light that can erase written information. When using in read mode, be sure to cover the transparent glass portion with a seal or other materials (ceramic package product).
- (2) Mitsubishi Electric corp. provides the seal for covering the transparent glass. Take care that the seal does not touch the read pins (ceramic package product).
- (3) Clean the transparent glass before erasing. Fingers' fat and paste disturb the passage of ultraviolet rays and may affect badly the erasure capability (ceramic package product).
- (4) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
- (5) The programmable M37735EHBFP that is shipped in blank is also provided. For the M37735EHBFP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.



Caution : Never expose to 150 °C exceeding 100 hours.

ADDRESSING MODES

The M37735EHBXXXFP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37735EHBXXXFP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.

- (1) M37735EHBXXXFP writing to PROM order confirmation form
- (2) 80P6N mark specification form
- (3) ROM data (EPROM 3 sets)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		−0.3 to +7	V
AV _{cc}	Analog power source voltage		−0.3 to +7	V
V _I	Input voltage RESET, CNVss, BYTE		−0.3 to +12 (Note)	V
V _I	Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, VREF, X _{IN}		−0.3 to V _{cc} + 0.3	V
V _O	Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{OUT} , E		−0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	300	mW
T _{opr}	Operating temperature		−20 to +85	°C
T _{stg}	Storage temperature		−40 to +150	°C

Note. When the EPROM is programmed, input voltage of pins CNVss and BYTE is 13 V respectively.

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 5 V ± 10%, T_a = −20 to +85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{cc}	Power source voltage	f(X _{IN}) : Operating	4.5	5.0	5.5	V
		f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz	2.7		5.5	
AV _{cc}	Analog power source voltage			V _{cc}		V
V _{ss}	Power source voltage			0		V
AV _{ss}	Analog power source voltage			0		V
V _{IH}	High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{IN} , RESET, CNVss, BYTE, X _{CIN} (Note 3)		0.8 V _{cc}		V _{cc}	V
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)		0.8 V _{cc}		V _{cc}	V
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)		0.5 V _{cc}		V _{cc}	V
V _{IL}	Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{IN} , RESET, CNVss, BYTE, X _{CIN} (Note 3)		0		0.2V _{cc}	V
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)		0		0.2V _{cc}	V
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)		0		0.16V _{cc}	V
I _{OH(peak)}	High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87				−10	mA
I _{OH(avg)}	High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87				−5	mA
I _{OL(peak)}	Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87				10	mA
I _{OL(peak)}	Low-level peak output current P44 – P47, P50 – P53				20	mA
I _{OL(avg)}	Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87				5	mA
I _{OL(avg)}	Low-level average output current P44 – P47, P50 – P53				15	mA
f(X _{IN})	Main-clock oscillation frequency (Note 4)				25	MHz
f(X _{CIN})	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

- The sum of I_{OL(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, and P7 must be 80 mA or less.
- Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".
- The maximum value of f(X_{IN}) = 12.5 MHz when the main clock division selection bit = "1".

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	$I_{OH} = -10\text{ mA}$	3			V
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OH} = -400\text{ }\mu\text{A}$	4.7			V
V_{OH}	High-level output voltage P30 – P32	$I_{OH} = -10\text{ mA}$	3.1			V
		$I_{CH} = -400\text{ }\mu\text{A}$	4.8			
V_{OH}	High-level output voltage $\bar{E}$	$I_{OH} = -10\text{ mA}$	3.4			V
		$I_{OH} = -400\text{ }\mu\text{A}$	4.8			
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P43, P54 – P57, P60 – P67, P70 – P75, P80 – P87	$I_{OL} = 10\text{ mA}$			2	V
V_{OL}	Low-level output voltage P44 – P47, P50 – P53	$I_{OL} = 20\text{ mA}$			2	V
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OL} = 2\text{ mA}$			0.45	V
V_{OL}	Low-level output voltage P30 – P32	$I_{OL} = 10\text{ mA}$			1.9	V
		$I_{OL} = 2\text{ mA}$			0.43	
V_{OL}	Low-level output voltage $\bar{E}$	$I_{OL} = 10\text{ mA}$			1.6	V
		$I_{OL} = 2\text{ mA}$			0.4	
$V_{T+} - V_{T-}$	Hysteresis $\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, $\overline{\text{TA0IN}} - \overline{\text{TA4IN}}$, $\overline{\text{TB0IN}} - \overline{\text{TB2IN}}$, $\overline{\text{INT0}} - \overline{\text{INT2}}$, $\overline{\text{ADTRG}}$, $\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$, $\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{KI0}} - \overline{\text{KI3}}$		0.4		1	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{\text{RESET}}$		0.2		0.5	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{\text{XIN}}$		0.1		0.4	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{\text{XCIN}}$ (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, $\overline{\text{XIN}}$, $\overline{\text{RESET}}$, $\overline{\text{CNVss}}$, $\overline{\text{BYTE}}$	$V_i = 5\text{ V}$			5	μA
I_{IL}	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, $\overline{\text{XIN}}$, $\overline{\text{RESET}}$, $\overline{\text{CNVss}}$, $\overline{\text{BYTE}}$	$V_i = 0\text{ V}$			-5	μA
I_{IL}	Low-level input current P54 – P57, P62 – P64	$V_i = 0\text{ V}$, without a pull-up transistor			-5	μA
		$V_i = 0\text{ V}$, with a pull-up transistor	-0.25	-0.5	-1.0	mA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC}	Power source current	In single-chip mode, output pins are open, and other pins are V _{SS} . $V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), ($f(f_2) = 12.5\text{ MHz}$), $f(X_{CIN}) = 32.768\text{ kHz}$, in operating (Note 1)		9.5	19	mA
		$V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), ($f(f_2) = 1.5625\text{ MHz}$), $f(X_{CIN}) = \text{Stopped}$, in operating (Note 1)		1.3	2.6	mA
		$V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), $f(X_{CIN}) = 32.768\text{ kHz}$, when a WIT instruction is executed (Note 2)		10	20	μA
		$V_{CC} = 5\text{ V}$, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, in operating (Note 3)		50	100	μA
		$V_{CC} = 5\text{ V}$, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, when a WIT instruction is executed (Note 4)		5	10	μA
		$T_a = 25\text{ }^{\circ}\text{C}$, when clock is stopped			1	μA
		$T_a = 85\text{ }^{\circ}\text{C}$, when clock is stopped			20	μA

- Notes**
1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
 2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
 3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
 4. This applies when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
—	Absolute accuracy	$V_{REF} = V_{CC}$			± 3	LSB
R _{LADDER}	Ladder resistance	$V_{REF} = V_{CC}$	10		25	k Ω
t _{CONV}	Conversion time		9.44			μs
V _{REF}	Reference voltage		2		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

TIMING REQUIREMENTS (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = -20 to 85 °C, f(X_{IN}) = 25 MHz, unless otherwise noted (Note))

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c	External clock input cycle time (Note 3)	40		ns
t _{w(H)}	External clock input high-level pulse width (Note 4)	15		ns
t _{w(L)}	External clock input low-level pulse width (Note 4)	15		ns
t _r	External clock rise time		8	ns
t _f	External clock fall time		8	ns

Notes 3. When the main clock division selection bit = "1", the minimum value of t_c = 80 ns.

4. When the main clock division selection bit = "1", values of t_{w(H)} / t_c and t_{w(L)} / t_c must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{su} (P0D-E)	Port P0 input setup time	60		ns
t _{su} (P1D-E)	Port P1 input setup time	60		ns
t _{su} (P2D-E)	Port P2 input setup time	60		ns
t _{su} (P3D-E)	Port P3 input setup time	60		ns
t _{su} (P4D-E)	Port P4 input setup time	60		ns
t _{su} (P5D-E)	Port P5 input setup time	60		ns
t _{su} (P6D-E)	Port P6 input setup time	60		ns
t _{su} (P7D-E)	Port P7 input setup time	60		ns
t _{su} (P8D-E)	Port P8 input setup time	60		ns
t _h (E-P0D)	Port P0 input hold time	0		ns
t _h (E-P1D)	Port P1 input hold time	0		ns
t _h (E-P2D)	Port P2 input hold time	0		ns
t _h (E-P3D)	Port P3 input hold time	0		ns
t _h (E-P4D)	Port P4 input hold time	0		ns
t _h (E-P5D)	Port P5 input hold time	0		ns
t _h (E-P6D)	Port P6 input hold time	0		ns
t _h (E-P7D)	Port P7 input hold time	0		ns
t _h (E-P8D)	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{su} (D-RDE)	Data input setup time	32		ns
t _{su} (RDY-φ1)	RDY input setup time	55		ns
t _{su} (HOLD-φ1)	HOLD input setup time	55		ns
t _h (RDE-D)	Data input hold time	0		ns
t _h (φ1-RDY)	RDY input hold time	0		ns
t _h (φ1-HOLD)	HOLD input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TA _{in} input cycle time	80		ns
t _w (TAH)	TA _{in} input high-level pulse width	40		ns
t _w (TAL)	TA _{in} input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TA _{in} input cycle time (Note)	320		ns
t _w (TAH)	TA _{in} input high-level pulse width (Note)	160		ns
t _w (TAL)	TA _{in} input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TA _{in} input cycle time (Note)	320		ns
t _w (TAH)	TA _{in} input high-level pulse width	80		ns
t _w (TAL)	TA _{in} input low-level pulse width	80		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in pulse width modulation mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _w (TAH)	TA _{in} input high-level pulse width	80		ns
t _w (TAL)	TA _{in} input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (UP)	TA _{IOU} input cycle time	2000		ns
t _w (UPH)	TA _{IOU} input high-level pulse width	1000		ns
t _w (UPL)	TA _{IOU} input low-level pulse width	1000		ns
t _{su} (UP-T _{IN})	TA _{IOU} input setup time	400		ns
t _h (T _{IN} -UP)	TA _{IOU} input hold time	400		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TA _{JIN} input cycle time	800		ns
t _{su} (TA _{JIN} -TA _{JOUT})	TA _{JIN} input setup time	200		ns
t _{su} (TA _{JOUT} -TA _{JIN})	TA _{JOUT} input setup time	200		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TB _{IN} input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TB _{IN} input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TB _{IN} input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TB _{IN} input cycle time (both edges count)	160		ns
$t_{w(TBH)}$	TB _{IN} input high-level pulse width (both edges count)	80		ns
$t_{w(TBL)}$	TB _{IN} input low-level pulse width (both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TB _{IN} input cycle time (Note)	320		ns
$t_{w(TBH)}$	TB _{IN} input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TB _{IN} input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TB _{IN} input cycle time (Note)	320		ns
$t_{w(TBH)}$	TB _{IN} input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TB _{IN} input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	AD _{TRG} input cycle time (minimum allowable trigger)	1000		ns
$t_{w(ADL)}$	AD _{TRG} input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CLK)}$	CLK _i input cycle time	200		ns
$t_{w(CLKH)}$	CLK _i input high-level pulse width	100		ns
$t_{w(CLKL)}$	CLK _i input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxD _i output delay time		80	ns
$t_{h(C-Q)}$	TxD _i hold time	0		ns
$t_{su(D-C)}$	RxD _i input setup time	30		ns
$t_{h(C-D)}$	RxD _i input hold time	90		ns

External interrupt $\overline{INT}_i$ input, key input interrupt $\overline{KI}_i$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT}_i$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT}_i$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI}_i$ input low-level pulse width	250		ns

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiin input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAiin input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAiin input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiin input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiin input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBiin input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBiin input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37735MHBXXXFP".

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 5		80	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			80	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			80	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			80	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			80	ns

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

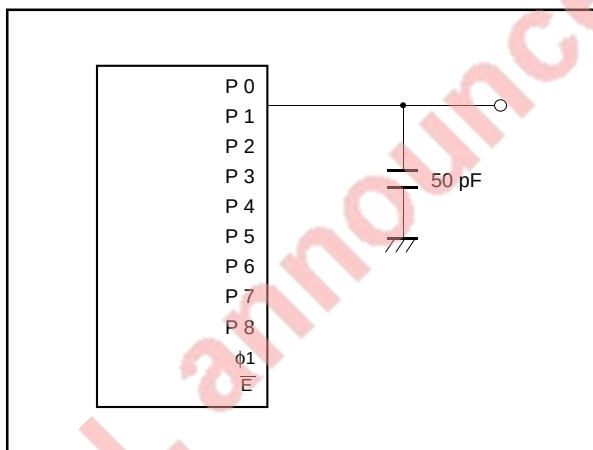


Fig. 5 Measuring circuit for ports P0 – P8 and ϕ_1

Memory expansion mode and microprocessor mode

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = -20 to 85 °C, f(X_{IN}) = 25 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
t _d (CS-WE) t _d (CS-RDE)	Chip-select output delay time	No wait	Fig. 5	12		ns
		Wait 1		87		ns
		Wait 0				
t _h (WE-CS) t _h (RDE-CS)	Chip-select hold time	No wait		4		ns
		Wait 1				
		Wait 0				
t _d (A _n -WE) t _d (A _n -RDE)	Address output delay time	No wait		12		ns
		Wait 1		87		ns
		Wait 0				
t _d (A-WE) t _d (A-RDE)	Address output delay time	No wait		12		ns
		Wait 1		75		ns
		Wait 0				
t _h (WE-A _n) t _h (RDE-A _n)	Address hold time	No wait		18		ns
		Wait 1				
		Wait 0				
t _w (ALE)	ALE pulse width	No wait		22		ns
		Wait 1		57		ns
		Wait 0				
t _{su} (A-ALE)	Address output setup time	No wait		5		ns
		Wait 1		45		ns
		Wait 0				
t _h (ALE-A)	Address hold time	No wait		9		ns
		Wait 1		15		ns
		Wait 0				
t _d (ALE-WE) t _d (ALE-RDE)	ALE output delay time	No wait		4		ns
		Wait 1		10		ns
		Wait 0				
t _d (WE-DQ)	Data output delay time				45	ns
t _h (WE-DQ)	Data hold time			18		ns
t _w (WE)	WE pulse width	No wait		50		ns
		Wait 1		130		ns
		Wait 0				
t _{pxz} (RDE-DZ)	Floating start delay time				5	ns
t _{pzx} (RDE-DZ)	Floating release delay time			20		ns
t _w (RDE)	RDE pulse width	No wait		48		ns
		Wait 1		128		ns
		Wait 0				
t _d (RSMP-WE) t _d (RSMP-RDE)	RSMP output delay time	No wait		10		ns
		Wait 1		0		ns
		Wait 0				
t _h (φ ₁ -RSMP)	RSMP hold time			0		ns
t _d (WE-φ ₁) t _d (RDE-φ ₁)	φ ₁ output delay time	No wait		0	18	ns
		Wait 1				
t _d (φ ₁ -HLDA)	HLDA output delay time				50	ns

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

Memory expansion mode and microprocessor mode

Bus timing data formulas ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Max., Note1), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time		4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{w(ALE)}$	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$		ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{h(ALE-A)}$	Address hold time	No wait	9		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$		ns
$t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$	ALE output delay time	No wait	4		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{d(WE-DQ)}$	Data output delay time			45	ns
$t_{h(WE-DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{w(WE)}$	$\overline{WE}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time			5	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 32$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 32$		ns
		Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 32$		ns
$t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$	RSMP output delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{h(\phi_1-RSMP)}$	RSMP hold time		0		ns
$t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$	ϕ_1 output delay time		0	18	ns

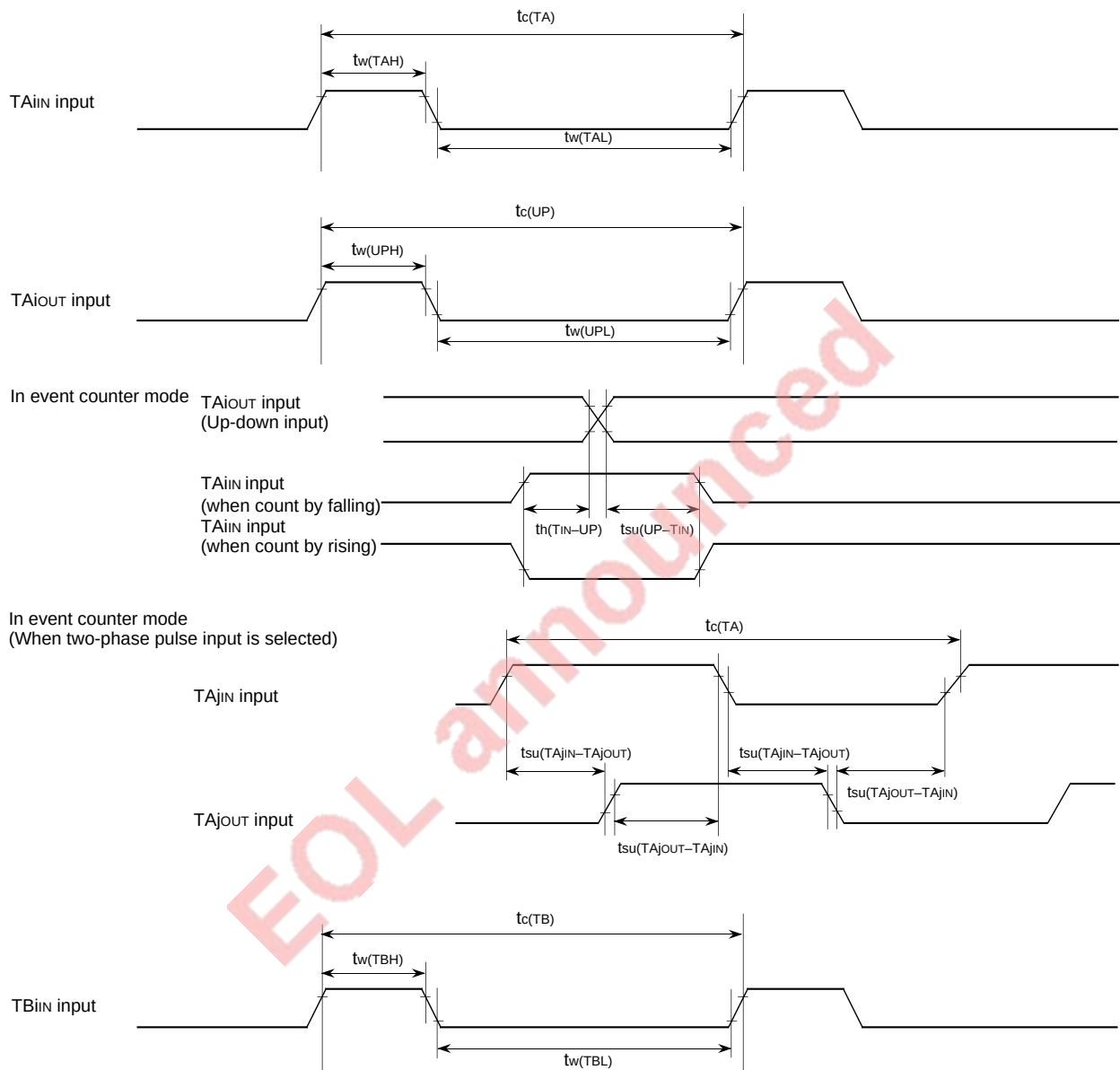
Notes 1. This applies when the main-clock division selection bit = "0".

2. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37735MHBXXXFP".

TIMING DIAGRAM



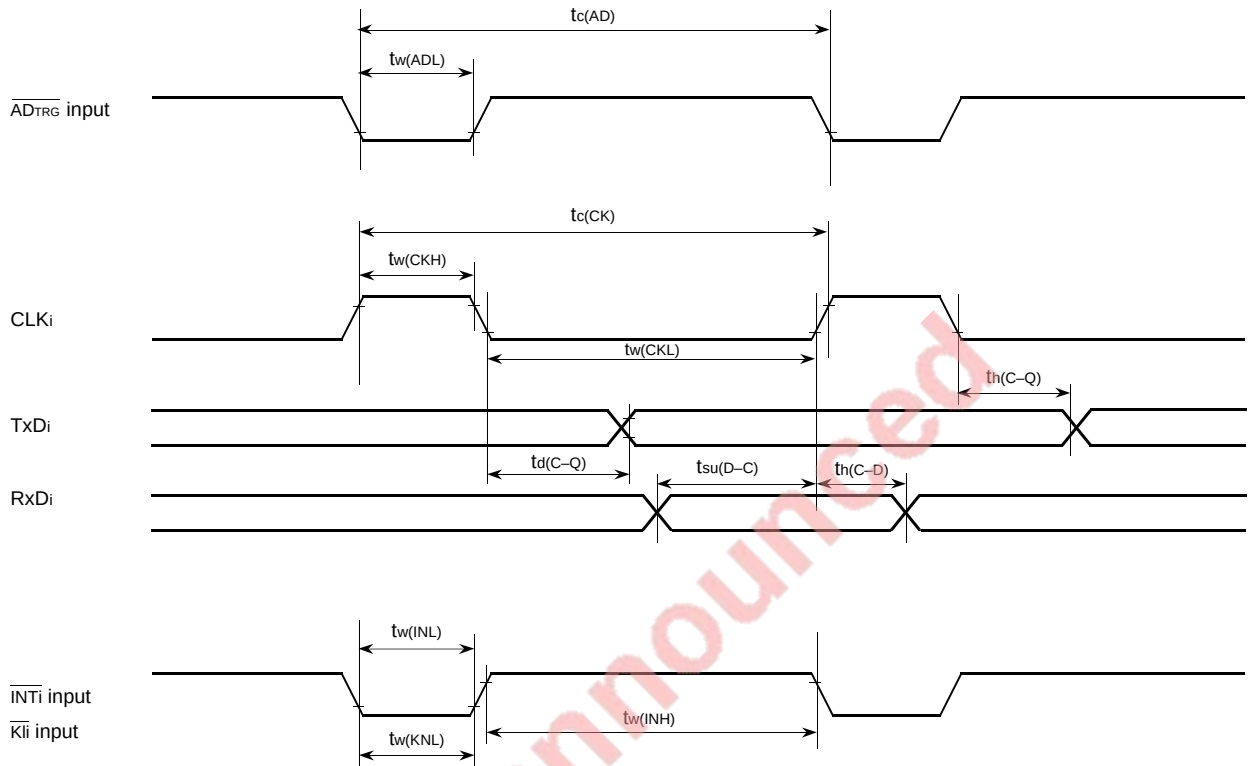


PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

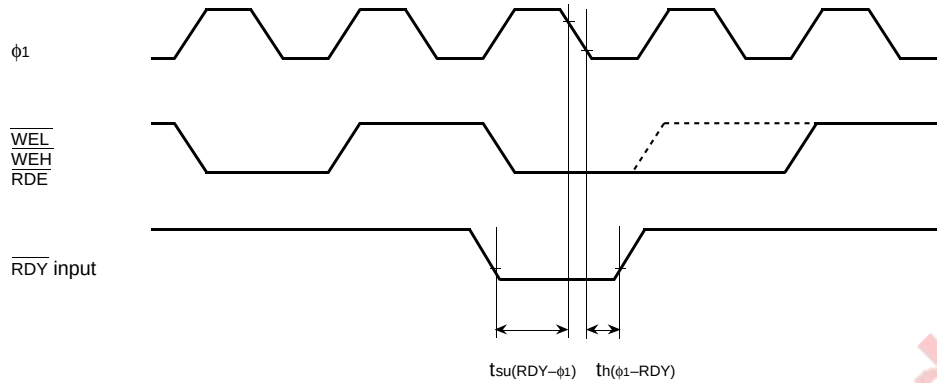
MITSUBISHI MICROCOMPUTERS

M37735EHBXXXFP M37735EHBFS

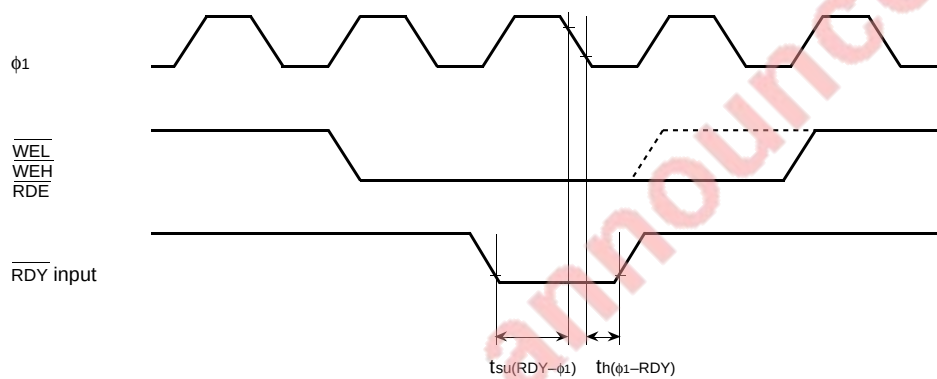
PROM VERSION OF M37735MHBXXXFP



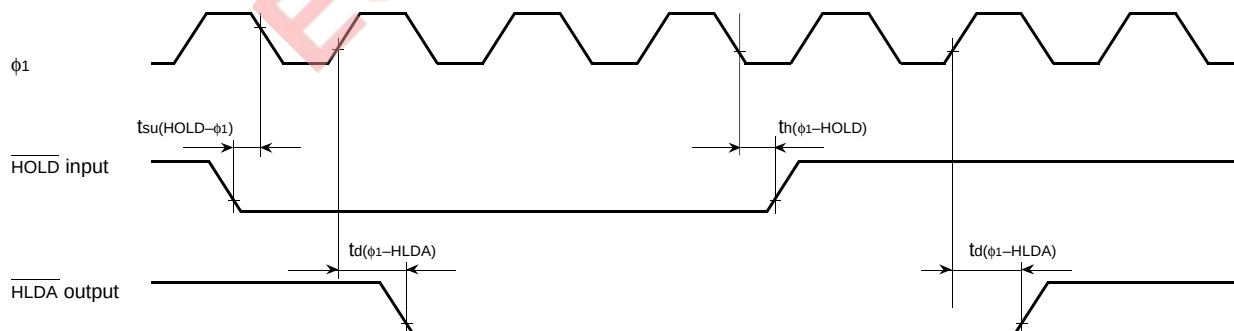
Memory expansion mode and microprocessor mode
 (When wait bit = "1")



(When wait bit = "0")



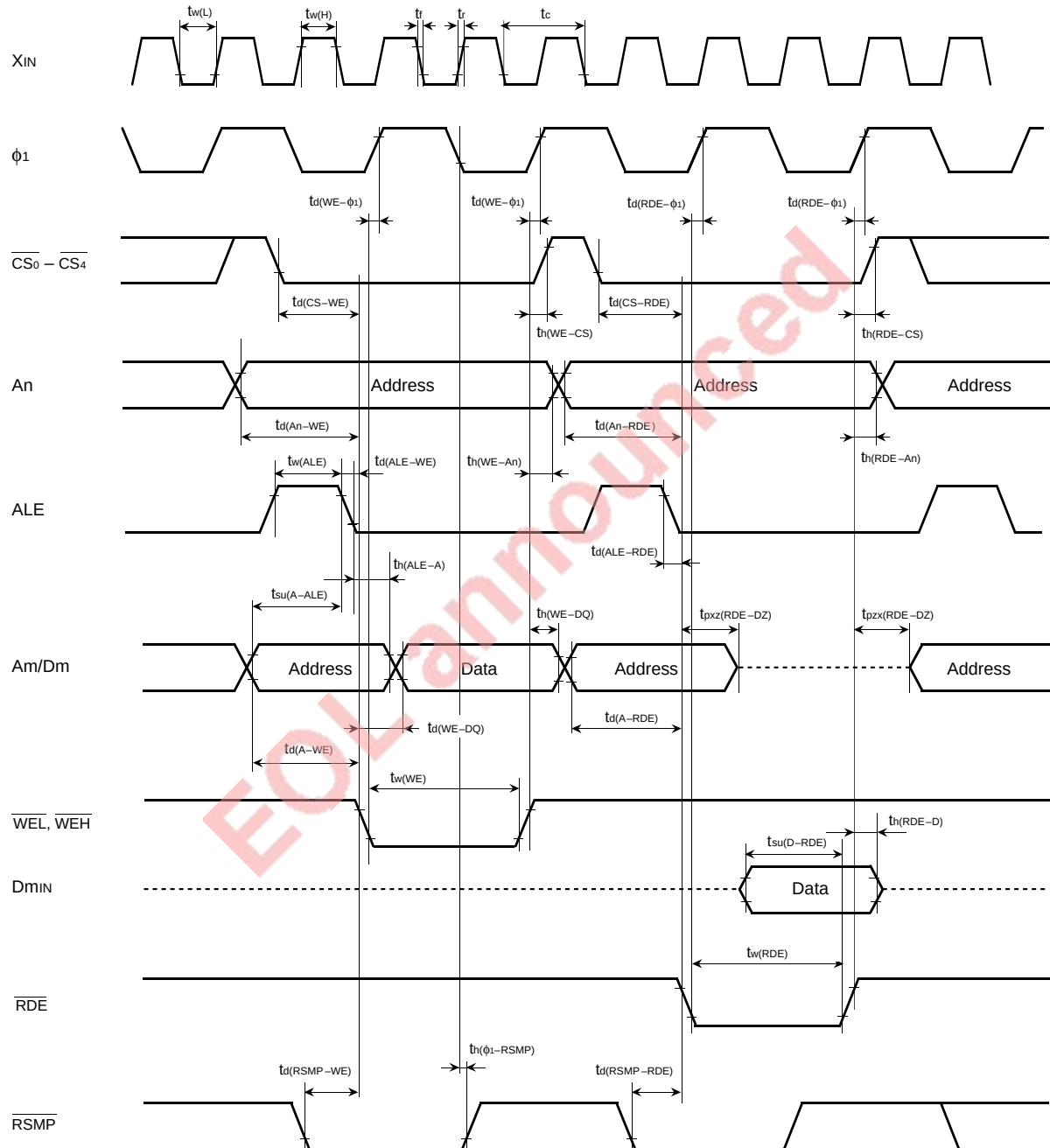
(When wait bit = "1" or "0" in common)



Test conditions

- $V_{CC} = 5 \text{ V} \pm 10\%$
- Input timing voltage : $V_{IL} = 1.0 \text{ V}$, $V_{IH} = 4.0 \text{ V}$
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$

Memory expansion mode and microprocessor mode
 (No wait : When wait bit = "1")

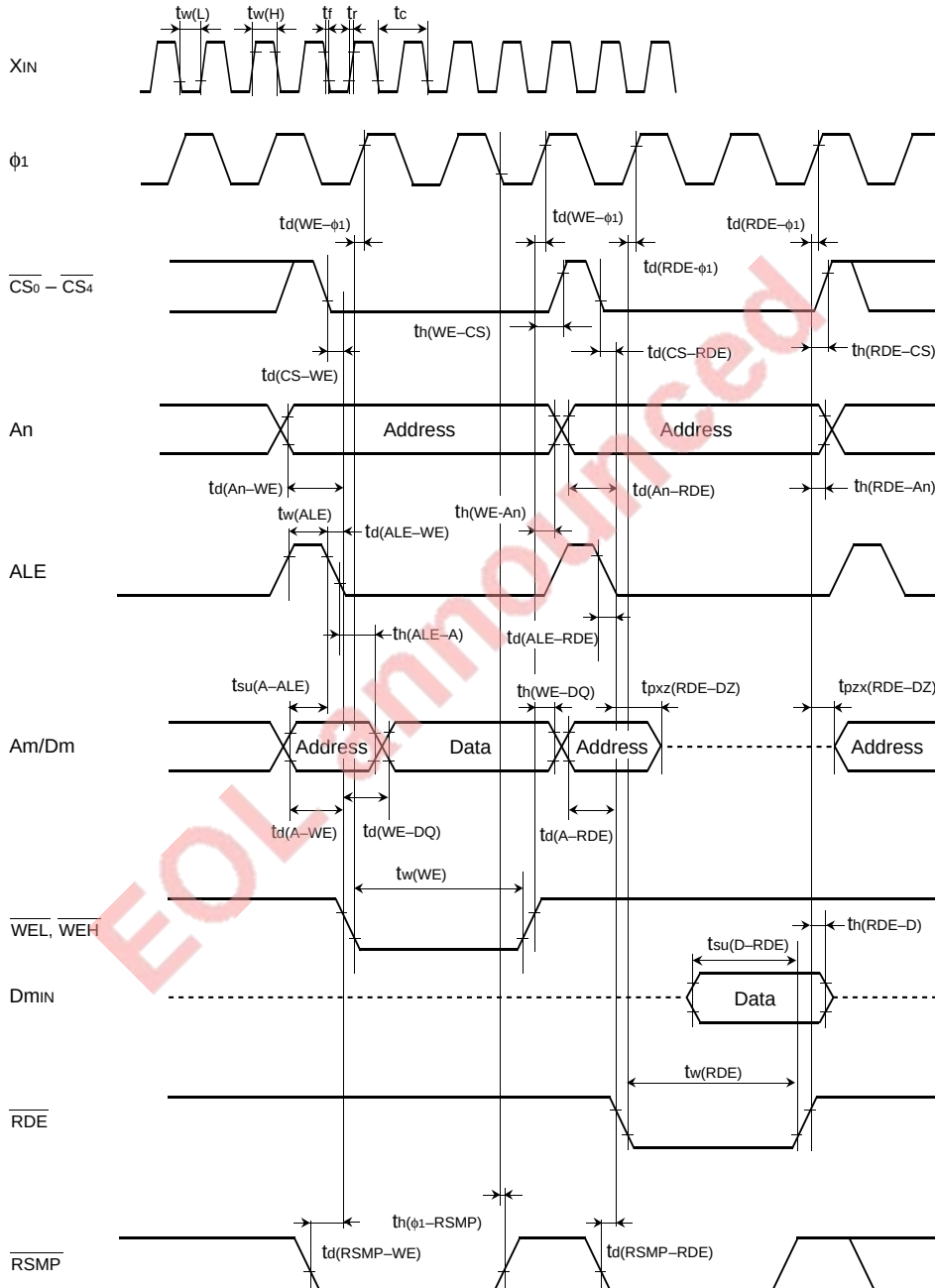


Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{MIN} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

Memory expansion mode and microprocessor mode

(Wait 1 : The external memory area is accessed when wait bit = "0" and wait selection bit = "1".)

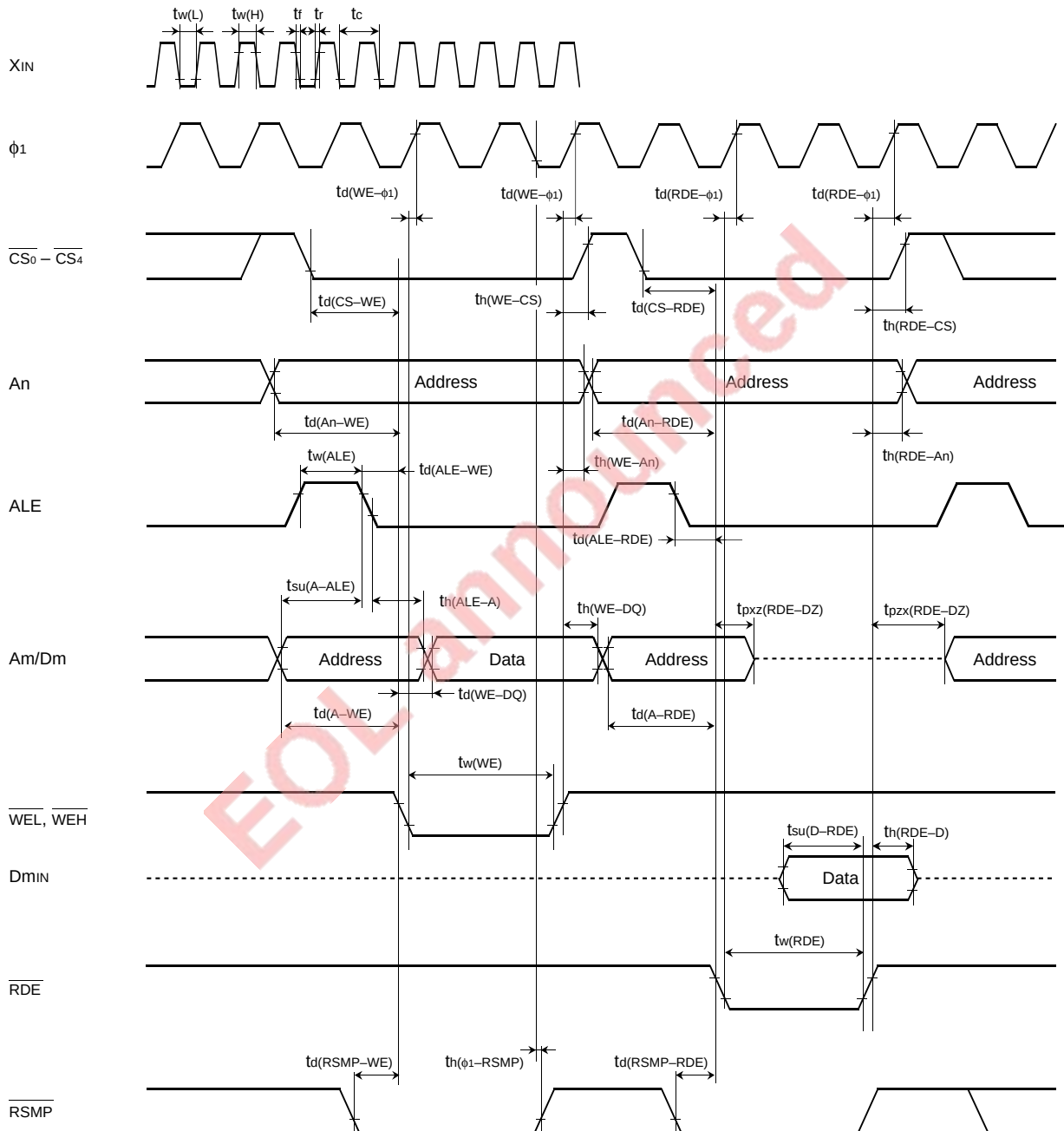


Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input Dmin : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

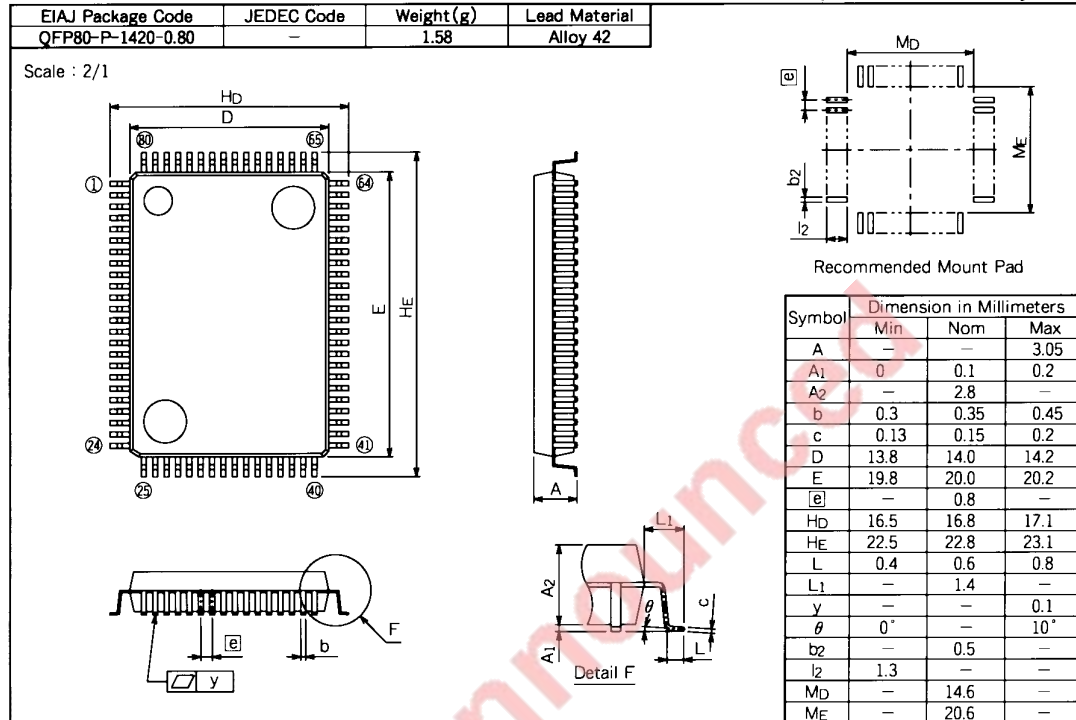
M37735EHBXXXFP
M37735EHBFS

PROM VERSION OF M37735MHBXXXFP

PACKAGE OUTLINE

80P6N-A

Plastic 80pin 14x20mm body QFP



7700 FAMILY WRITING TO PROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37735EHBXXXFP
MITSUBISHI ELECTRIC

ROM number	
------------	--

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ※

※	Customer	Company name	TEL ()	Issuance signatures	Responsible officer	Supervisor
		Date issued	Date:			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain the identical data, we will produce writing to PROM based on this data. We shall assume the responsibility for errors only if the written PROM data on the products we produce differ from this data.

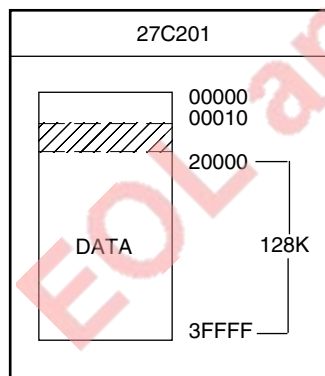
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas

--	--	--	--

 (hexadecimal notation)

EPROM Type :



Note : Make sure that address 01FFFF₁₆ of the microcomputer's internal ROM corresponds to address 3FFFF₁₆ of EPROM.

(1) Set "FF₁₆" in the shaded area.

(2) Address 0₁₆ to 0F₁₆ are the area for storing the data on model designation. This area must be written with the data shown below.

Address and data are written in hexadecimal notation.

Address		Address	
4D	0	42	8
33	1	FF	9
37	2	FF	A
37	3	FF	B
33	4	FF	C
35	5	FF	D
45	6	FF	E
48	7	FF	F

※2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6N Mark Specification Form (for M37735EHBXXXFP) and attach to the Writing to PROM Order Confirmation Form.

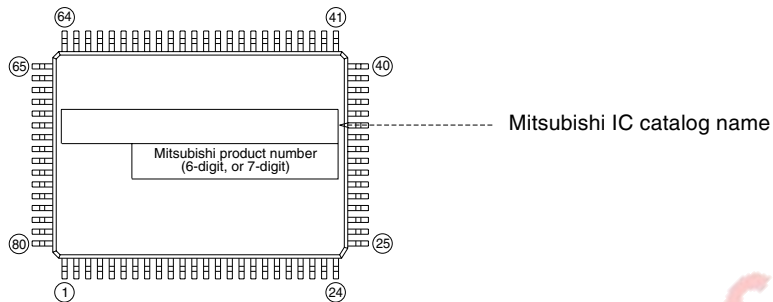
※3. Comments

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

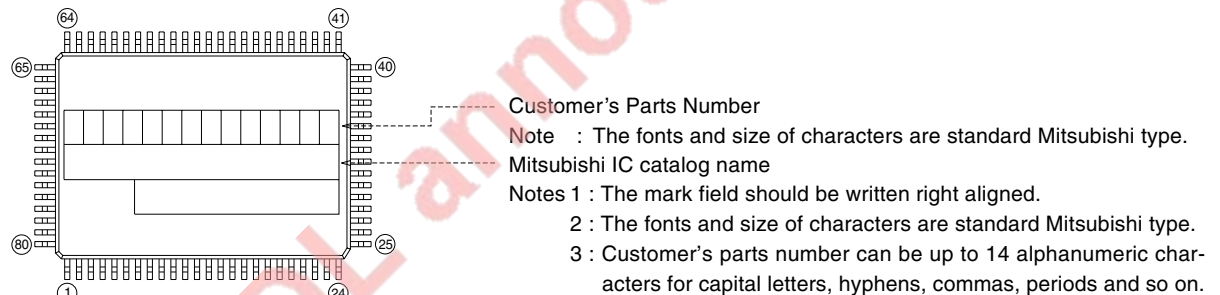
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

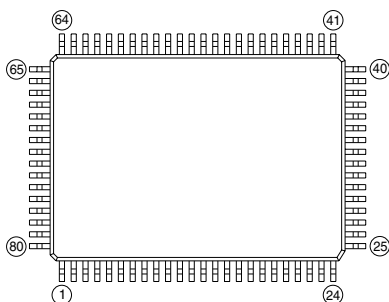
A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi IC Catalog Name



C. Special Mark Required



Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.

Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.

2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.

For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

☐

PRELIMINARY
Notice: This is not a final specification.
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MITSUBISHI MICROCOMPUTERS

M37735EHBXXXFP
M37735EHBFS

PROM VERSION OF M37735MHBXXXFP

EOL announced

Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

Keep safety first in your circuit designs!

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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REVISION DESCRIPTION LIST

M37735EBXXXXFP, M37735EBBFS Datasheet

Rev. No.	Revision Description		Rev. date
1.00	First Edition		970604
1.01	The following are added: • PROM ORDER CONFIRMATION FORM • MARK SPECIFICATION FORM		980526
2.00	The following are revised:		980731
	Page	Previous Version	
	P12 Right column Line 2	The M37735EBXXXXFP has 28 powerful addressing modes. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for the details of each addressing mode. MACHINE INSTRUCTION LIST The M37735EBXXXXFP has 103 machine instructions. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for details.	
		The M37735EBXXXXFP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details. MACHINE INSTRUCTION LIST The M37735EBXXXXFP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.	