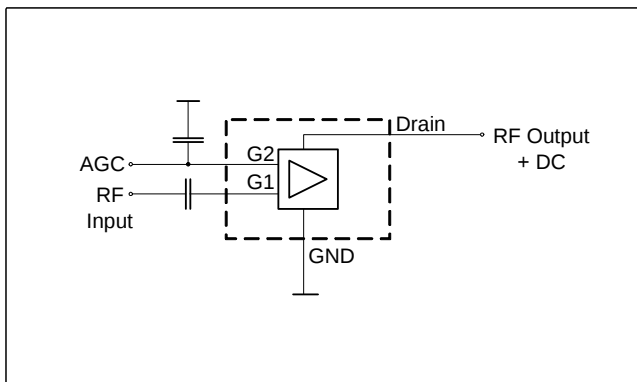
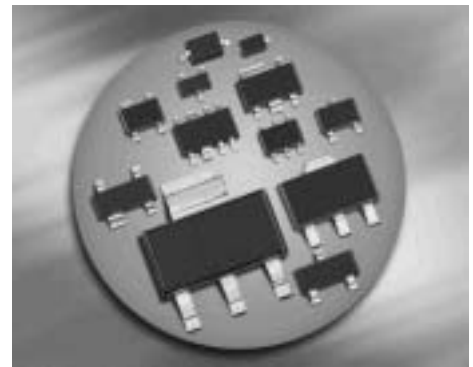


## Silicon N-Channel MOSFET Tetrode

- For low noise, high gain controlled input stage up to 1 GHz
- Operating voltage 9 V
- Integrated biasing network
- Pb-free (RoHS compliant) package<sup>1)</sup>
- Qualified according AEC Q101



**ESD (Electrostatic discharge) sensitive device, observe handling precaution!**

| Type     | Package | Pin Configuration |     |      |      |   |   | Marking |
|----------|---------|-------------------|-----|------|------|---|---|---------|
| BF1009S  | SOT143  | 1=S               | 2=D | 3=G2 | 4=G1 | - | - | JLs     |
| BF1009SR | SOT143R | 1=D               | 2=S | 3=G1 | 4=G2 | - | - | JLs     |

### Maximum Ratings

| Parameter                                                                  | Symbol           | Value       | Unit             |
|----------------------------------------------------------------------------|------------------|-------------|------------------|
| Drain-source voltage                                                       | $V_{DS}$         | 12          | V                |
| Continuous drain current                                                   | $I_D$            | 25          | mA               |
| Gate 1/ gate 2-source current                                              | $\pm I_{G1/2SM}$ | 10          |                  |
| Gate 1 (external biasing)                                                  | $+V_{G1SE}$      | 3           | V                |
| Total power dissipation<br>$T_S \leq 76^\circ\text{C}$ , BF1009S, BF1009SR | $P_{tot}$        | 200         | mW               |
| Storage temperature                                                        | $T_{stg}$        | -55 ... 150 | $^\circ\text{C}$ |
| Channel temperature                                                        | $T_{ch}$         | 150         |                  |

<sup>1)</sup>Pb-containing package may be available upon special request

### Note:

**It is not recommended to apply external DC-voltage on Gate 1 in active mode.**

**Thermal Resistance**

| Parameter                                                    | Symbol      | Value      | Unit |
|--------------------------------------------------------------|-------------|------------|------|
| Channel - soldering point <sup>1)</sup><br>BF1009S, BF1009SR | $R_{thchs}$ | $\leq 370$ | K/W  |

**Electrical Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

| Parameter                                                                                        | Symbol             | Values |      |      | Unit          |
|--------------------------------------------------------------------------------------------------|--------------------|--------|------|------|---------------|
|                                                                                                  |                    | min.   | typ. | max. |               |
| DC Characteristics                                                                               |                    |        |      |      |               |
| Drain-source breakdown voltage<br>$I_D = 500\text{ }\mu\text{A}$ , $V_{G1S} = 0$ , $V_{G2S} = 0$ | $V_{(BR)DS}$       | 12     | -    | -    | V             |
| Gate1-source breakdown voltage<br>$+I_{G1S} = 10\text{ mA}$ , $V_{G2S} = 0$ , $V_{DS} = 0$       | $+V_{(BR)G1SS}$    | 9      | -    | 12   |               |
| Gate2 source breakdown voltage<br>$\pm I_{G2S} = 10\text{ mA}$ , $V_{G1S} = 0$ , $V_{DS} = 0$    | $\pm V_{(BR)G2SS}$ | 9      | -    | 12   |               |
| Gate1-source leakage current<br>$V_{G1S} = 6\text{ V}$ , $V_{G2S} = 0$                           | $+I_{G1SS}$        | -      | -    | 60   | $\mu\text{A}$ |
| Gate 2 source leakage current<br>$\pm V_{G2S} = 8\text{ V}$ , $V_{G1S} = 0$ , $V_{DS} = 0$       | $\pm I_{G2SS}$     | -      | -    | 50   | nA            |
| Drain current<br>$V_{DS} = 9\text{ V}$ , $V_{G1S} = 0$ , $V_{G2S} = 6\text{ V}$                  | $I_{DSS}$          | -      | -    | 500  | $\mu\text{A}$ |
| Operating current (selfbiased)<br>$V_{DS} = 9\text{ V}$ , $V_{G2S} = 6\text{ V}$                 | $I_{DSO}$          | 10     | 13   | 16   | mA            |
| Gate2-source pinch-off voltage<br>$V_{DS} = 9\text{ V}$ , $I_D = 500\text{ }\mu\text{A}$         | $V_{G2S(p)}$       | -      | 0.9  | -    | V             |

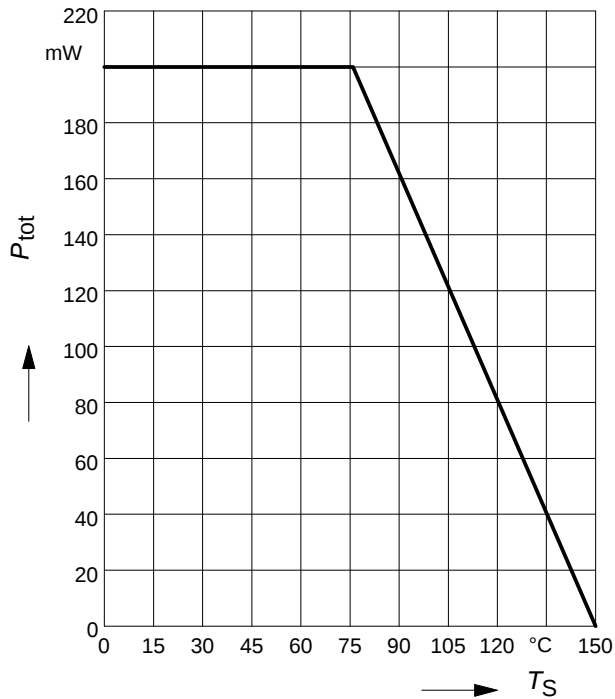
<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

**Electrical Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

| Parameter                                                                                     | Symbol       | Values |      |      | Unit |
|-----------------------------------------------------------------------------------------------|--------------|--------|------|------|------|
|                                                                                               |              | min.   | typ. | max. |      |
| AC Characteristics (verified by random sampling)                                              |              |        |      |      |      |
| Forward transconductance<br>$V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}$                       | $g_{fs}$     | 26     | 30   | -    | mS   |
| Gate1 input capacitance<br>$V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 10\text{ MHz}$     | $C_{g1ss}$   | -      | 2.1  | 2.7  | pF   |
| Output capacitance<br>$V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 10\text{ MHz}$          | $C_{dss}$    | -      | 0.9  | -    |      |
| Power gain (self biased)<br>$V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 800\text{ MHz}$   | $G_p$        | 18     | 22   | -    | dB   |
| Noise figure<br>$V_{DS} = 9\text{ V}, V_{G2S} = 6\text{ V}, f = 800\text{ MHz}$               | $F$          | -      | 1.4  | 2.1  | dB   |
| Gain control range<br>$V_{DS} = 9\text{ V}, V_{G2S} = 6 \dots 0\text{ V}, f = 800\text{ MHz}$ | $\Delta G_p$ | 40     | 50   | -    |      |

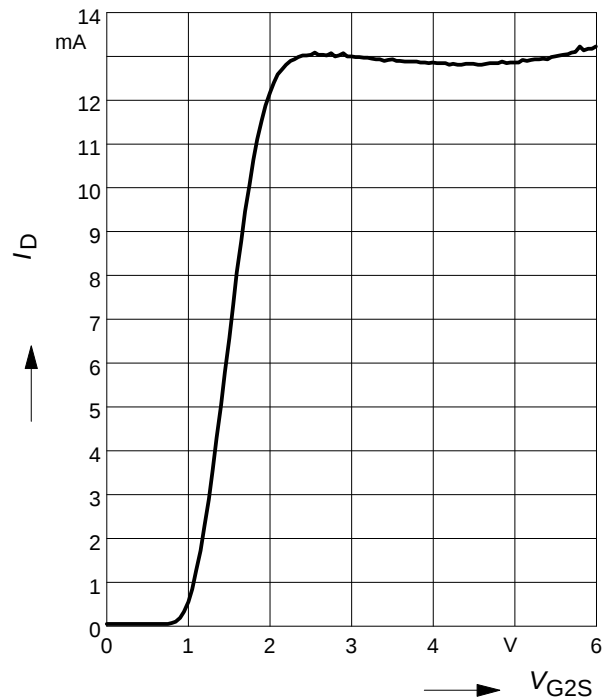
**Total power dissipation**  $P_{\text{tot}} = f(T_S)$

BF1009S, BF1009SR



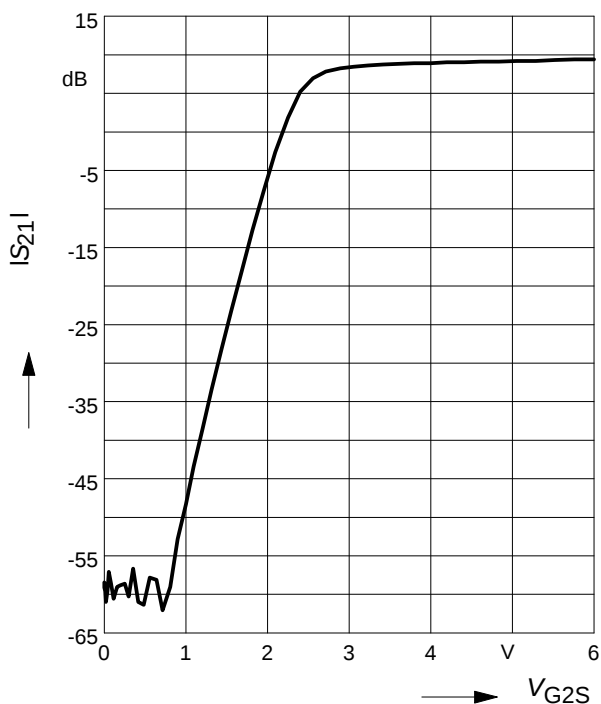
**Drain current**  $I_D = f(V_{G2S})$

$V_{DS} = 9 \text{ V}$



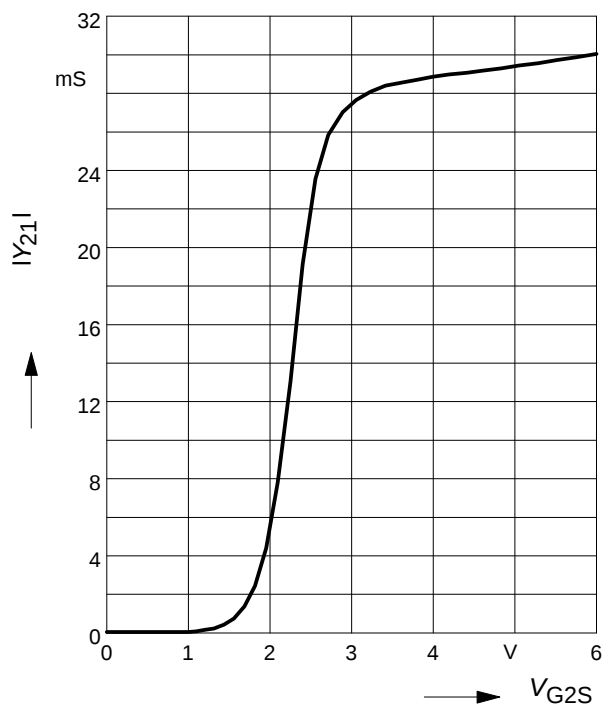
**Insertion power gain**

$|S_{21}|^2 = f(V_{G2S}), f = 200 \text{ MHz}$



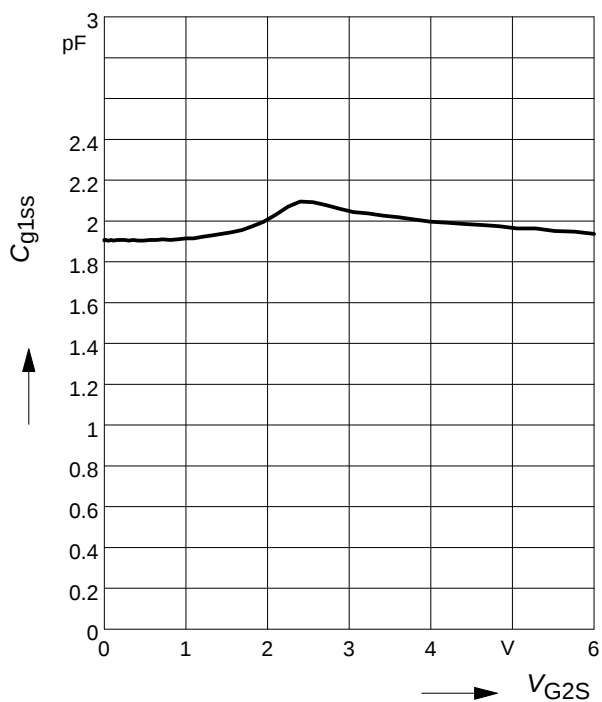
**Forward transfer admittance**

$|Y_{21}| = f(V_{G2S}), f = 200 \text{ MHz}$



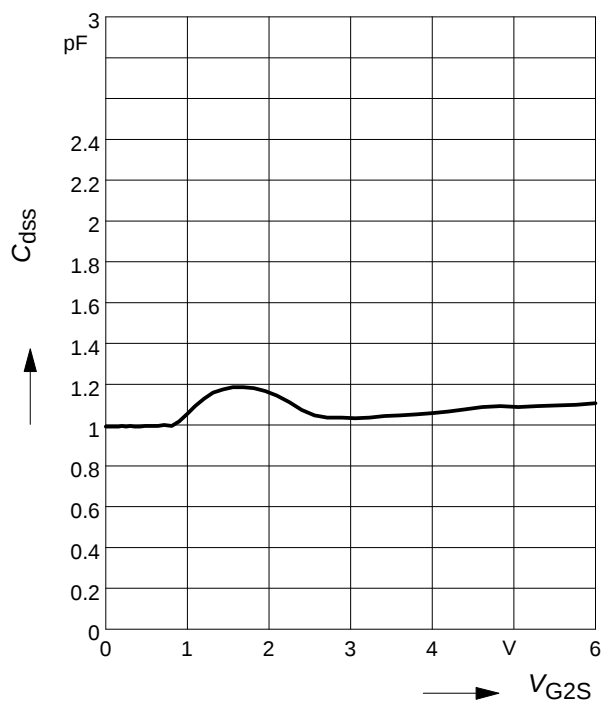
**Gate 1 input capacitance  $C_{g1ss} = f(V_{G2S})$**

$f = 200 \text{ MHz}$

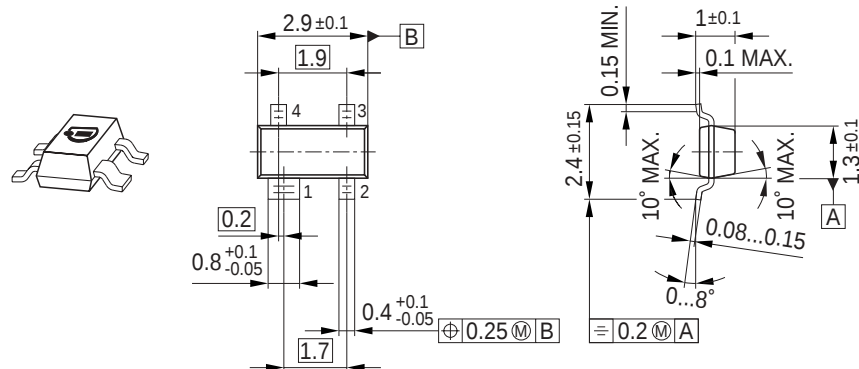


**Output capacitance  $C_{dss} = f(V_{G2S})$**

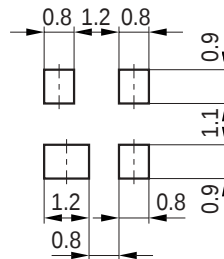
$f = 200 \text{ MHz}$



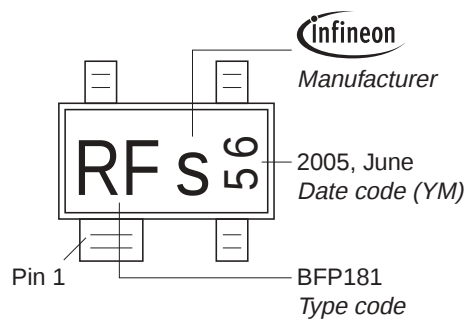
## Package Outline



## Foot Print

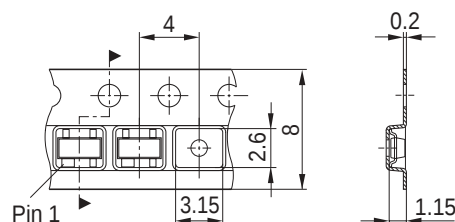


## Marking Layout (Example)

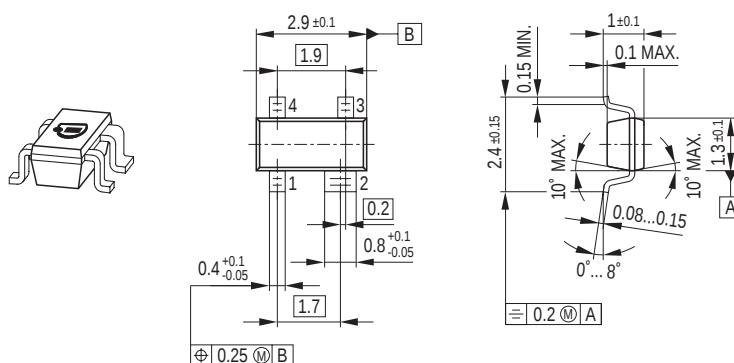


## Standard Packing

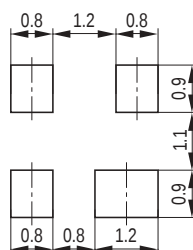
Reel ø180 mm = 3.000 Pieces/Reel  
Reel ø330 mm = 10.000 Pieces/Reel



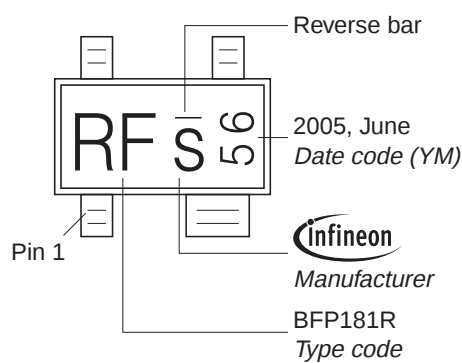
## Package Outline



## Foot Print

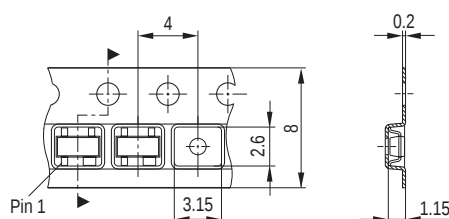


## Marking Layout (Example)



## Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel  
Reel ø330 mm = 10.000 Pieces/Reel



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