
Description

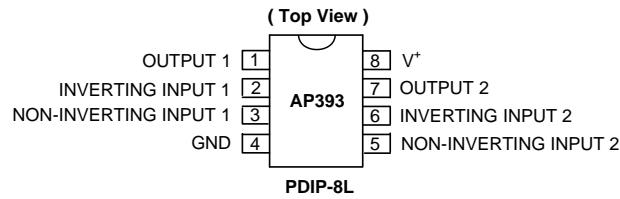
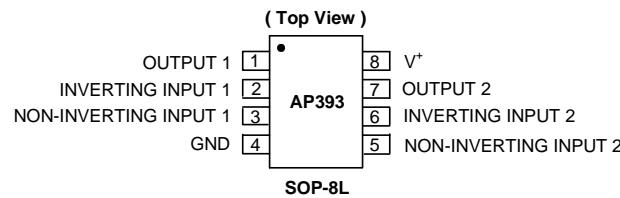
The AP393 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The AP393 is designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AP393 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Features

- Wide supply
 - Voltage range: 2.0V to 36V
 - Single or dual supplies: $\pm 1.0V$ to $\pm 18V$
- Very low supply current drain (0.4mA) – independent of supply voltage
- Low input biasing current: 25nA
- Low input offset current: $\pm 5nA$
- Maximum offset voltage: $\pm 3mV$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250mV at 4mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Lead Free packages: SOP-8L and PDIP-8L
- SOP-8L and PDIP-8L: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)

Pin Assignments

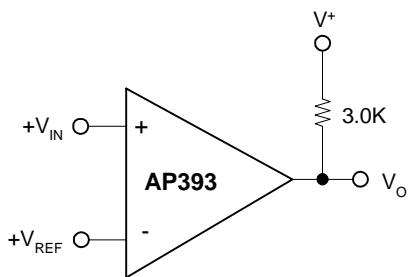


Application

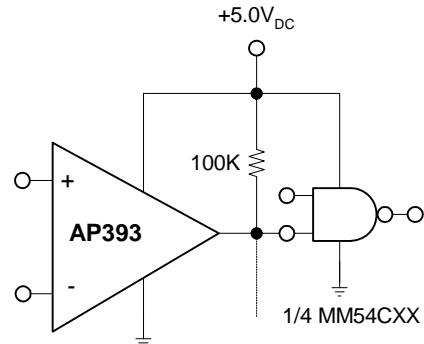
- High precision comparators
- Reduced VOS drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

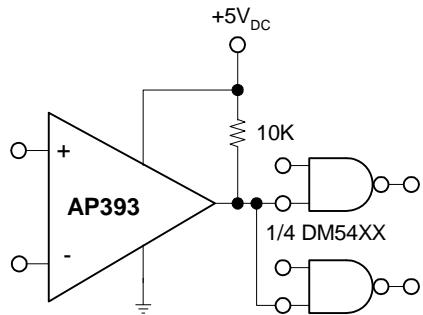
Typical Circuit ($V_{CC}=5.0V_{DC}$)



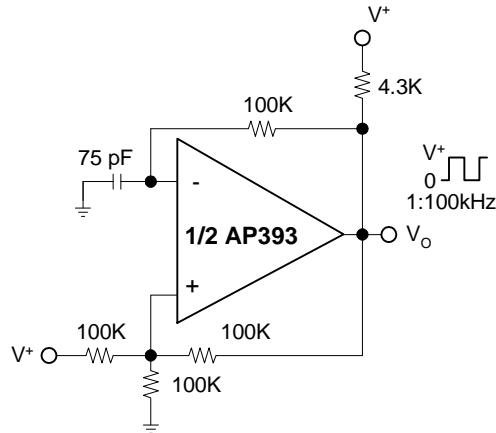
Basic Comparator



Driving CMOS

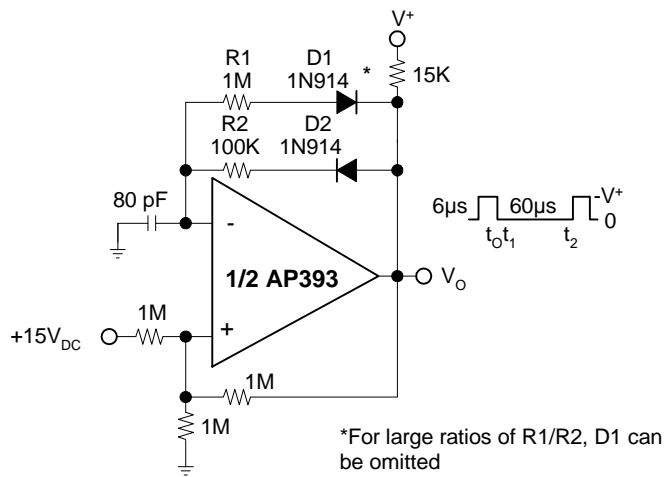


Driving TTL



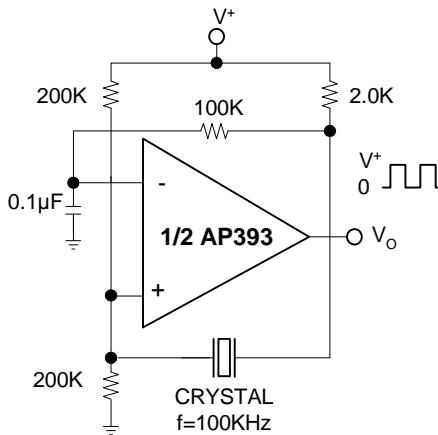
Squarewave Oscillator

Typical Circuit (Continued) (V_{CC}=5.0V_{DC})

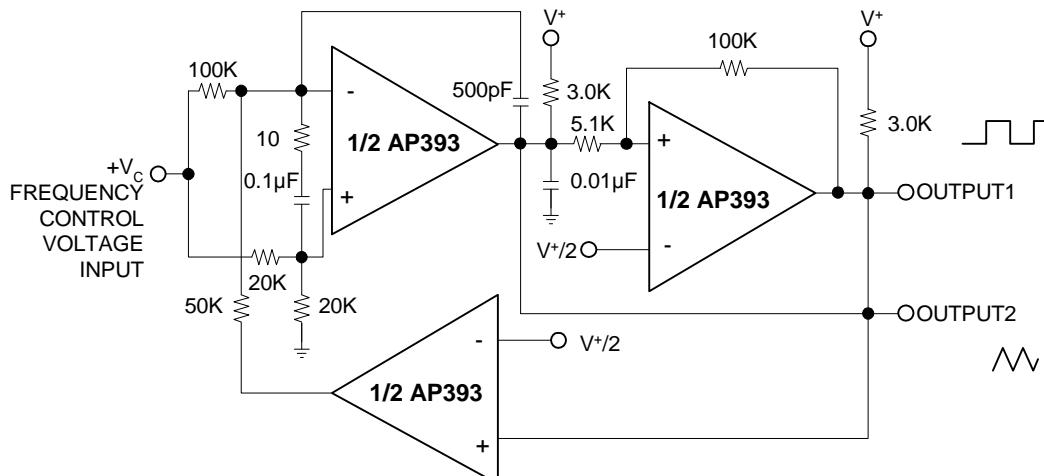


Pulse Generator

*For large ratios of R1/R2, D1 can be omitted

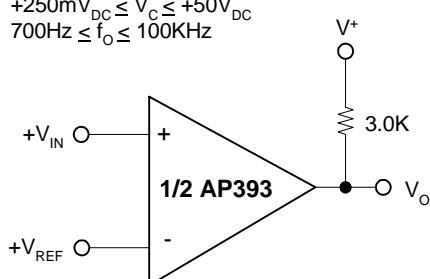


Crystal Controlled Oscillator

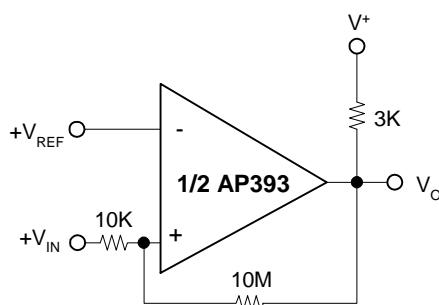


Two-Decade High Frequency VCO

$$\begin{aligned}V^* &= +30V_{DC} \\+250mV_{DC} &\leq V_C \leq +50V_{DC} \\700Hz &\leq f_O \leq 100KHz\end{aligned}$$

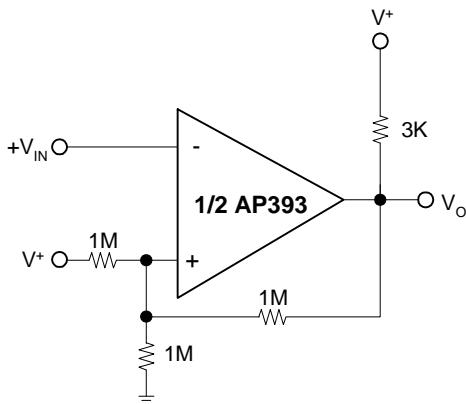


Basic Comparator

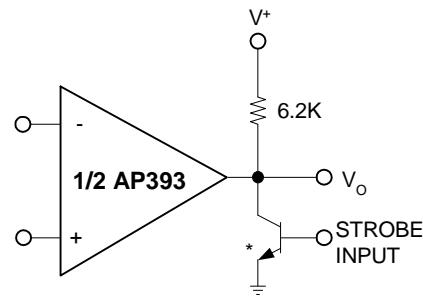


Non-Inverting Comparator with Hysteresis

Typical Circuit (Continued) (V_{CC}=5.0V_{DC})

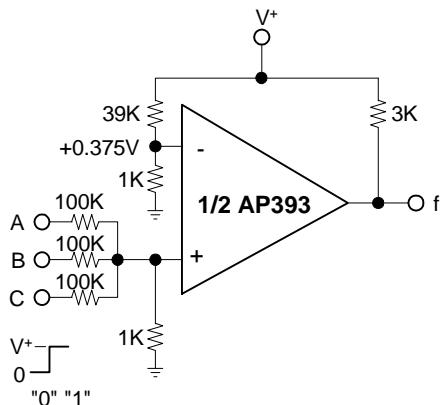


Inverting Comparator with Hysteresis

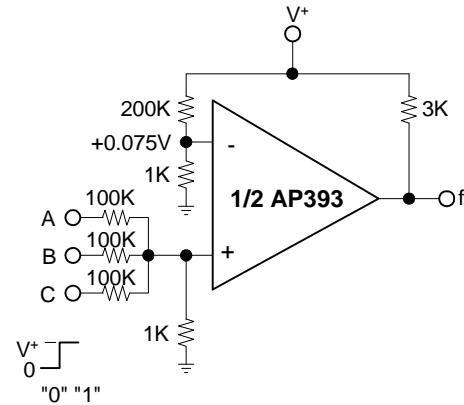


* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

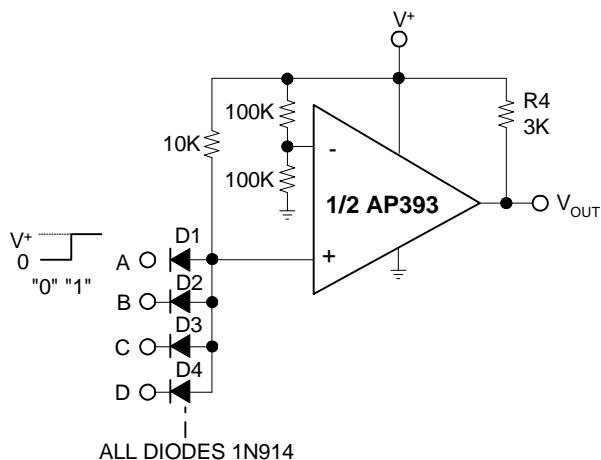
Output Strobing



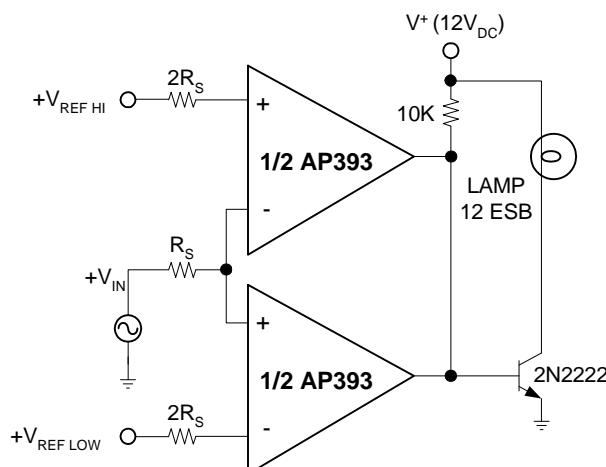
AND Gate



Or Gate

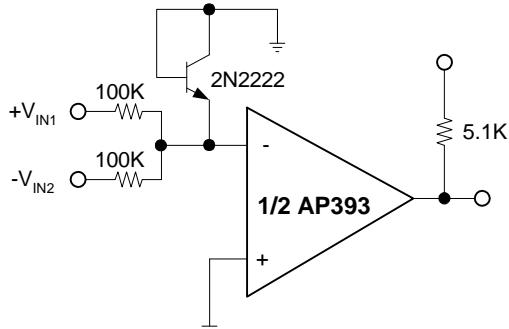


Large Fan-in AND Gate

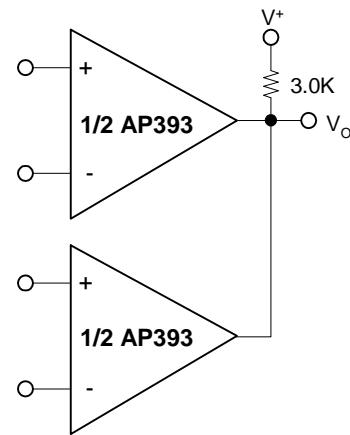


Limit Comparator

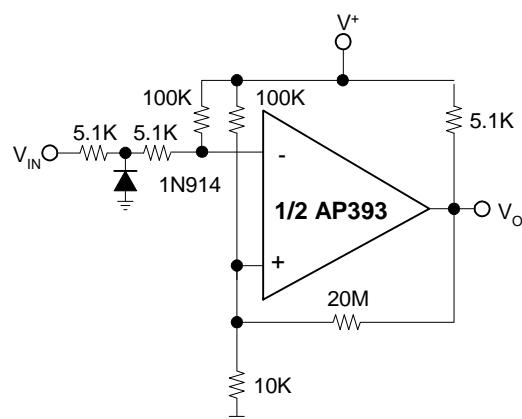
Typical Circuit (Continued) (V_{CC}=5.0V_{DC})



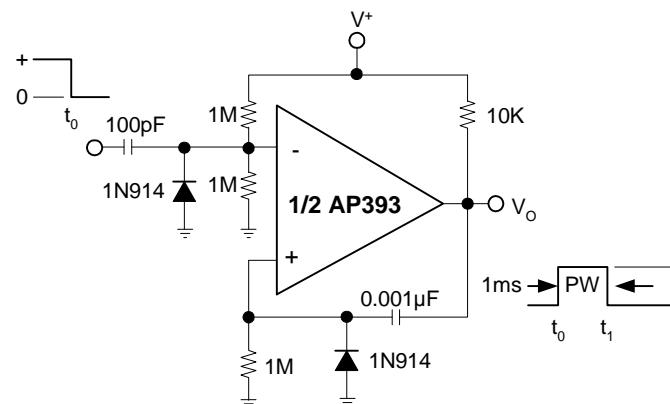
**Comparing Input Voltages of
Opposite Polarity**



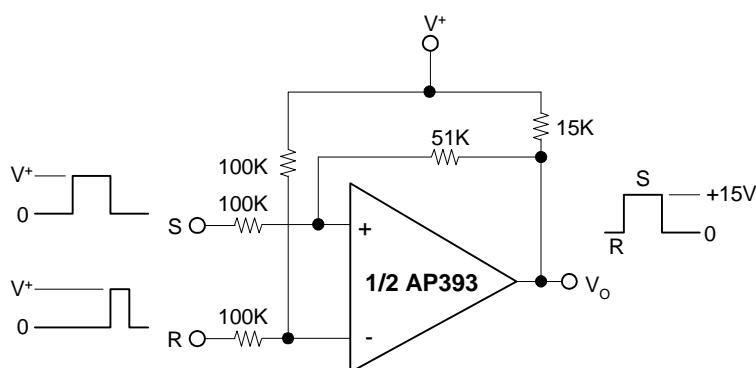
ORing the Outputs



**Zero Crossing Detector
(Single Power Supply)**

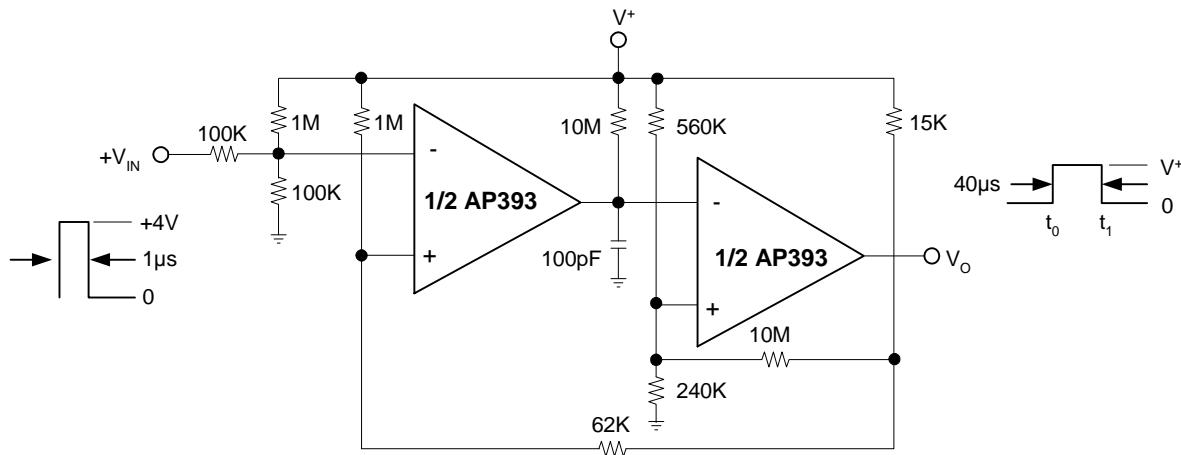


One-Shot Multivibrator

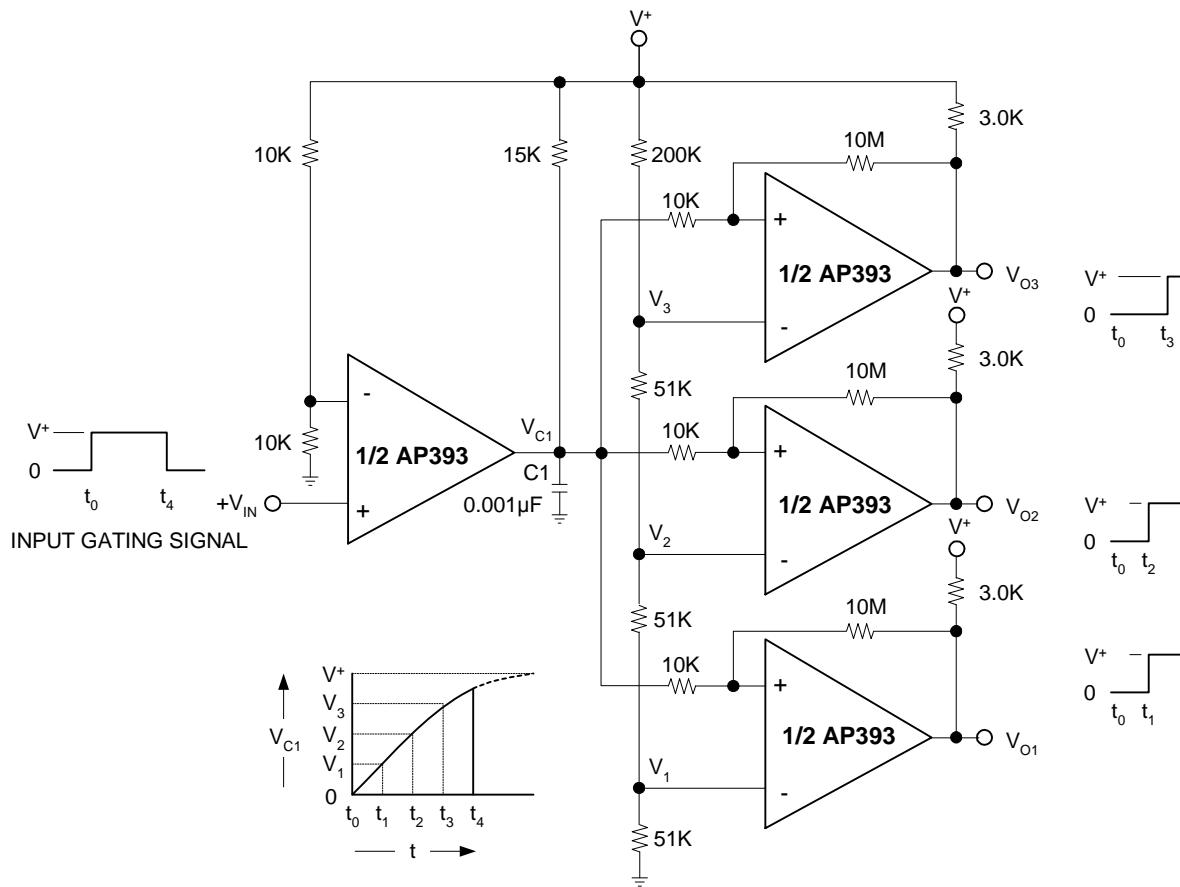


Bi-Stable Multivibrator

Typical Circuit (Continued) (V_{CC}=5.0V_{DC})

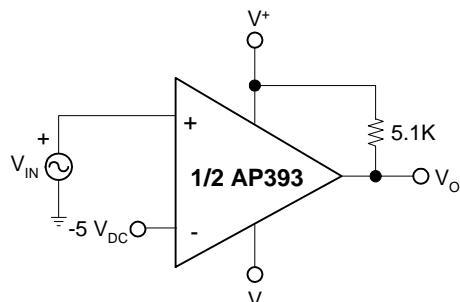
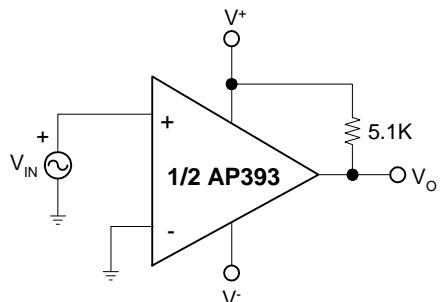
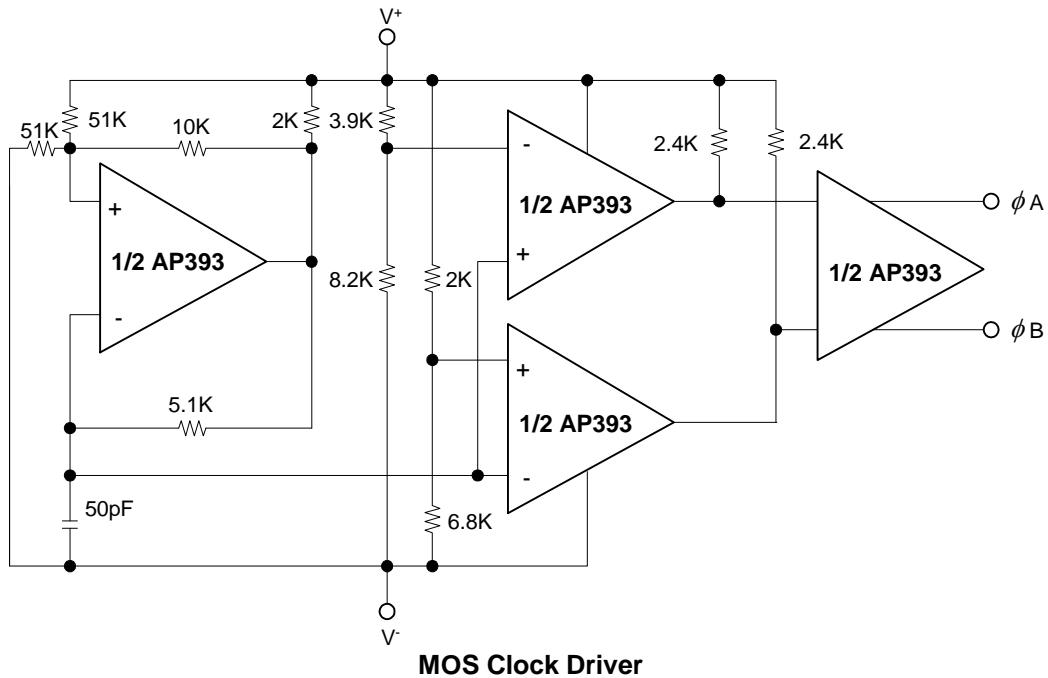


One-Shot Multivibrator with Input Lock Out

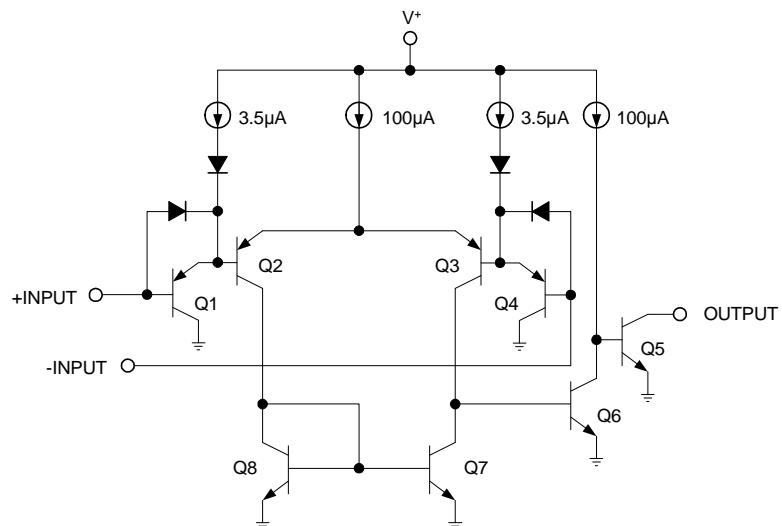
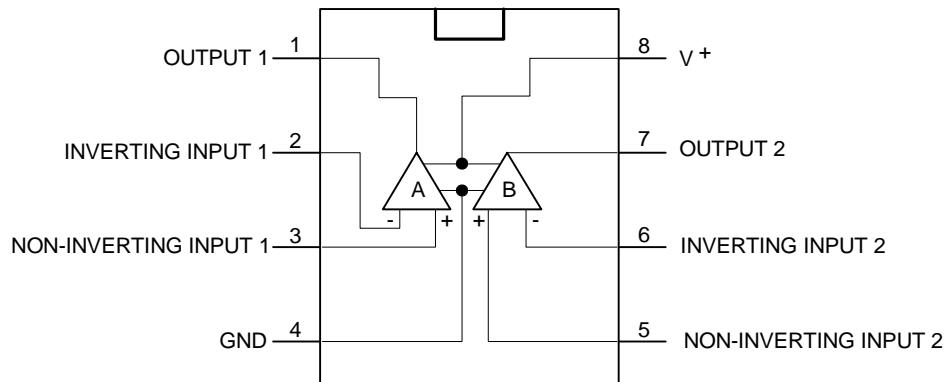


Time Delay Generator

Split-Supply Applications ($V^+ = +15V_{DC}$ and $V^- = -15V_{DC}$)



Functional Block Diagram



Pin Descriptions

| Pin Name | Pin # | Description |
|-----------------------|-------|--------------------------|
| OUTPUT 1 | 1 | Channel 1 Output |
| INVERTING INPUT 1 | 2 | Channel 1 Negative Input |
| NON-INVERTING INPUT 1 | 3 | Channel 1 Positive Input |
| GND | 4 | Ground |
| NON-INVERTING INPUT 2 | 5 | Channel 2 Positive Input |
| INVERTING INPUT 2 | 6 | Channel 2 Negative Input |
| OUTPUT 2 | 7 | Channel 2 Output |
| V ⁺ | 8 | V _{CC} |

Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|----------|--|-------------|------|
| V_{CC} | Supply Voltage | 36 | V |
| V_{IN} | Differential Input Voltage (Note 9) | 36 | V |
| V_{IN} | Input Voltage | -0.3 to +36 | V |
| I_{CC} | Input Current (V_{IN} -0.3V) (Note 4) | 50 | mA |
| P_D | Power Dissipation (Note 2) | 780 | mW |
| | | 510 | |
| | Output Short-Circuit to Ground (Note 3) | Continuous | |
| T_{OP} | Operating Junction Temperature Range | 0 to +70 | °C |
| T_{ST} | Storage Temperature Range | -65 to +150 | °C |

Electrical Characteristics ($V_{CC} = 5V$, $T_A = 25^\circ C$, unless otherwise stated)

| Symbol | Parameter | Conditions | | Min | Typ. | Max | Unit |
|---------------|---------------------------------|---|---------------------------|-----|------|-------------|------|
| V_{OFFSET} | Input Offset Voltage | (Note 10) | | - | 1.0 | 5.0 | mV |
| I_{BIAS} | Input Bias Current | $I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, $V_{CM} = 0V$ (Note 6) | | - | 25 | 250 | nA |
| I_{OFFSET} | Input Offset Current | $I_{IN}(+) - I_{IN}(-)$ $V_{CM} = 0V$ | | - | 5.0 | 50 | nA |
| | Input Common Mode Voltage Range | $V^+ = 30V$ (Note 7) | | 0 | - | $V^+ - 1.5$ | V |
| I_{CC} | Supply Current | $R_L = \infty$ | $V^+ = 5V$ $V^+ = 36V$ | - | 0.4 | 1 | mA |
| | Voltage Gain | $R_L \geq 15k\Omega$, $V^+ = 15V$ $V_O = 1V$ to $11V$ | | 50 | 200 | - | |
| | Large Signal Response Time | $V_{IN} = TTL$ Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1k\Omega$ | | - | 300 | - | ns |
| | Response Time | $V_{RL} = 5V$, $R_L = 5.1k\Omega$ (Note 8) | | - | 1.3 | - | μs |
| $I_{O(Sink)}$ | Output Sink Current | $V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$ | | 6.0 | 16 | - | mA |
| V_{SAT} | Saturation Voltage | $V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$ | | - | 250 | 400 | mV |
| $I_{O(Leak)}$ | Output Leakage Current | $V_{IN}(-) = 0$, $V_{IN}(+) = 1V$, $V_O = 5V$ | | - | 0.1 | - | nA |

Electrical Characteristics (Continued)
 $(V_{CC} = 5V)$ (Note 5)

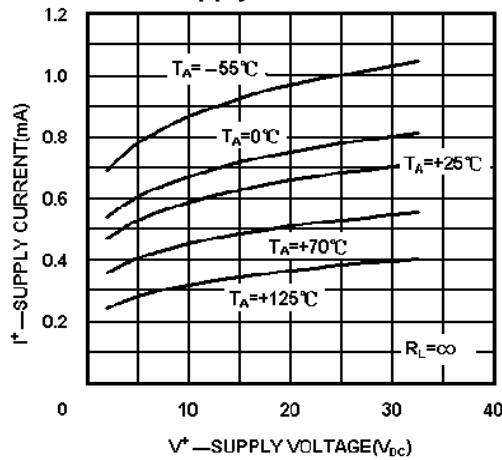
| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|---------------|---------------------------------|---|-----|------|-------------|---------|
| V_{OFFSET} | Input Offset Voltage | (Note 10) | - | - | 9 | mV |
| I_{OFFSET} | Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | - | - | 150 | nA |
| I_{BIAS} | Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$ with Output In Linear Range, $V_{CM} = 0V$ (Note 6) | - | - | 400 | nA |
| | Input Common Mode Voltage Range | $V^+ = 30V$ (Note 7) | 0 | - | $V^+ - 2.0$ | V |
| V_{SAT} | Saturation Voltage | $V_{IN(-)} = 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ | - | - | 700 | mV |
| $I_{O(Leak)}$ | Output Leakage Current | $V_{IN(-)} = 0$, $V_{IN(+)} = 1V$, $V_O = 30V$ | - | - | 1.0 | μA |
| | Differential Input Voltage | Keep All V_{IN} 's $\geq 0V$ (or V^- , if Used), (Note 9) | - | - | 36 | V |

Notes:

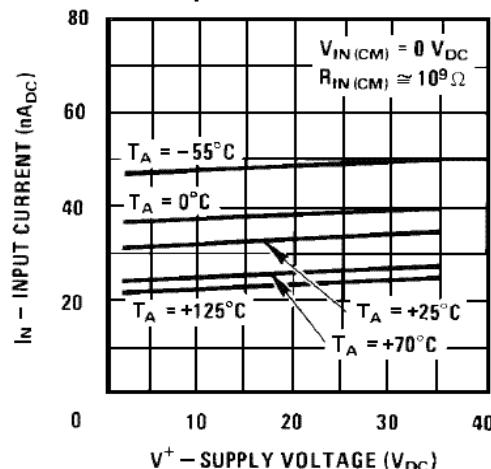
2. For operating at high temperatures, the AP393 must be derated based on a $125^{\circ}C$ maximum junction temperature and a thermal resistance of $170^{\circ}C/W$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small, ($P_D \leq 100mW$), provided the output transistors are allowed to saturate
3. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately $20mA$ independent of the magnitude of V^+ .
4. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than $-0.3V$.
5. The AP393 temperature specifications are limited to $0^{\circ}C \leq T_{OP} \leq +70^{\circ}C$.
6. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
7. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than $0.3V$. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at $25^{\circ}C$, but either or both inputs can go to $36V$ without damage, independent of the magnitude of V^+ .
8. The response time specified is for a $100mV$ input step with $5mV$ overdrive. For larger overdrive signals $300ns$ can be obtained, see typical performance characteristics section.
9. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$ (or $0.3V$ below the magnitude of the negative power supply, if used).
10. At output switch point, $V_O \geq 1.4V$, $R_S = 0\Omega$ with V^+ from $5V$ to $30V$; and over the full input common-mode range ($0V$ to $V^+ - 1.5V$), at $25^{\circ}C$.

Typical Performance Characteristics

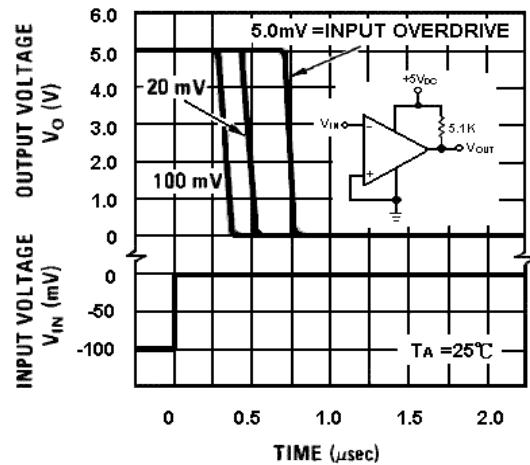
Supply Current



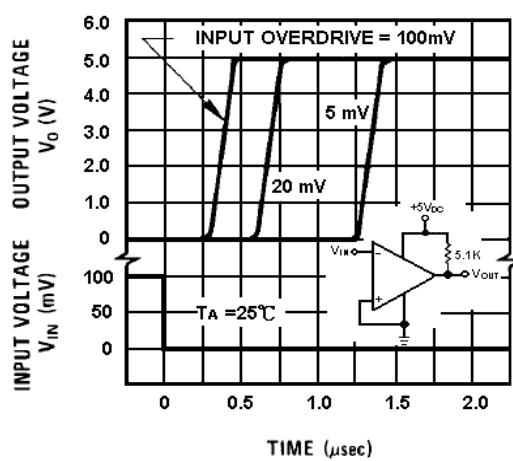
Input Current



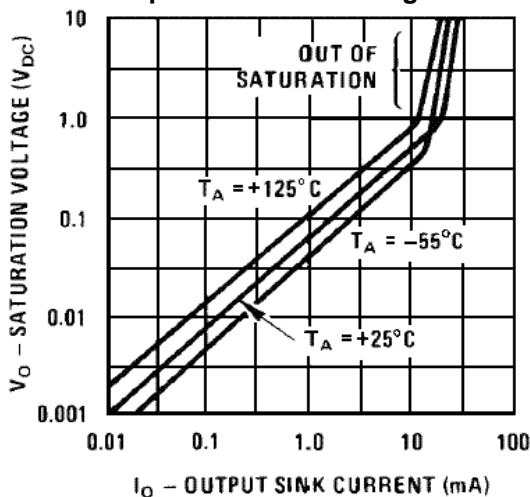
**Response Time for Various Input Overdrives—
Negative Transition**



**Response Time for Various Input Overdrives—
Positive Transition**



Output Saturation Voltage



Application Information

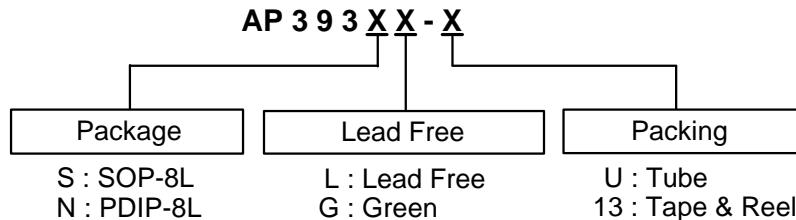
The AP393 is high gain, wide bandwidth devices, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required. All input pins of any unused comparators should be tied to the negative supply.

The bias network of the AP393 establishes a drain current independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}. It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V₊ without damaging the device (Note 11). Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the AP393 is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage applied to the V₊ terminal of the AP393 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current the output device can sink is limited by the drive available (which is independent of V₊) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Ordering Information

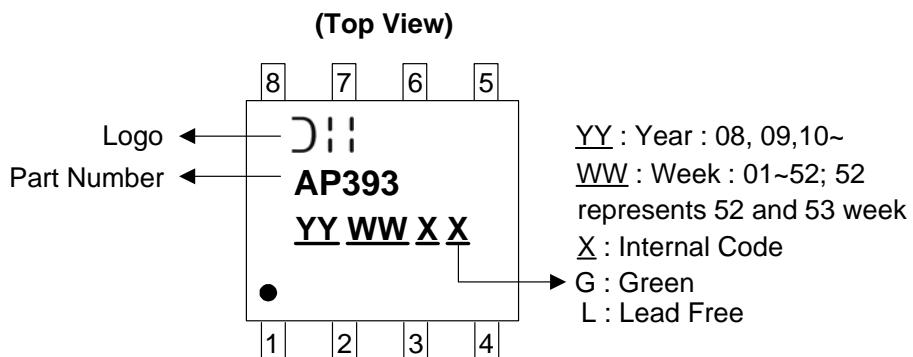


| Device | Package Code | Packaging (Note 11) | Tube | | 13" Tape and Reel | |
|------------|--------------|---------------------|----------|--------------------|-------------------|--------------------|
| | | | Quantity | Part Number Suffix | Quantity | Part Number Suffix |
| AP393SL-13 | S | SOP-8L | NA | NA | 2500/Tape & Reel | -13 |
| AP393SG-13 | S | SOP-8L | NA | NA | 2500/Tape & Reel | -13 |
| AP393NL-U | N | PDIP-8L | 60 | -U | NA | NA |
| AP393NG-U | N | PDIP-8L | 60 | -U | NA | NA |

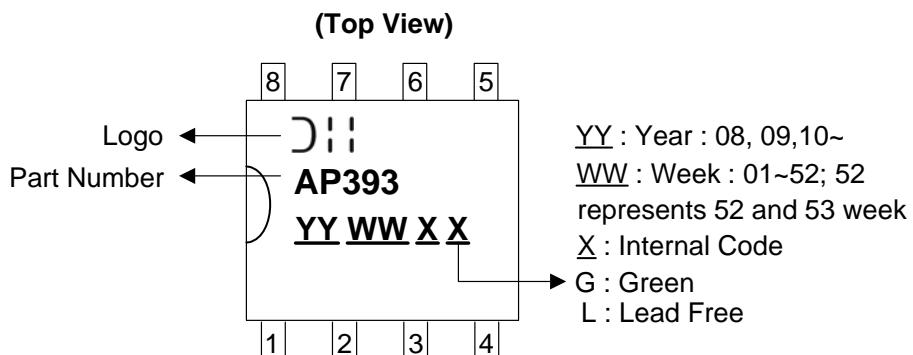
Notes: 11. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Marking Information

(1) SOP-8L

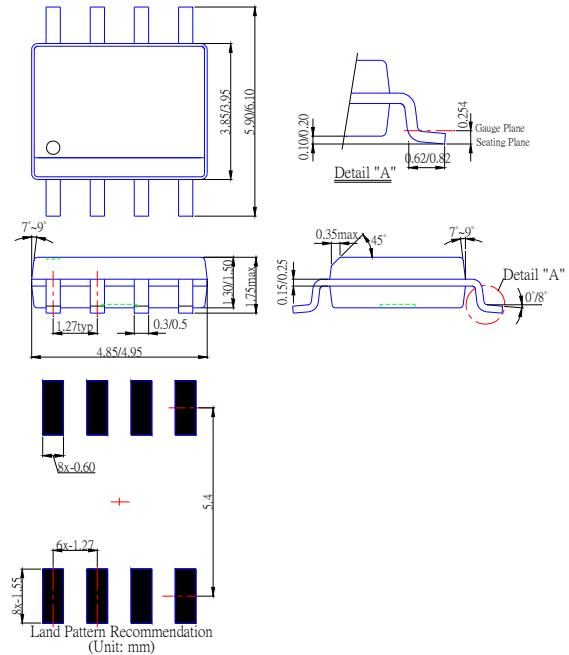


(2) PDIP-8L

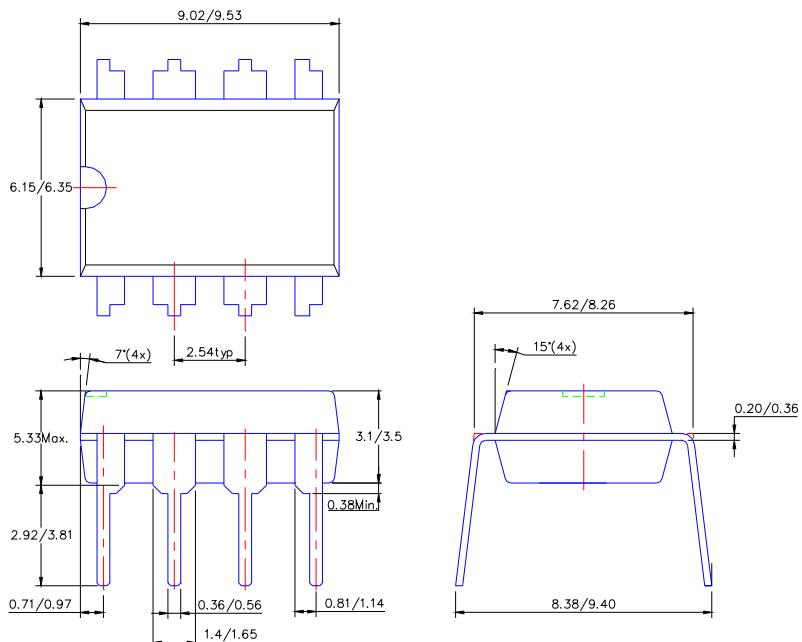


Package Outline Dimensions (All Dimensions in mm)

(1) Package type: SOP- 8L



(2) Package type: PDIP- 8L



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