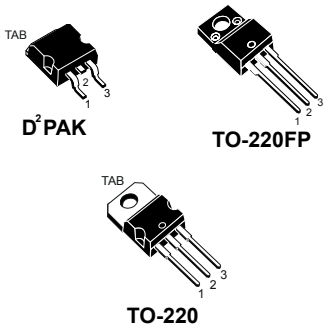
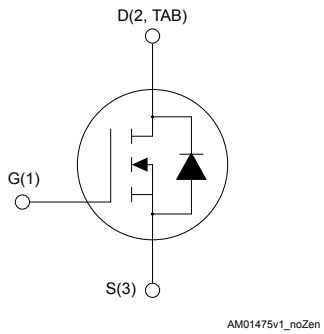
STB23NM50N, STF23NM50N, STP23NM50N

Datasheet

N-channel 500 V, 162 mΩ typ., 17 A MDmesh II Power MOSFET in a D²PAK, TO-220FP and TO-220 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB23NM50N	500 V	190 mΩ	17 A
STF23NM50N			
STP23NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

Product status links
STB23NM50N
STF23NM50N
STP23NM50N

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK Unit TO-220	TO-220FP	
V_{DS}	Drain-source voltage	500		V
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	17		A
I_D	Drain current (continuous) at T_C = 100 °C	11		A
I_{DM}(1)	Drain current (pulsed)	68		A
P_{TOT}	Total power dissipation at T_C = 25 °C	125	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all,three leads to external heat sink (t = 1 s; T_C = 25 °C)	-	2.5	kV
dv/dt(2)	Peak diode recovery voltage slope	15		V/ns
°C	Storage temperature range	-55 to 150		°C
T_J	Maximum operating junction temperature	150		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 17 A, di/dt ≤ 400 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D^2PAK	TO-220	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	1		4.17	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30(1)	62.5		°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	254	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	500	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_C = 125 °C(1)	-	-	100	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8.5 A	-	162	190	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	1330	-	pF
C_{oss}	Output capacitance		-	84	-	pF
C_{rss}	Reverse transfer capacitance		-	4.8	-	pF
$C_{oss\ eq.}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	210	-	pF
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 17 A, V_{GS} = 0 to 10 V (see the Figure 15. Test circuit for gate charge behavior)	-	45	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	24	-	nC
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	4.6	-	Ω

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 17 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	6.6	-	ns
t_r	Rise time		-	19	-	ns
$t_{d(off)}$	Turn-off delay time		-	71	-	ns
t_f	Fall time		-	29	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	17	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	68	A
V_{SD}(2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs, V_{DD} = 60 V (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	286	-	ns
Q_{rr}	Reverse recovery charge		-	3.7	-	µC
I_{RRM}	Reverse recovery current		-	26	-	A
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	350	-	ns
Q_{rr}	Reverse recovery charge		-	4.8	-	µC
I_{RRM}	Reverse recovery current		-	27	-	A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK and TO-220

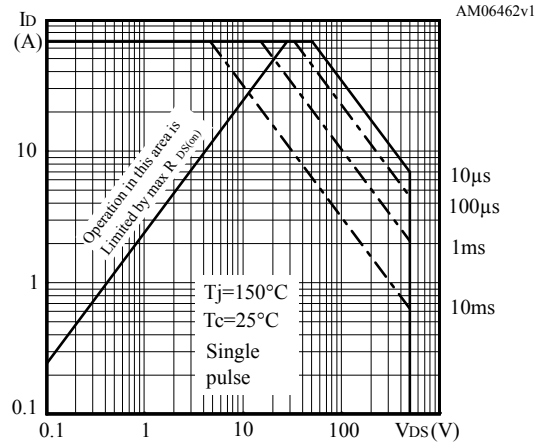


Figure 2. Normalized transient thermal impedance for D²PAK and TO-220

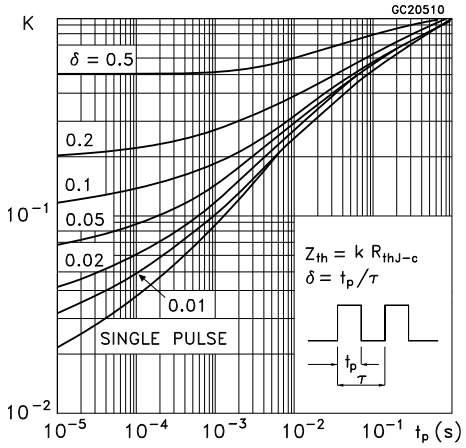


Figure 3. Safe operating area for TO-220FP

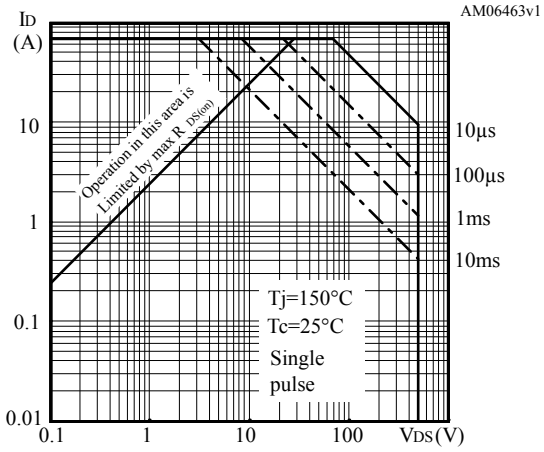


Figure 4. Normalized transient thermal impedance for TO-220FP

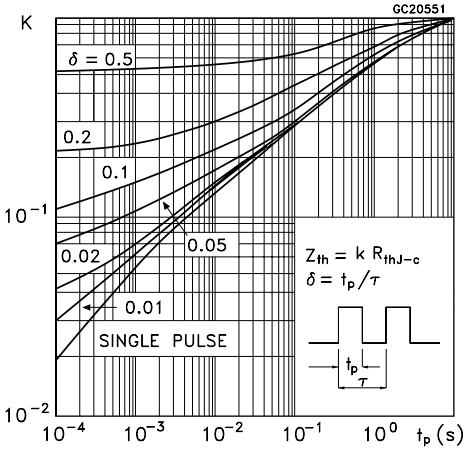


Figure 5. Typical output characteristics

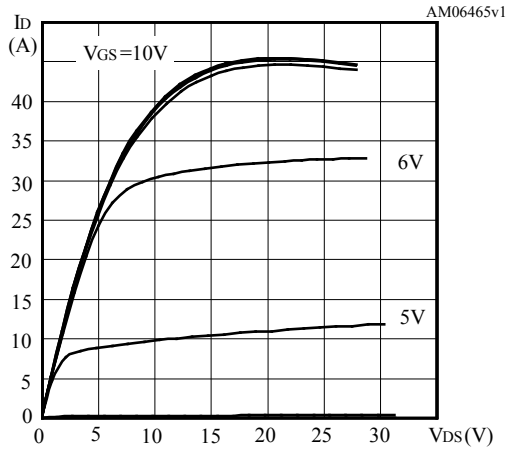


Figure 6. Typical transfer characteristics

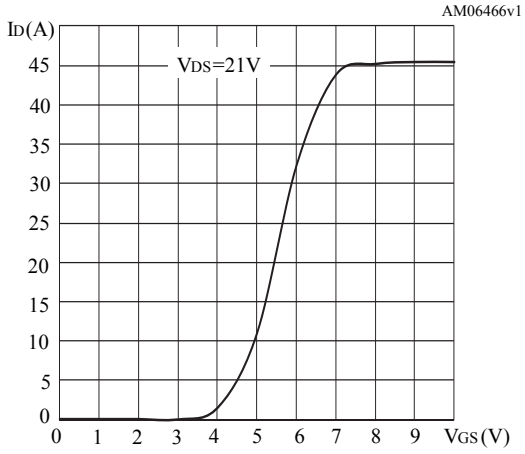


Figure 7. Typical gate charge characteristics

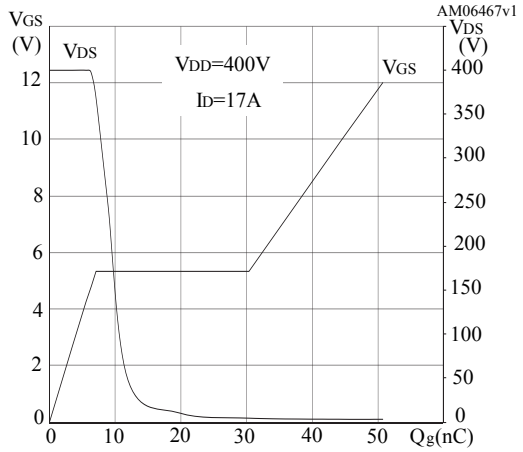


Figure 8. Typical capacitance characteristics

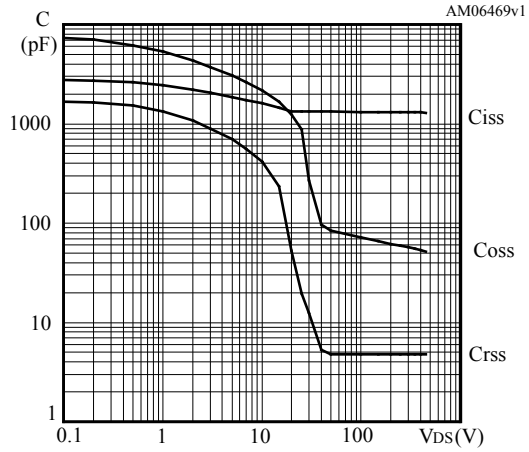


Figure 9. Typical drain-source on-resistance

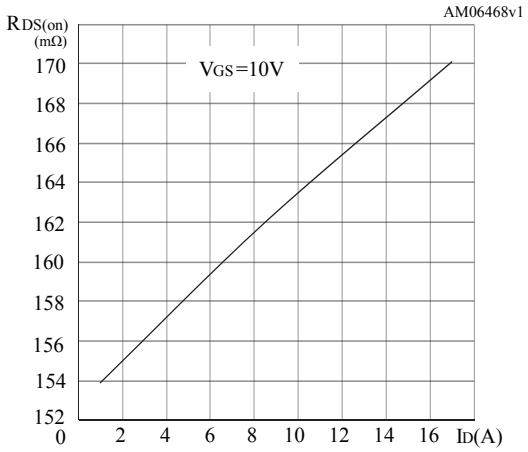


Figure 10. Normalized breakdown voltage vs temperature

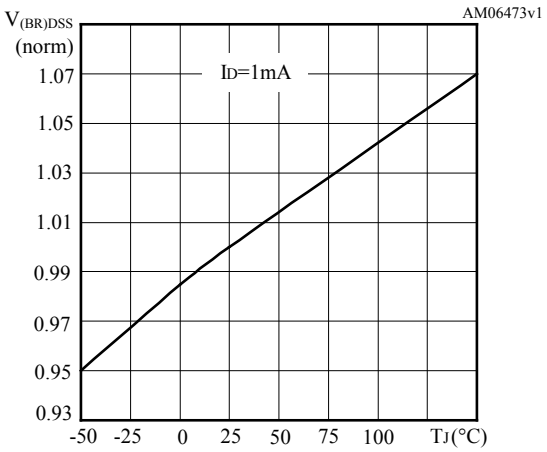


Figure 11. Normalized gate threshold vs temperature

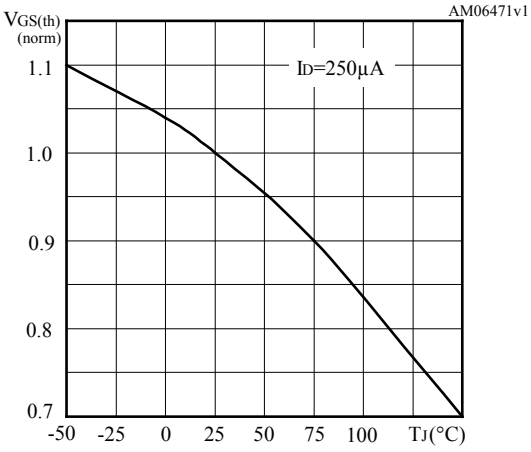


Figure 12. Normalized on-resistance vs temperature

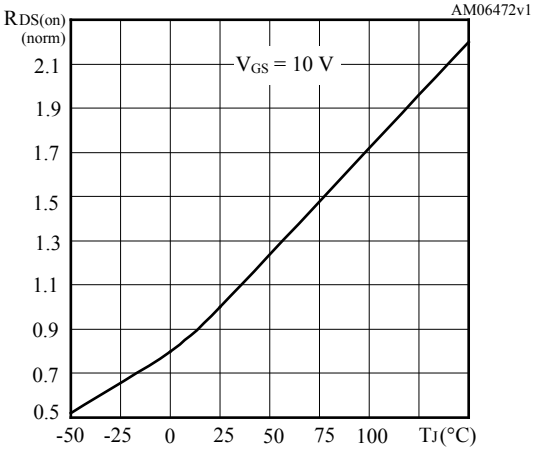
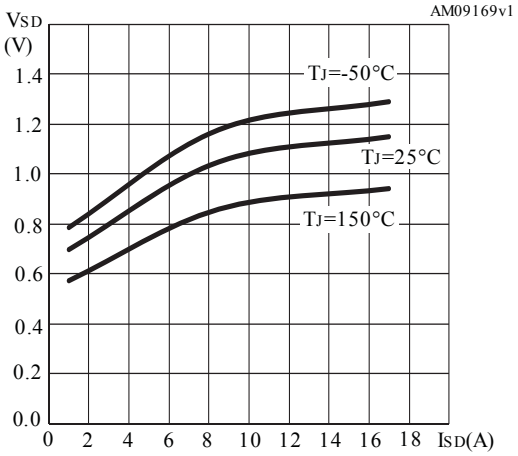


Figure 13. Typical reverse diode forward characteristics



3 Test circuits

Figure 14. Test circuit for resistive load switching times

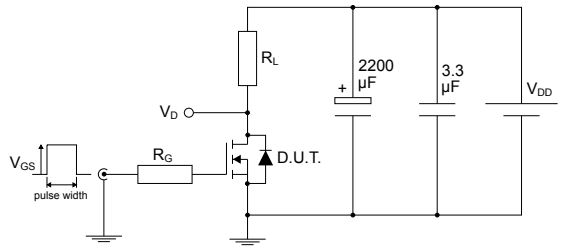


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Figure 15. Test circuit for gate charge behavior

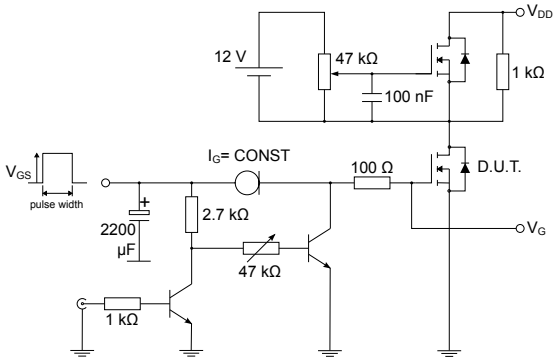

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Figure 16. Test circuit for inductive load switching and diode recovery times

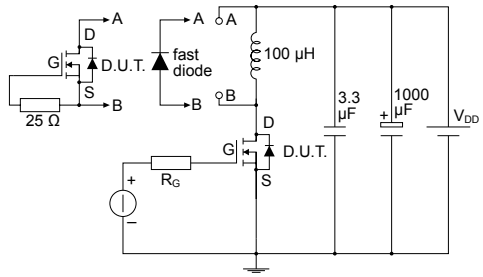

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Figure 17. Unclamped inductive load test circuit

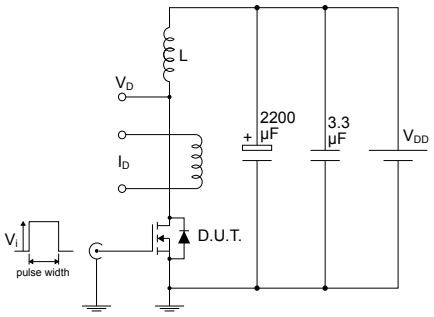

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Figure 18. Unclamped inductive waveform

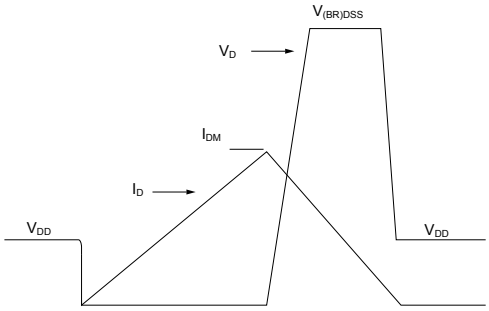

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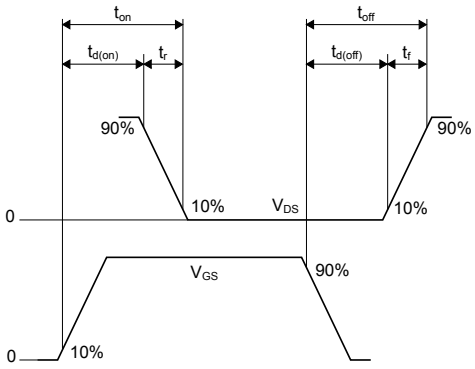
Figure 19. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 20. **D²PAK (TO-263) type A package outline**

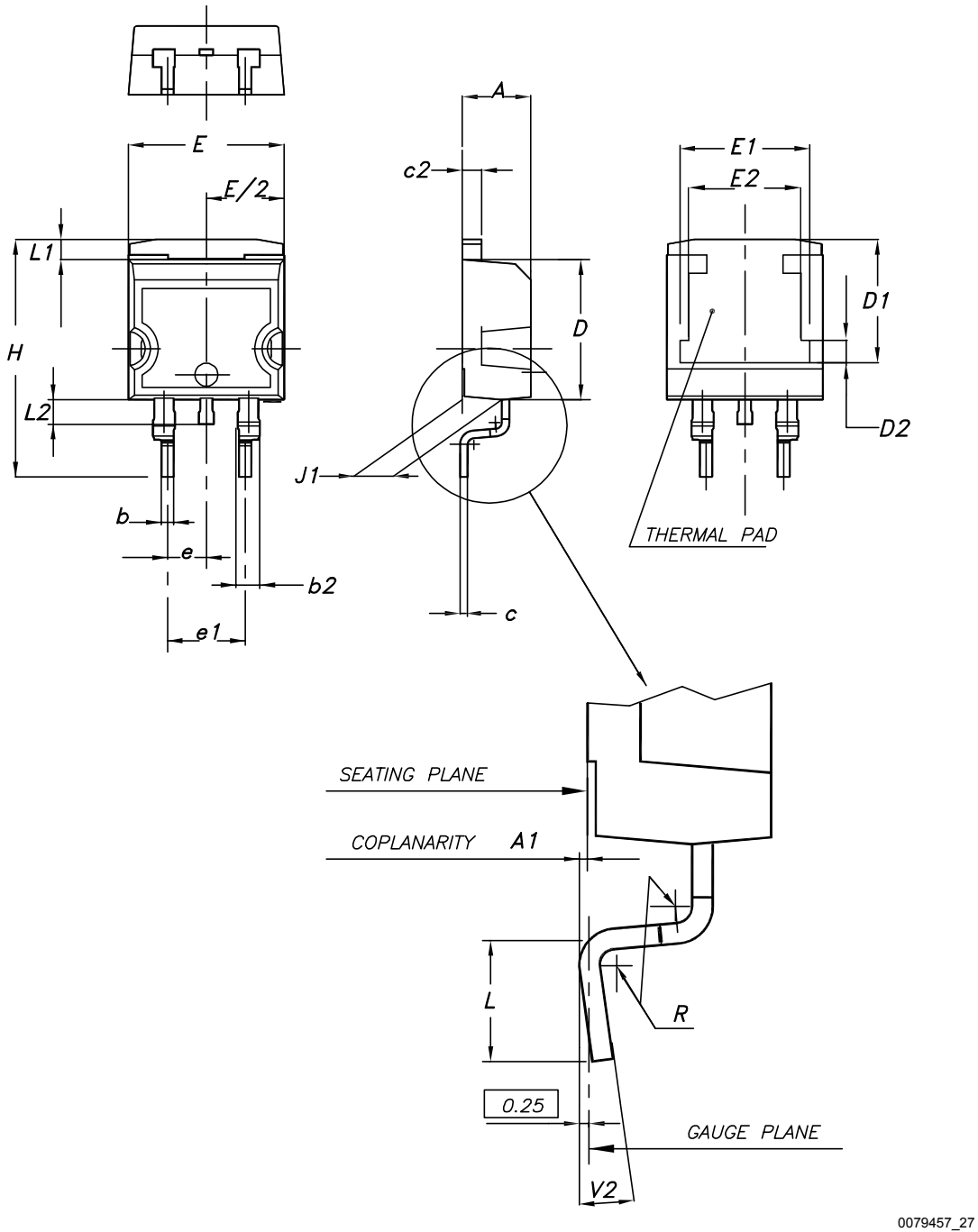
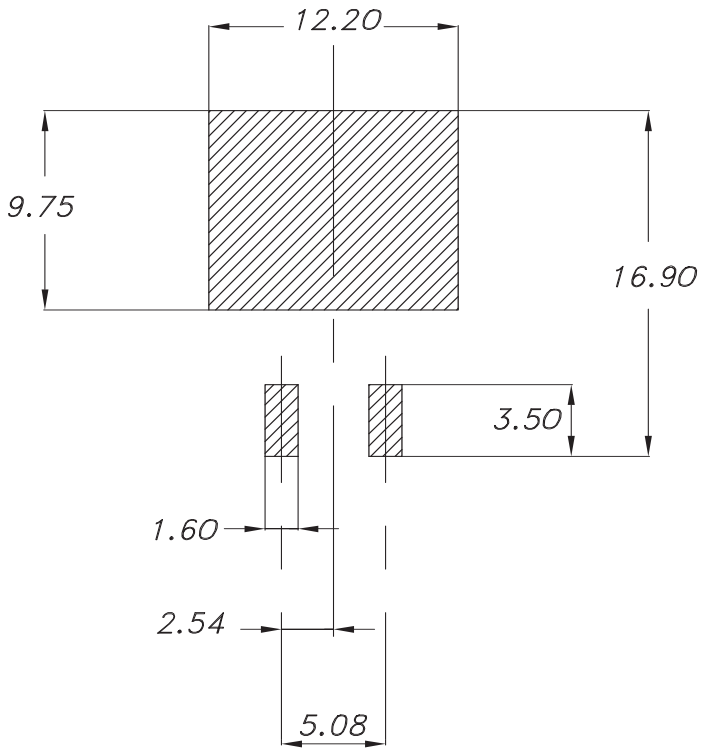


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220FP type B package information

Figure 22. **TO-220FP type B package outline**

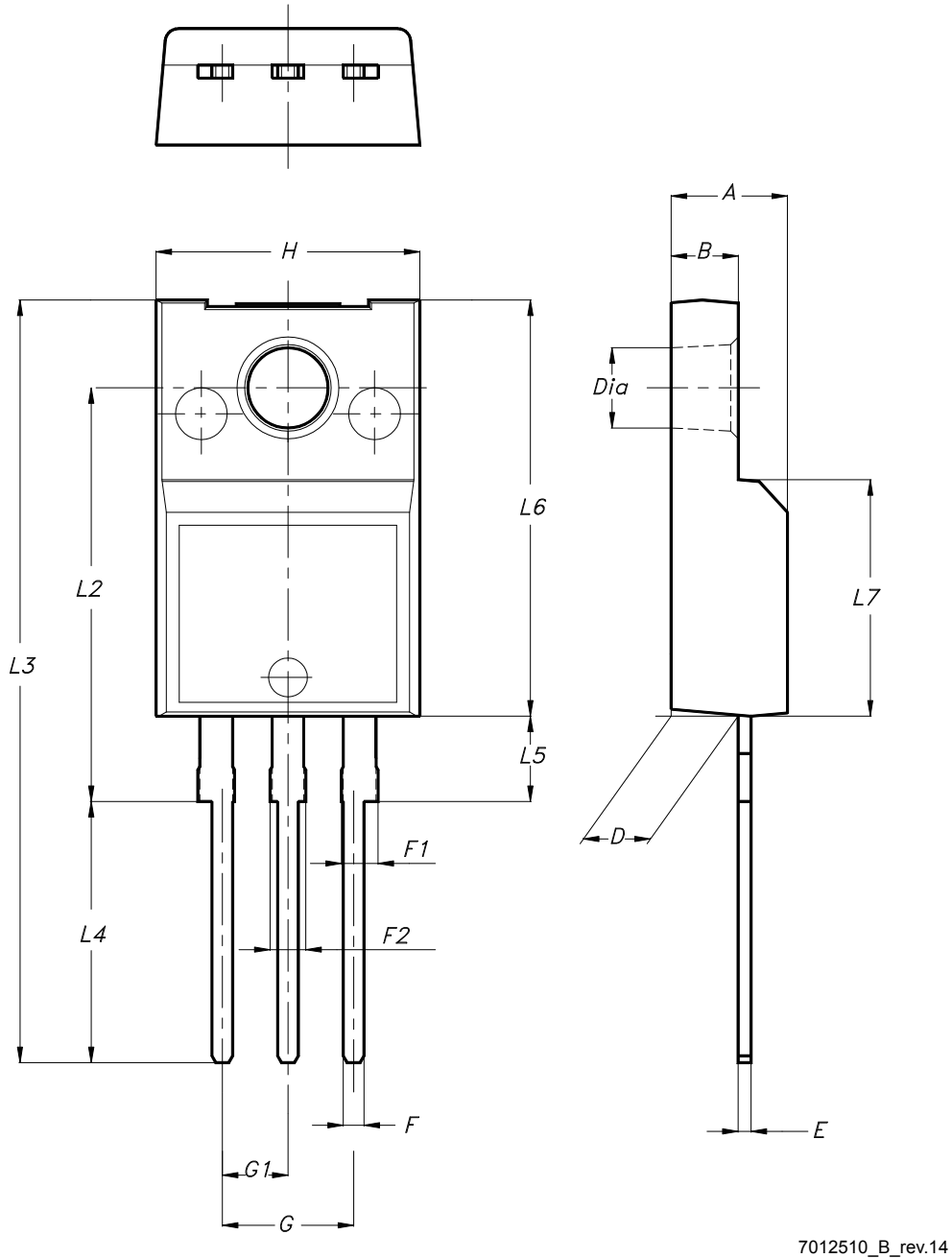


Table 9. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.3 TO-220 type A package information

Figure 23. **TO-220 type A package outline**

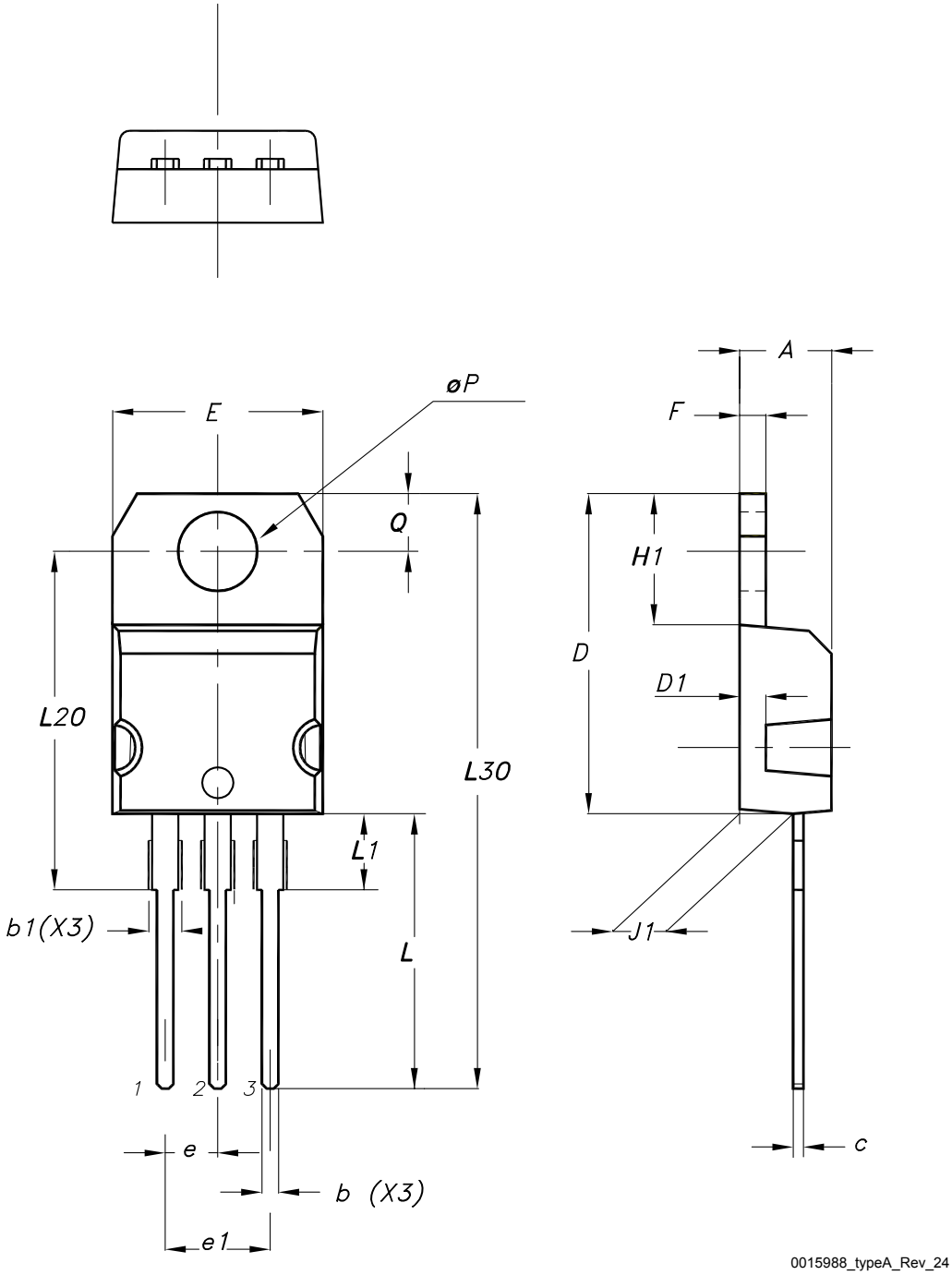
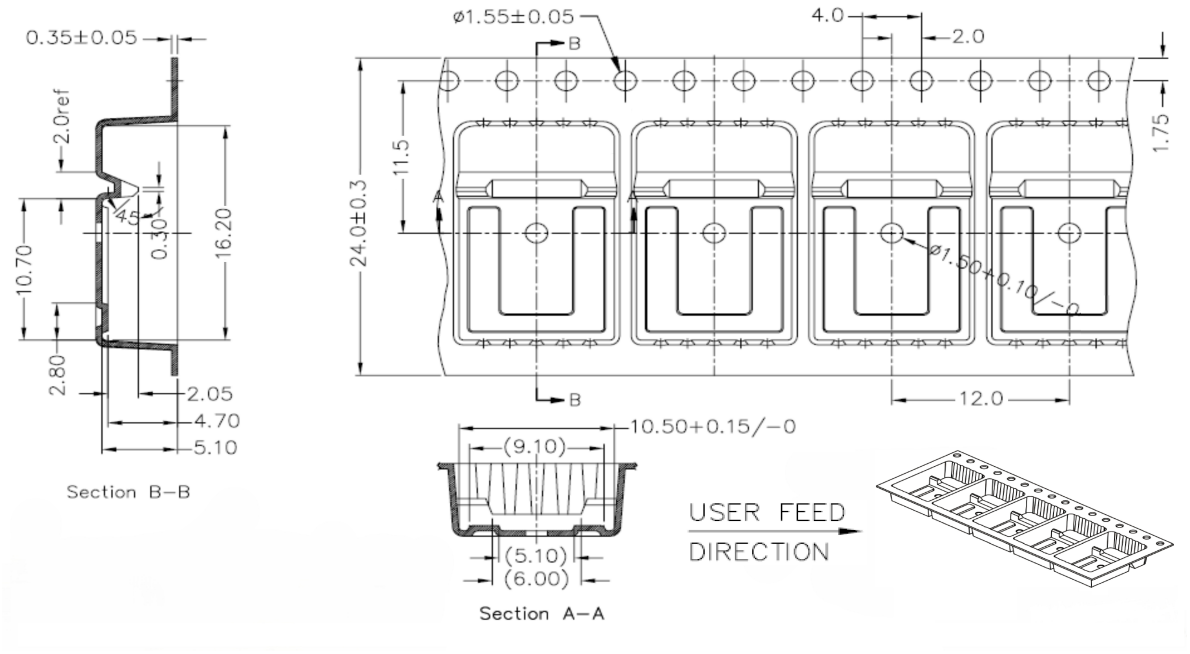


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 D²PAK packing information

Figure 24. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

5 Ordering information

Table 11. **Order codes**

Order codes	Marking	Package	Packing
STB23NM50N	23NM50N	D²PAK	Tape and reel
STF23NM50N		TO-220FP	Tube
STP23NM50N		TO-220	

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
11-Dec-2009	1	First release.
26-May-2010	2	Document status promoted from preliminary data to datasheet.
16-Sep-2010	3	Added new value in *Figure 14*, *Figure 15* and *Figure 10*.
23-May-2011	4	*Section 2.1: Electrical characteristics (curves)* has been updated.
11-Aug-2025	5	Removed order code STW23NM50N. Updated Section 4: Package information. Minor text changes.

Contents