

N-channel 650 V, 1.1 Ω typ., 6.0 A Power MOSFET
in DPAK, I²PAKFP, TO-220 and IPAK packages

Datasheet – preliminary data

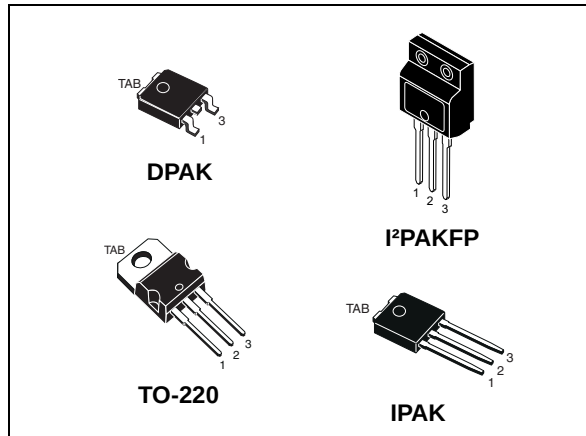
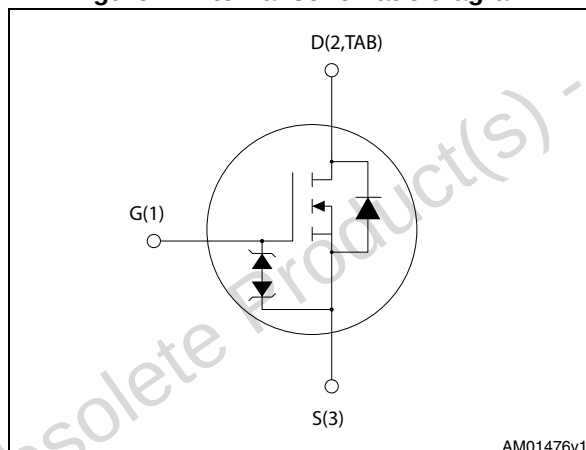


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STDLED656	650 V	1.3 Ω	6.0 A	70 W
STFILED656				25 W
STPLED656				70 W
STULED656				

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- LED lighting applications

Description

These Power MOSFETs boast extremely low on-resistance and very good dv/dt capability, rendering them suitable for buck-boost and flyback topologies.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STDLED656	LED656	DPAK	Tape and reel
STFILED656		I ² PAKFP (TO-281)	Tube
STPLED656		TO-220	
STULED656		IPAK	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220 IPAK	I ² PAKFP	
V _{DS}	Drain- source voltage	650		V
V _{GS}	Gate- source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	6.0	6.0 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	3.3	3.3 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	24.0	24.0 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	30	110	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	5.4		A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	2.5		kV
ESD	Gate-source human body model (C=100 pF, R=1.5 kΩ)			
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12		V/ns
V _{ISO}	Insulation withstand voltage (AC)		2500	V
T _{stg}	Storage temperature	- 55 to 150		°C
T _J	Operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 5.4 A, di/dt ≤ 400 A/μs, V_{DD} = 80% V_{(BR)DSS}.

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	I ² PAKFP	TO-220	IPAK	
R _{thj-case}	Thermal resistance junction-case max.		4.17	-	1.14	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max		62.5	-	100	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max.	50		-		°C/W

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650 \text{ V}$ $V_{DS} = 650 \text{ V}$, $T_C = 125^\circ \text{C}$			0.8 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$; $V_{DS} = 0$			± 9	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50 \mu\text{A}$	3	3.6	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$, $I_D = 2.7 \text{ A}$		1.1	1.3	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	895 67 12.5	-	pF pF pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent capacitance energy related	$V_{DS} = 0 \text{ to } 520 \text{ V}$, $V_{GS} = 0$	-	27	-	pF
R_g	Gate input resistance	$f = 1 \text{ MHz}$ open drain	-	3.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 500 \text{ V}$, $I_D = 5.4 \text{ A}$, $V_{GS} = 10 \text{ V}$ (see Figure 17)	-	34 4 21	-	nC nC nC

1. $C_{oss \text{ eq.}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	$V_{DD} = 325 \text{ V}$, $I_D = 2.7 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 17)	-	14 10 44 24	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		5.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		21.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.4 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 5.4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	285		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	5100		nC
I_{RRM}	Reverse recovery current	(see Figure 21)	-	14		A
t_{rr}	Reverse recovery time	$I_{SD} = 5.4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	330		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	2500		nC
I_{RRM}	Reverse recovery current	(see Figure 21)	-	15.5		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK, TO-220 and IPAK

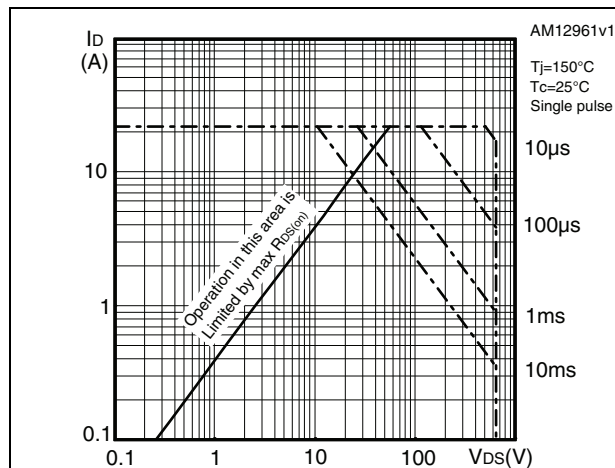


Figure 3. Thermal impedance for DPAK, TO-220 and IPAK

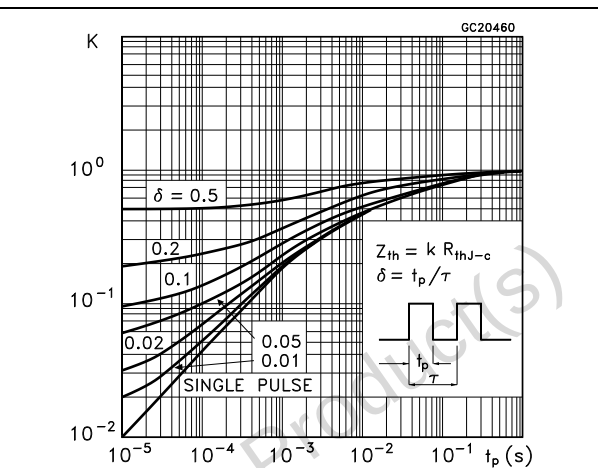


Figure 4. Safe operating area for I²PAKFP

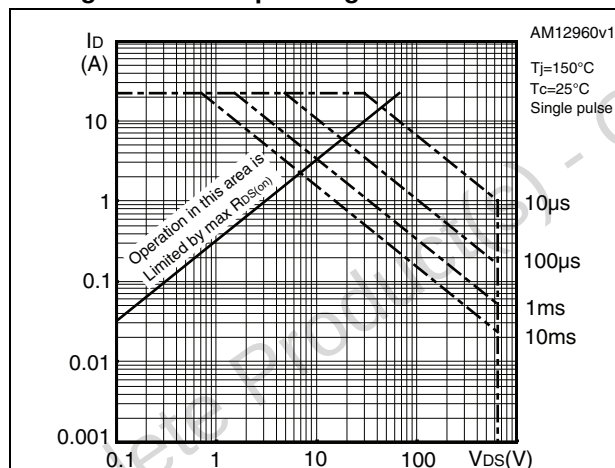


Figure 5. Thermal impedance for I²PAKFP

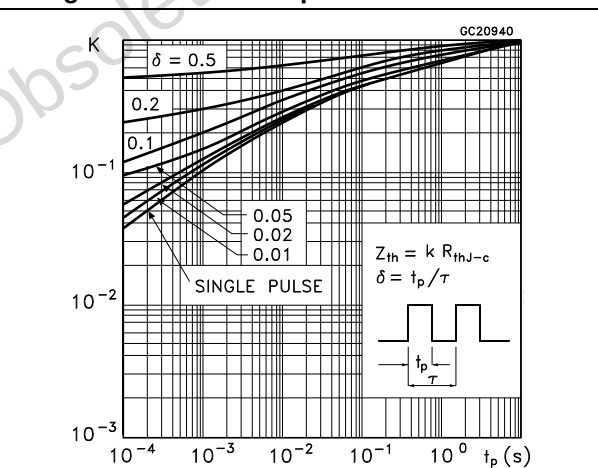


Figure 6. Output characteristics

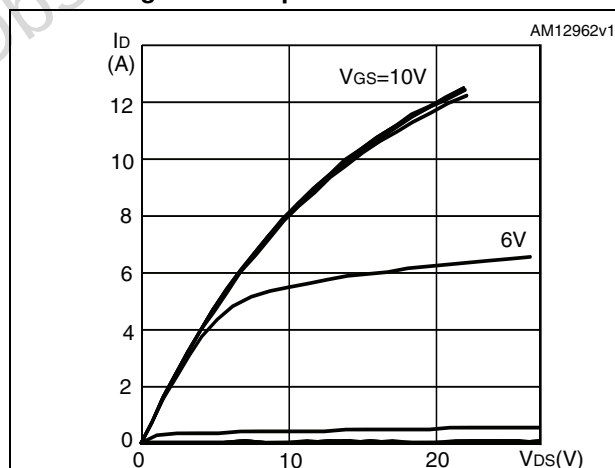


Figure 7. Transfer characteristics

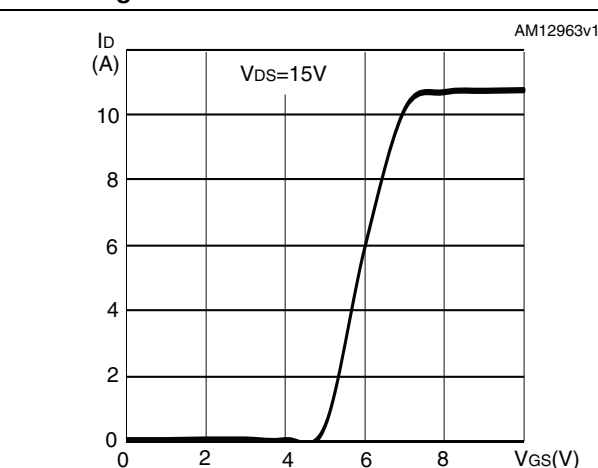


Figure 8. Gate charge vs gate-source voltage

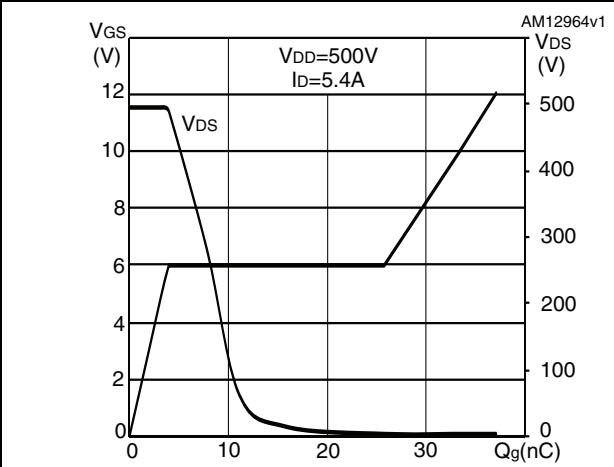


Figure 9. Static drain-source on-resistance

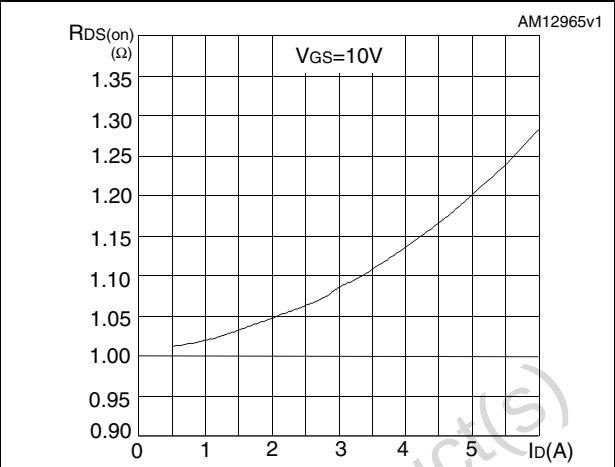


Figure 10. Capacitance variations

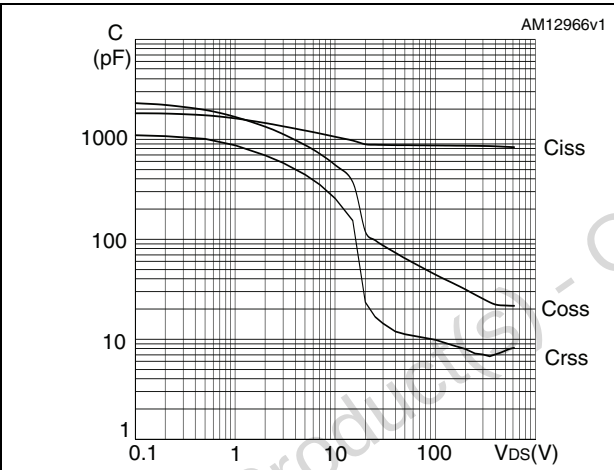


Figure 11. Output capacitance stored energy

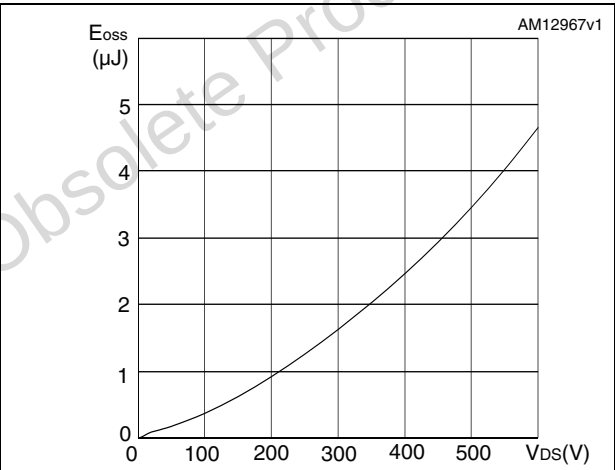


Figure 12. Normalized gate threshold voltage vs temperature

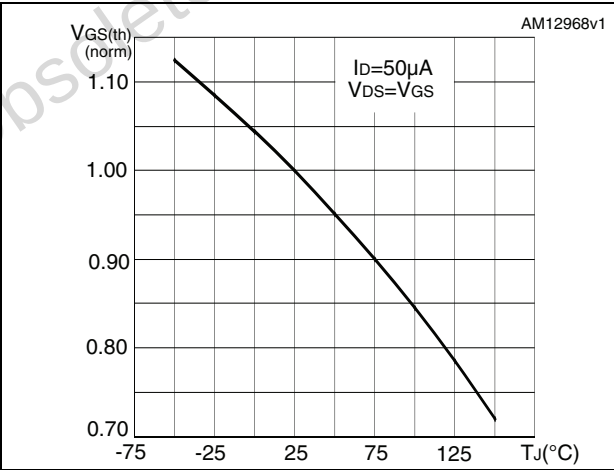


Figure 13. Normalized on-resistance vs temperature

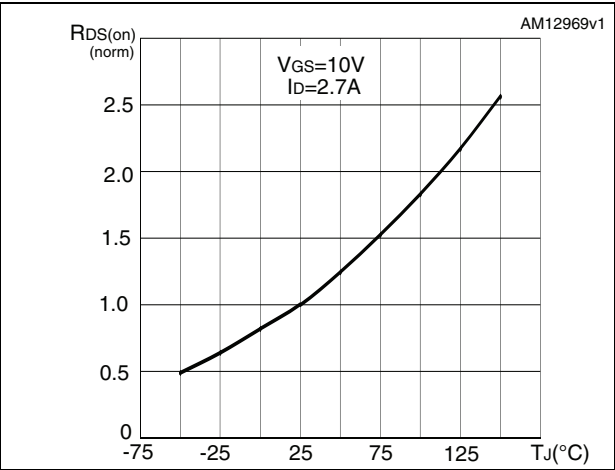


Figure 14. Normalized BV_{DSS} vs temperature

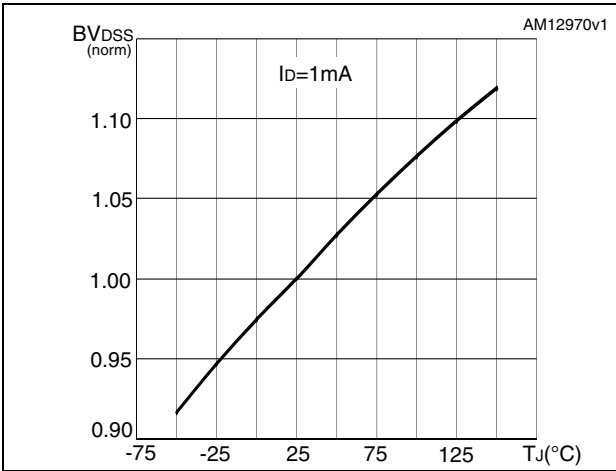


Figure 15. Source-drain diode forward characteristics

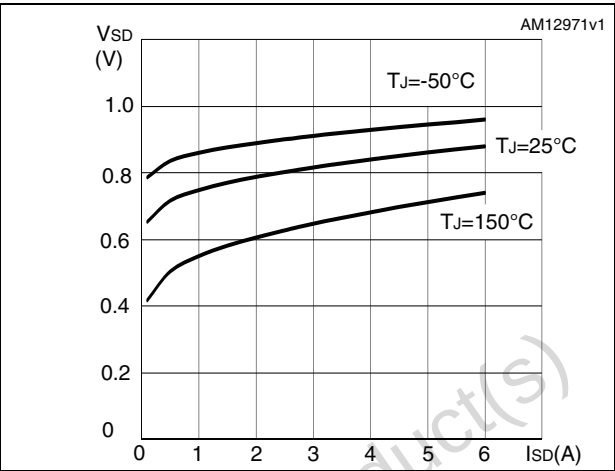
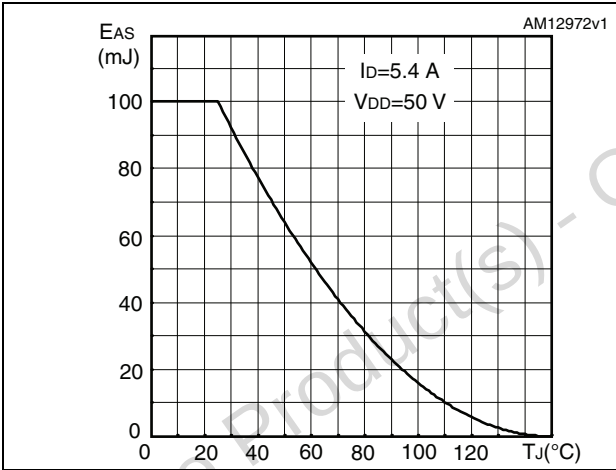


Figure 16. Maximum avalanche energy vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load

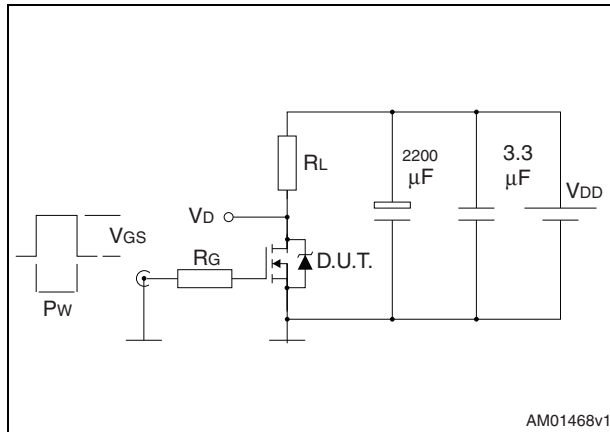


Figure 18. Gate charge test circuit

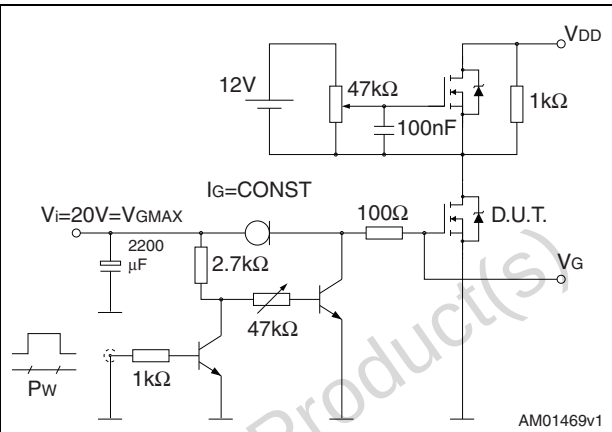


Figure 19. Test circuit for inductive load switching and diode recovery times

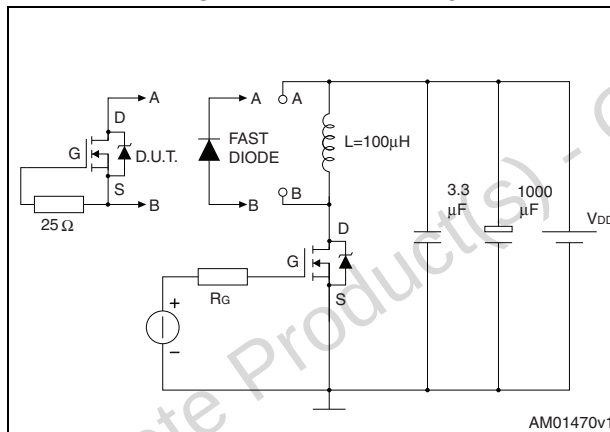


Figure 20. Unclamped inductive load test circuit

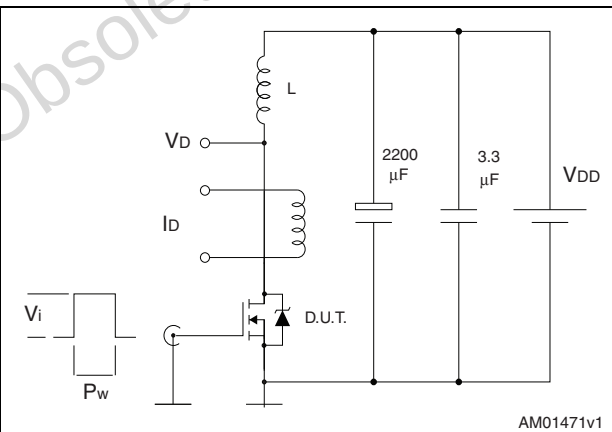


Figure 21. Unclamped inductive waveform

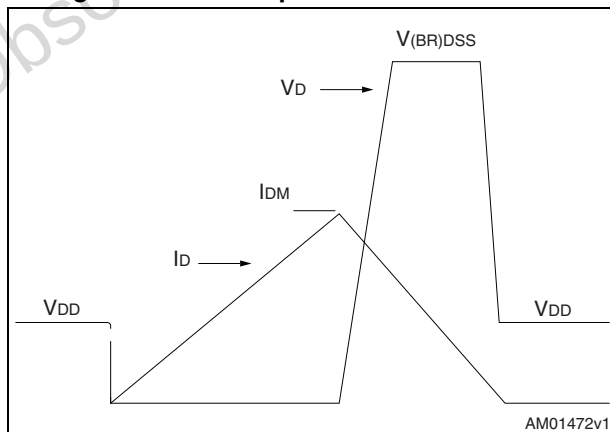
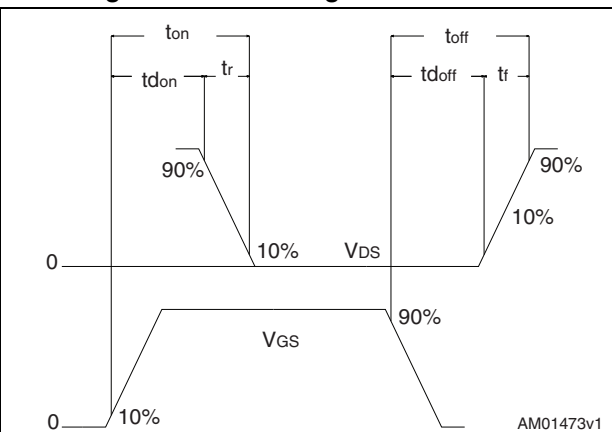


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 23. DPAK (TO-252) drawing

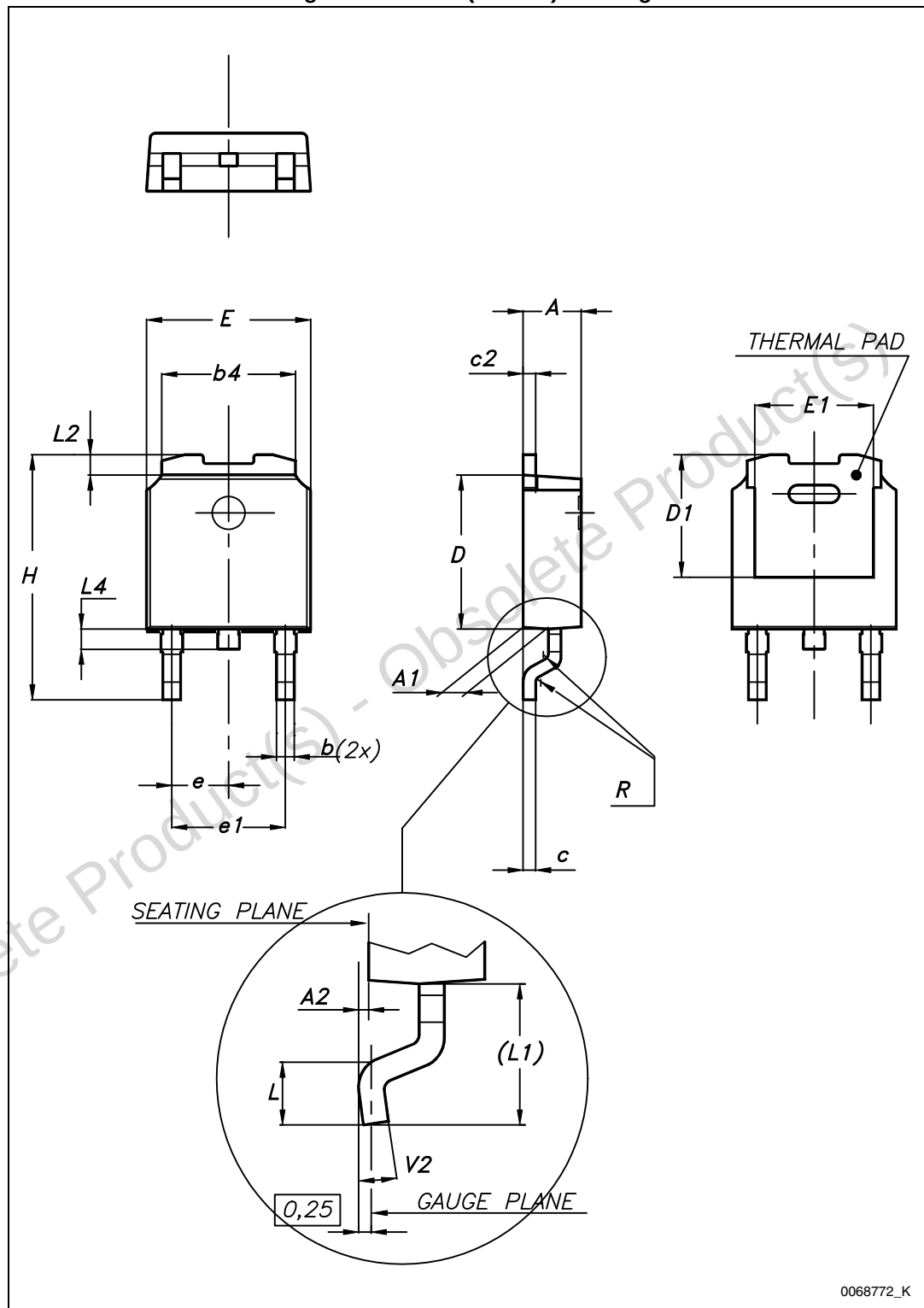
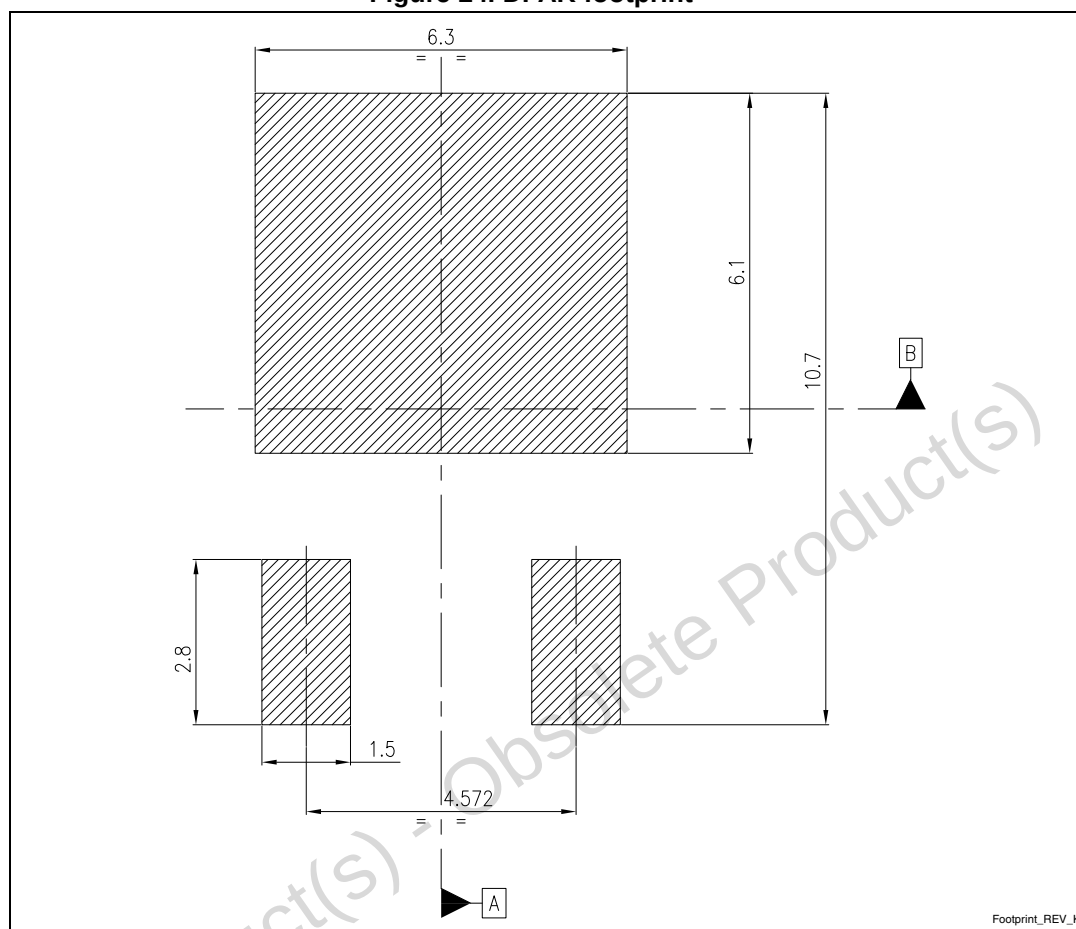


Figure 24. DPAK footprint (a)



a. All dimensions are in millimeters

Table 10. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30	7.50	

Figure 25. I²PAKFP (TO-281) drawing

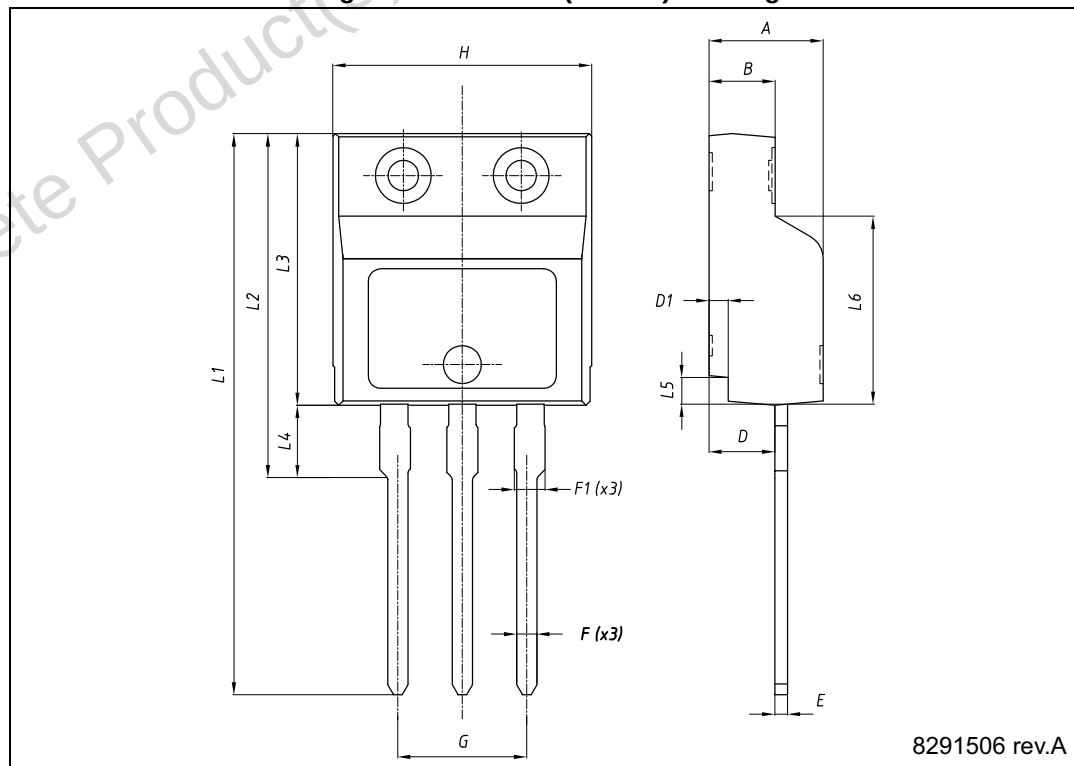


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing

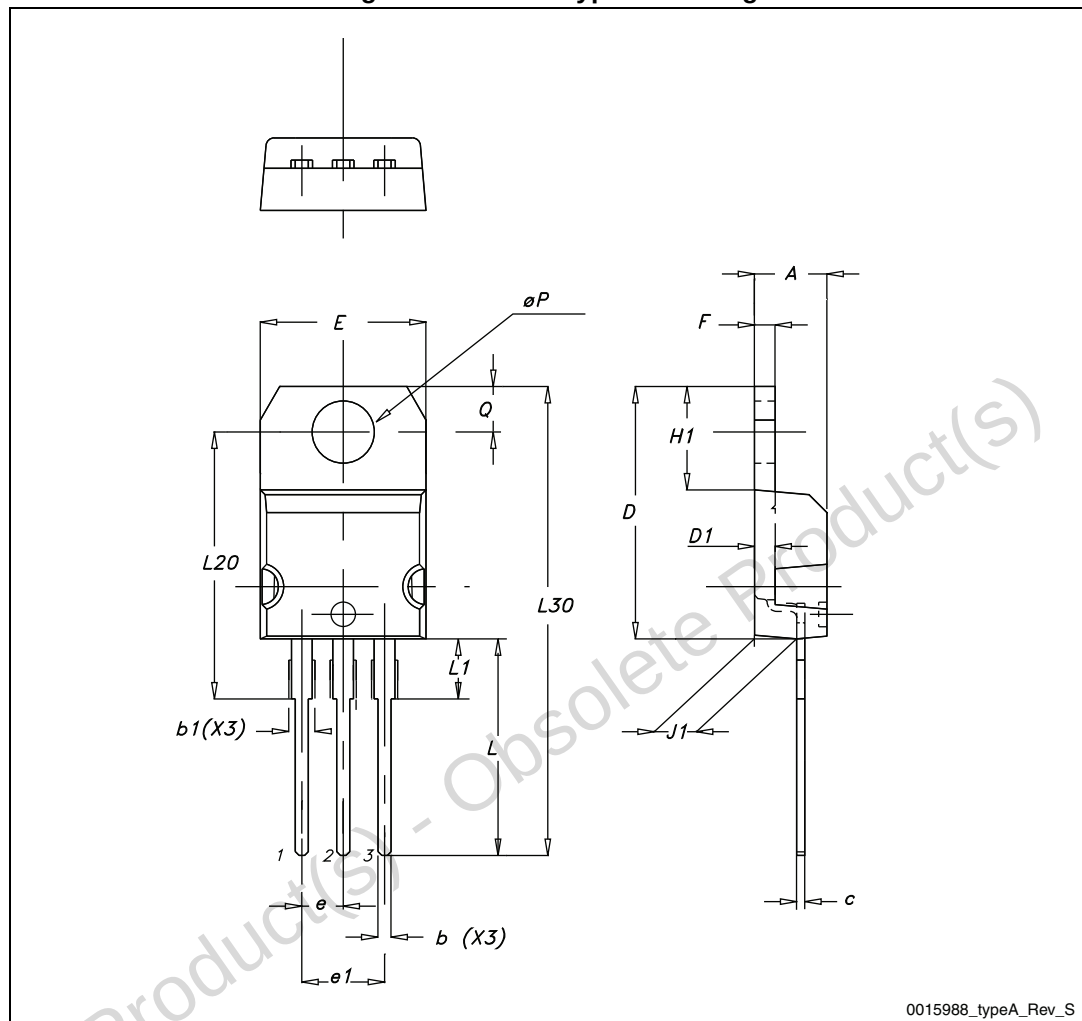
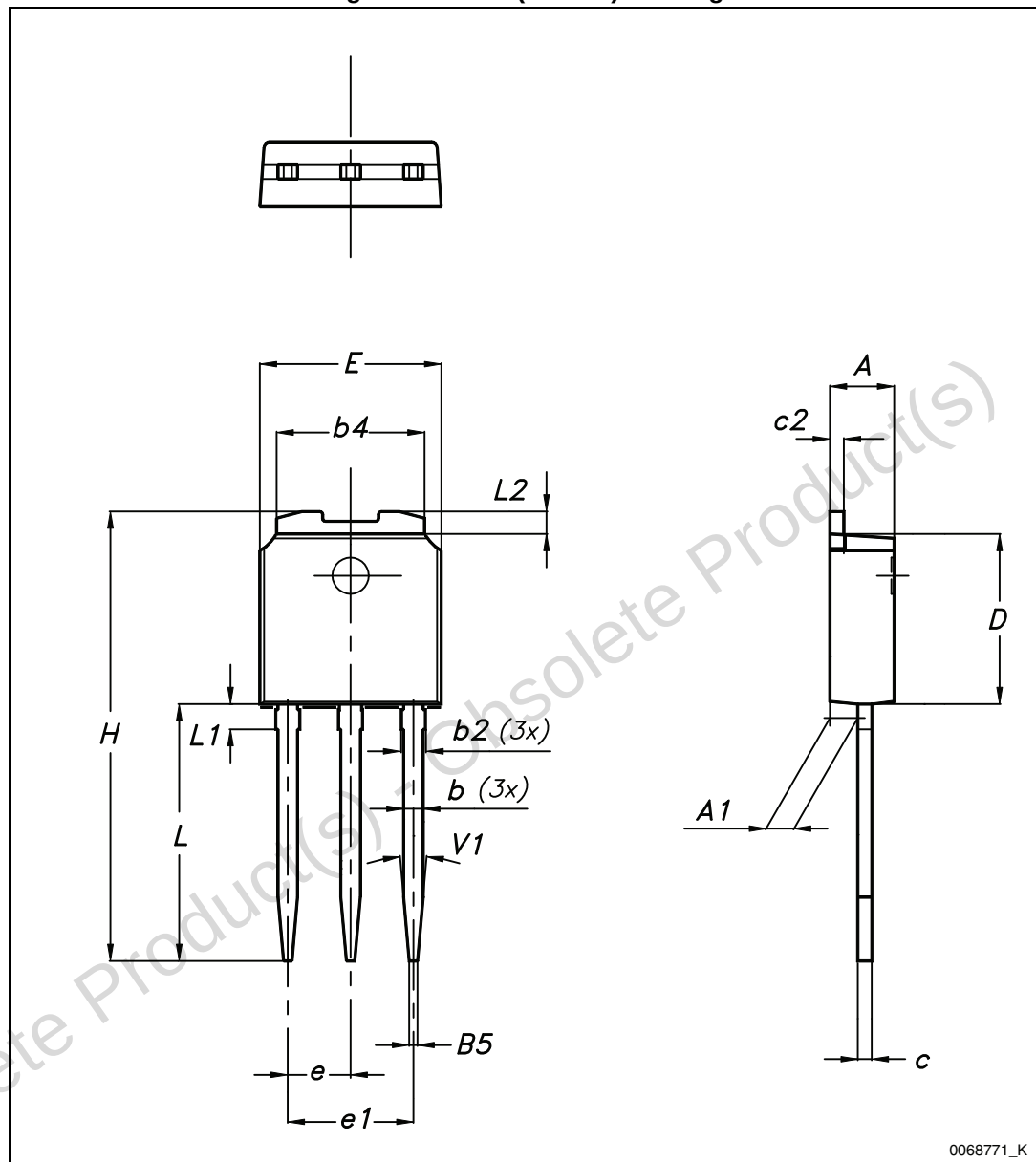


Table 12. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 27. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 28. Tape for DPAK (TO-252)

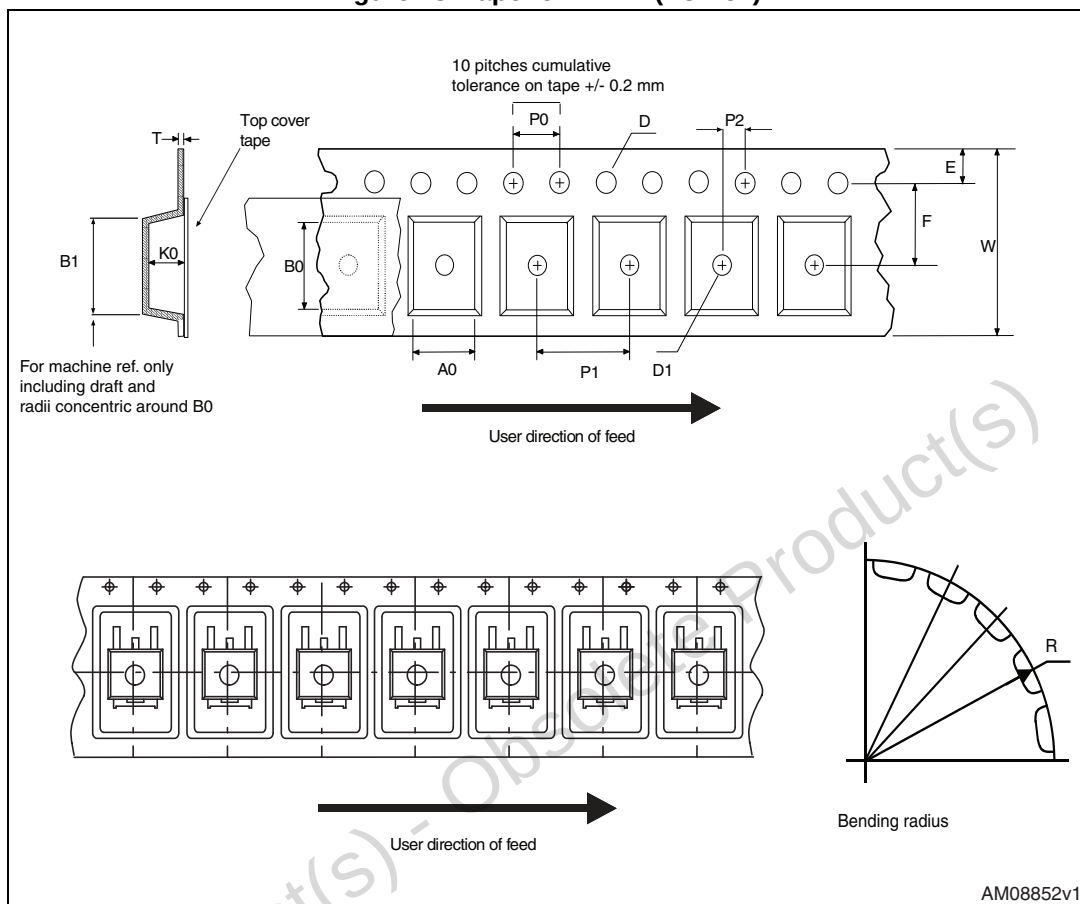
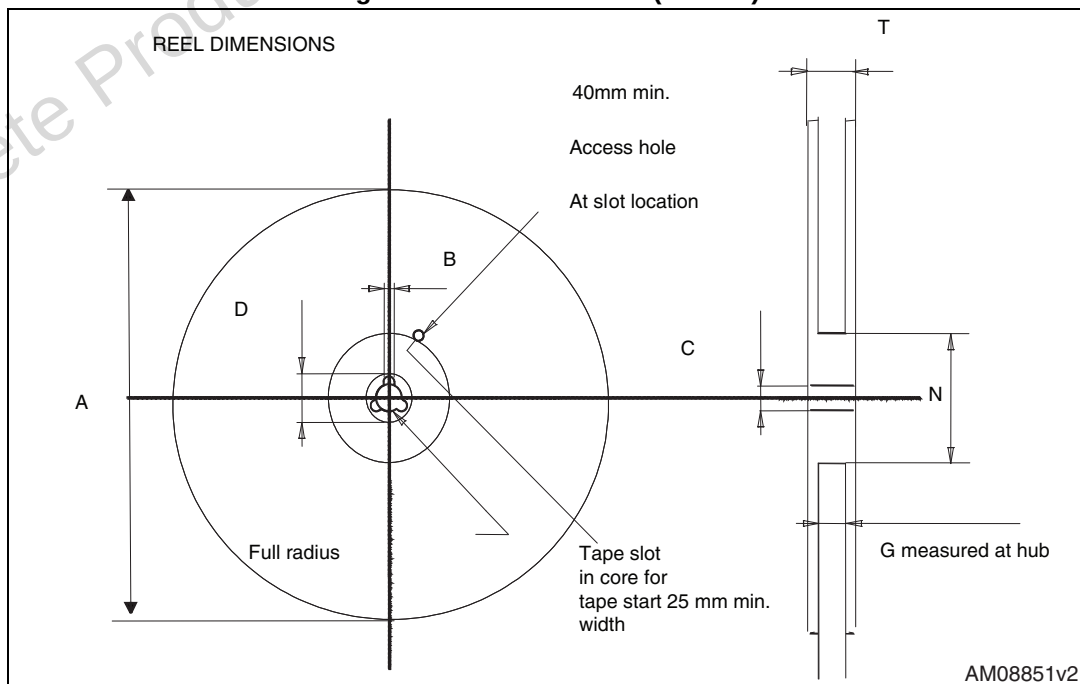


Figure 29. Reel for DPAK (TO-252)



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
26-Mar-2013	1	First release.

Obsolete Product(s) - Obsolete Product(s)

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