

HEF4051B

8-channel analog multiplexer/demultiplexer

Rev. 11 — 11 September 2014

Product data sheet

1. General description

The HEF4051B is an 8-channel analog multiplexer/demultiplexer with three address inputs (S1 to S3), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z). With $\overline{E}$ LOW, one of the eight switches is selected (low-impedance ON-state) by S1 to S3. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 to S3, and $\overline{E}$). The V_{DD} to V_{SS} range is 3 V to 15 V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

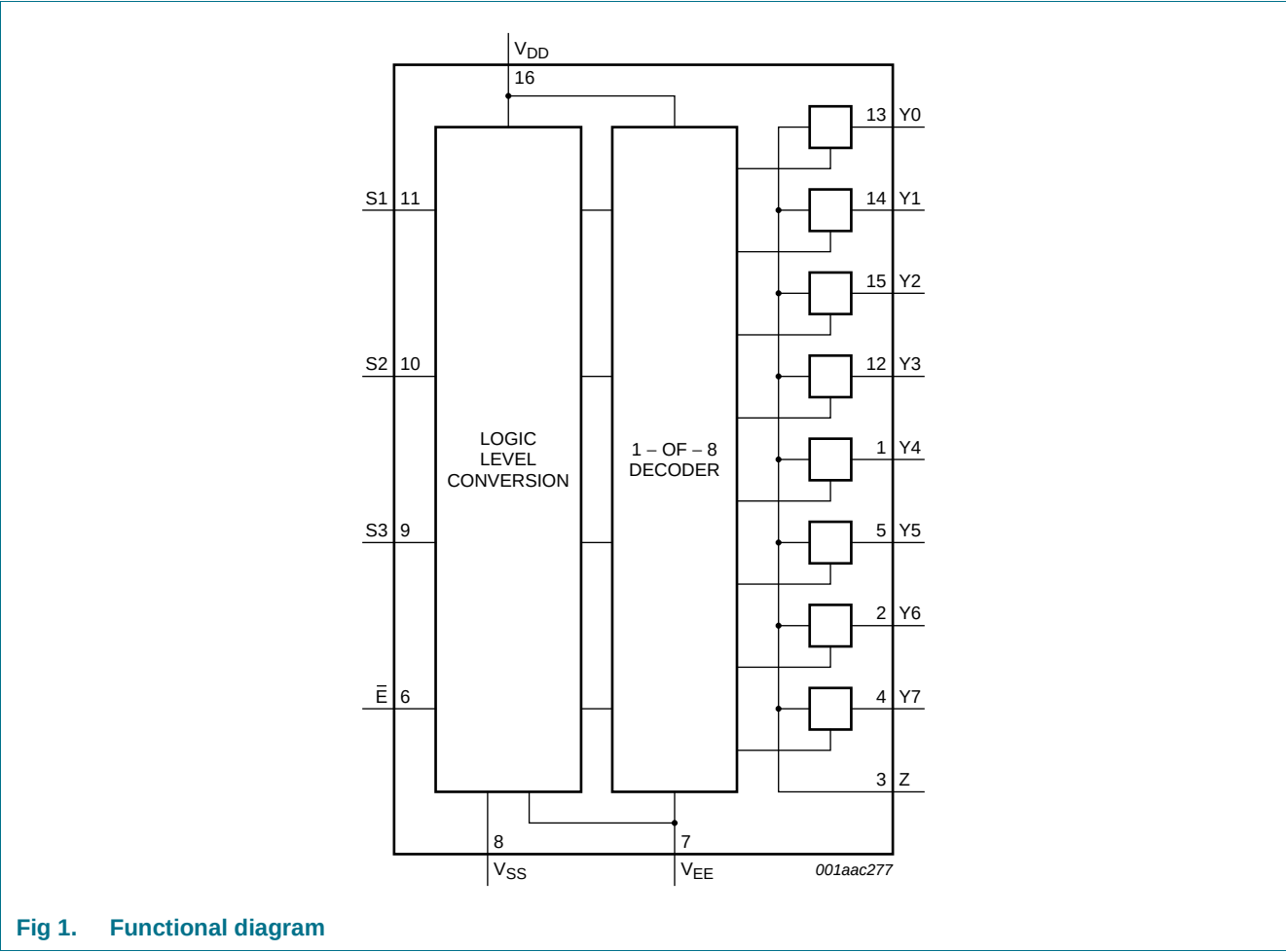


4. Ordering information

Table 1. Ordering information
All types operate from -40 °C to +125 °C.

Type number	Package		
	Name	Description	Version
HEF4051BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4051BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4051BTS	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
HEF4051BTT	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram



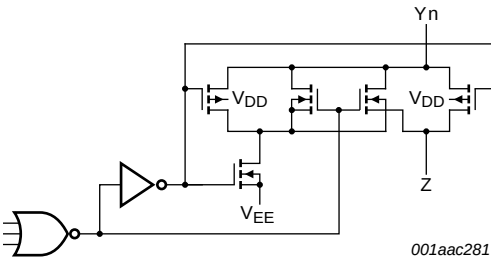


Fig 2. Schematic diagram (one switch)

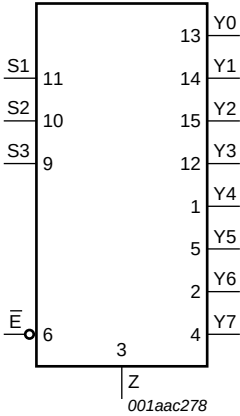


Fig 3. Logic symbol

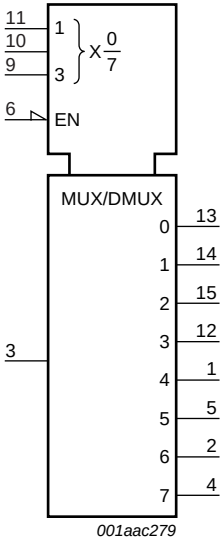


Fig 4. IEC logic symbol

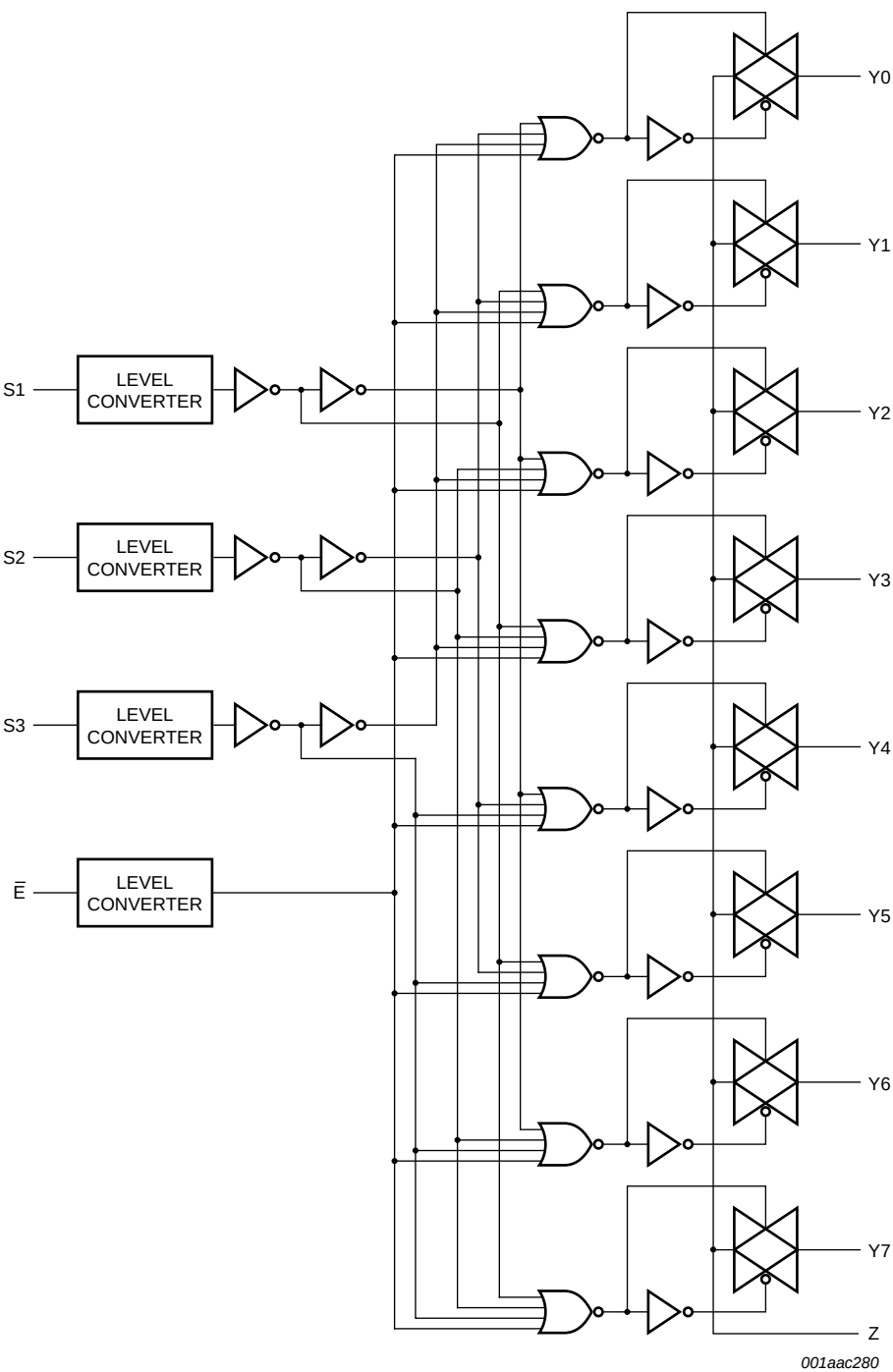
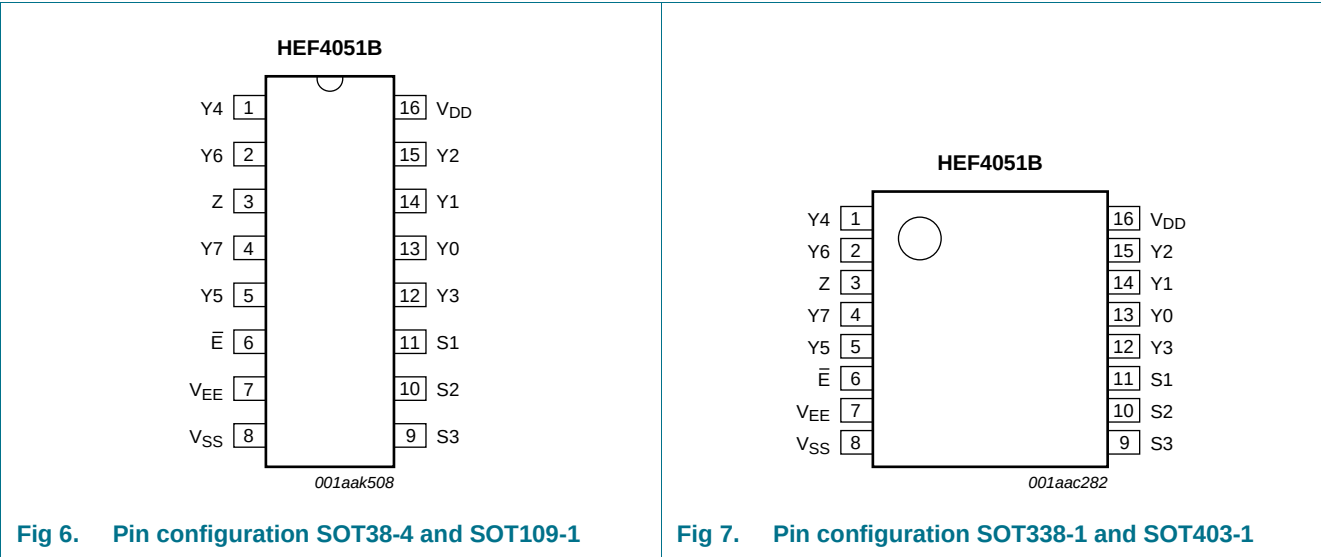


Fig 5. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\bar{E}$	6	enable input (active LOW)
V _{EE}	7	supply voltage
V _{SS}	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	13, 14, 15, 12, 1, 5, 2, 4	independent input or output
Z	3	common output or input
V _{DD}	16	supply voltage

7. Functional description

7.1 Function table

Table 3. Function table^[1]

Input				Channel ON
$\overline{E}$	S3	S2	S1	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
V_{EE}	supply voltage	referenced to V_{DD}	^[1] -18	+0.5	V
I_{IK}	input clamping current	pins Sn and $\overline{E}$; $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[2]		
		DIP16 package	-	750	mW
		SO16 package	-	500	mW
		SSOP16 package	-	500	mW
		TSSOP16 package	-	500	mW
P	power dissipation	per output	-	100	mW

[1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE} .

[2] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
 For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	see Figure 8	3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

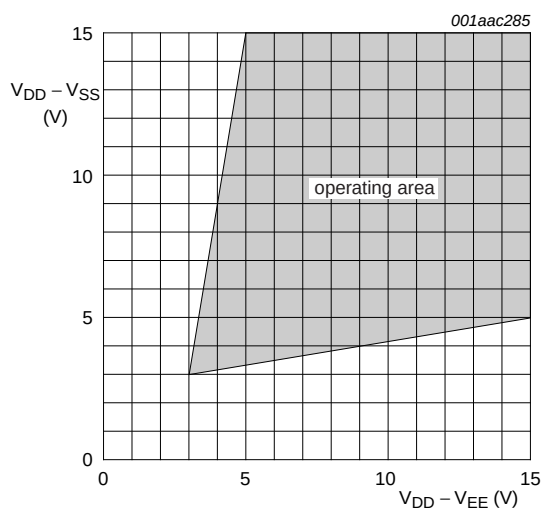


Fig 8. Operating area as a function of the supply voltages

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = V_{EE} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		$T_{amb} = 125\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
I_I	input leakage current		15 V	-	± 0.1	-	± 0.1	-	± 1.0	-	± 1.0	μA

Table 6. Static characteristics ...continued
 $V_{SS} = V_{EE} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$		$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$		$T_{\text{amb}} = 85\text{ }^{\circ}\text{C}$		$T_{\text{amb}} = 125\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$I_{S(\text{OFF})}$	OFF-state leakage current	Z port; all channels OFF; see Figure 9	15 V	-	-	-	1000	-	-	-	-	nA
		Y port; per channel; see Figure 10	15 V	-	-	-	200	-	-	-	-	nA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C_I	input capacitance	$S_n, \bar{E}$ inputs	-	-	-	-	7.5	-	-	-	-	pF

10.1 Test circuits

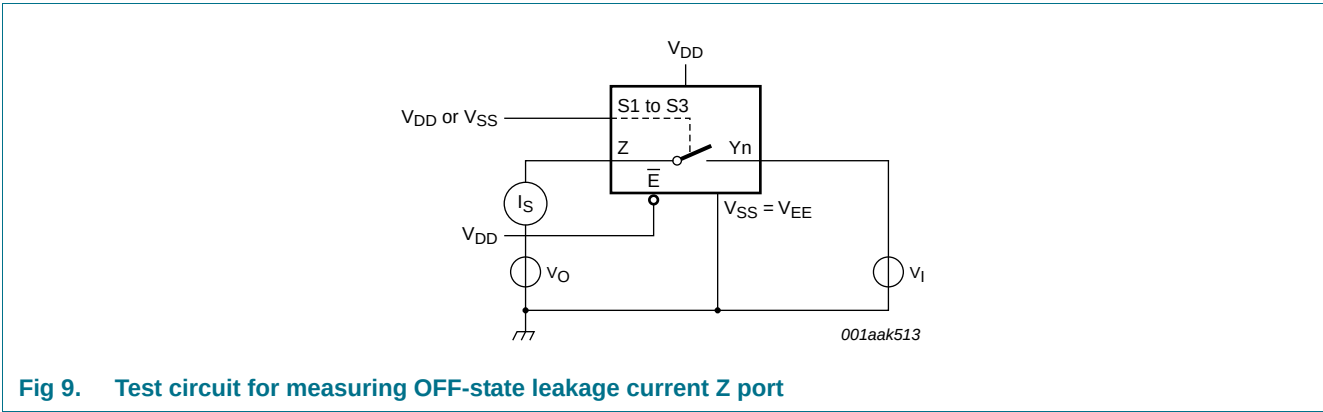


Fig 9. Test circuit for measuring OFF-state leakage current Z port

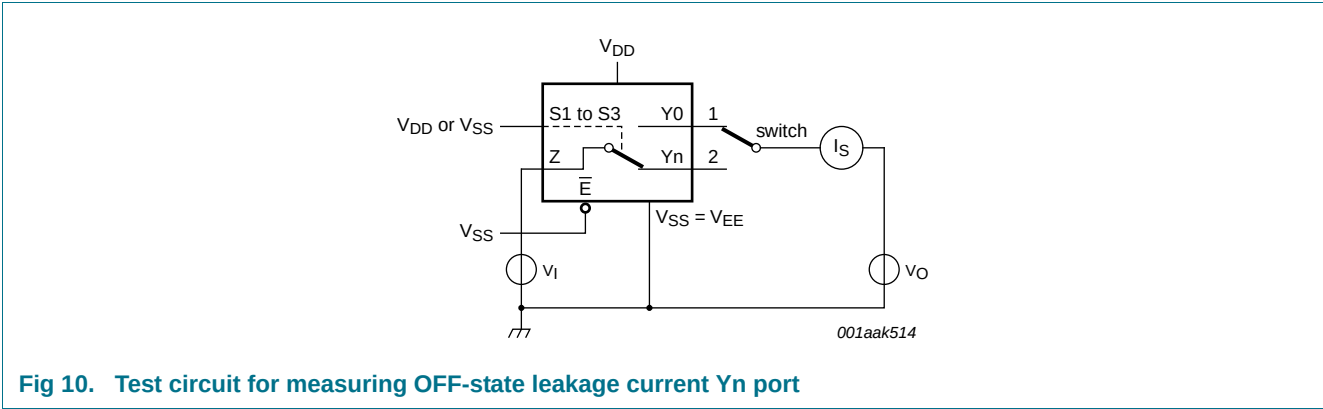


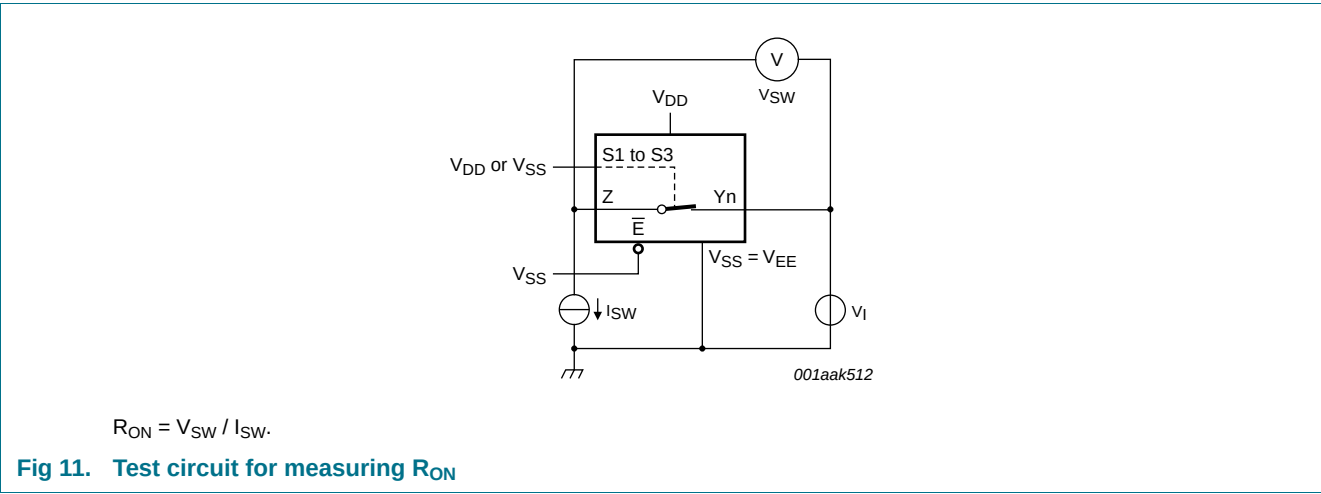
Fig 10. Test circuit for measuring OFF-state leakage current Yn port

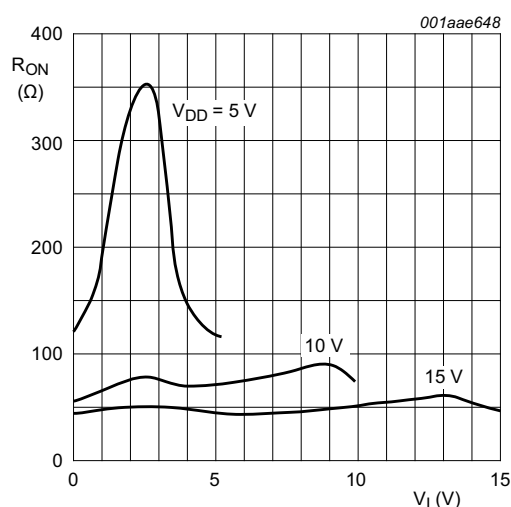
10.2 ON resistance

Table 7. ON resistance
T_amb = 25 °C; I_SW = 200 μA; V_SS = V_EE = 0 V.

Symbol	Parameter	Conditions	V _{DD} - V _{EE}	Typ	Max	Unit
R _{ON(peak)}	ON resistance (peak)	V _I = 0 V to V _{DD} - V _{EE} ; see Figure 11 and Figure 12	5 V	350	2500	Ω
			10 V	80	245	Ω
			15 V	60	175	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = 0 V; see Figure 11 and Figure 12	5 V	115	340	Ω
			10 V	50	160	Ω
			15 V	40	115	Ω
		V _I = V _{DD} - V _{EE} ; see Figure 11 and Figure 12	5 V	120	365	Ω
			10 V	65	200	Ω
			15 V	50	155	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I = 0 V to V _{DD} - V _{EE} ; see Figure 11	5 V	25	-	Ω
			10 V	10	-	Ω
			15 V	5	-	Ω

10.2.1 ON resistance waveform and test circuit



Fig 12. Typical R_{ON} as a function of input voltage

11. Dynamic characteristics

Table 8. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{SS} = V_{EE} = 0\text{ V}$; for test circuit see [Figure 16](#).

Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	Yn, Z to Z, Yn; see Figure 13	5 V	15	30	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to Yn, Z; see Figure 14	5 V	150	300	ns
			10 V	60	120	ns
			15 V	45	90	ns
t_{PLH}	LOW to HIGH propagation delay	Yn, Z to Z, Yn; see Figure 13	5 V	15	30	ns
			10 V	5	10	ns
			15 V	5	10	ns
		Sn to Yn, Z; see Figure 14	5 V	150	300	ns
			10 V	65	130	ns
			15 V	45	90	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{E}$ to Yn, Z; see Figure 15	5 V	120	240	ns
			10 V	90	180	ns
			15 V	85	170	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{E}$ to Yn, Z; see Figure 15	5 V	140	280	ns
			10 V	55	110	ns
			15 V	40	80	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{E}$ to Yn, Z; see Figure 15	5 V	145	290	ns
			10 V	120	240	ns
			15 V	115	230	ns

Table 8. Dynamic characteristics ...continued
 $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{SS} = V_{EE} = 0\text{ V}$; for test circuit see Figure 16.

Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
t_{PZL}	OFF-state to LOW propagation delay	$\bar{E}$ to Y_n, Z ; see Figure 15	5 V	140	280	ns
			10 V	55	110	ns
			15 V	40	80	ns

11.1 Waveforms and test circuit

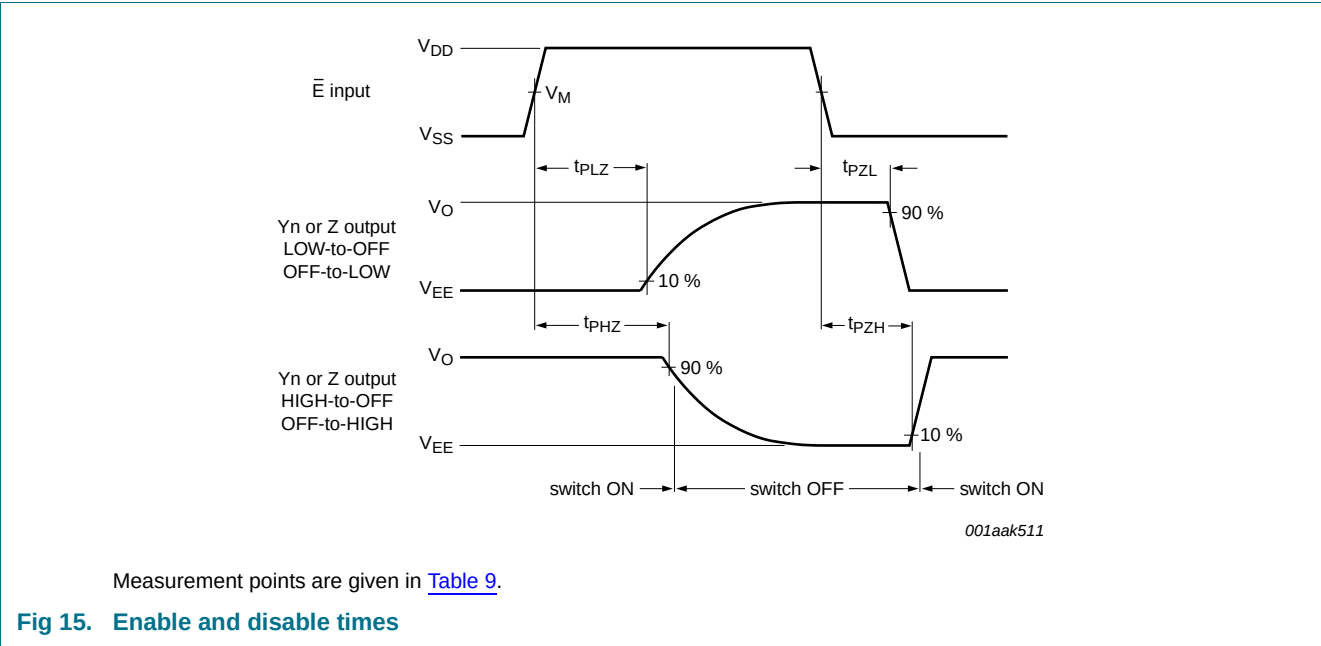
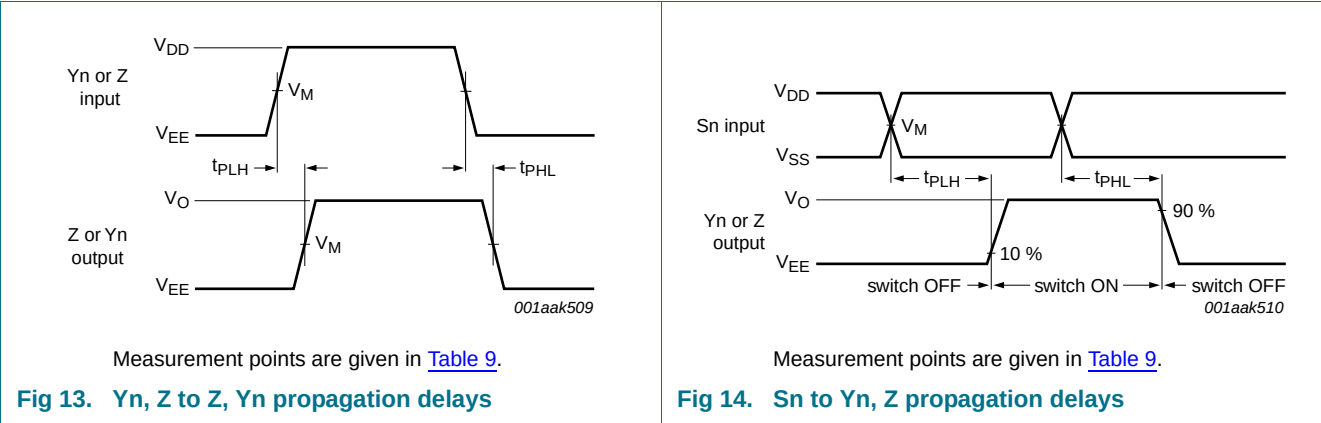
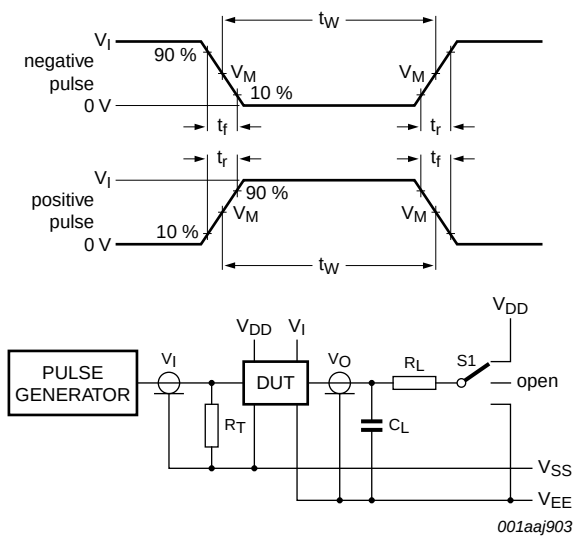


Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including test jig and probe.

R_L = Load resistance.

Fig 16. Test circuit for measuring switching times

Table 10. Test data

Input				Load		S1 position				
Yn, Z	Sn and $\bar{E}$	t_r, t_f	V_M	C_L	R_L	t_{PHL} ^[1]	t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	other
V_{DD} or V_{EE}	V_{DD} or V_{SS}	≤ 20 ns	$0.5V_{DD}$	50 pF	10 k Ω	V_{DD} or V_{EE}	V_{EE}	V_{EE}	V_{DD}	V_{EE}

[1] For Yn to Z or Z to Yn propagation delays use V_{EE} . For Sn to Yn or Z propagation delays use V_{DD} .

11.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

$V_{SS} = V_{EE} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
THD	total harmonic distortion	see Figure 17 ; $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; channel ON; $V_I = 0.5V_{DD}$ (p-p); $f_i = 1\text{ kHz}$	5 V	[1]	0.25	- %
			10 V	[1]	0.04	- %
			15 V	[1]	0.04	- %
$f_{(-3\text{dB})}$	-3 dB frequency response	see Figure 18 ; $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel ON; $V_I = 0.5V_{DD}$ (p-p)	5 V	[1]	13	- MHz
			10 V	[1]	40	- MHz
			15 V	[1]	70	- MHz
α_{iso}	isolation (OFF-state)	see Figure 19 ; $f_i = 1\text{ MHz}$; $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel OFF; $V_I = 0.5V_{DD}$ (p-p)	10 V	[1]	-50	- dB
V_{ct}	crosstalk voltage	digital inputs to switch; see Figure 20 ; $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; E or Sn = V_{DD} (square-wave)	10 V		50	- mV
Xtalk	crosstalk	between switches; see Figure 21 ; $f_i = 1\text{ MHz}$; $R_L = 1\text{ k}\Omega$; $V_I = 0.5V_{DD}$ (p-p)	10 V	[1]	-50	- dB

[1] f_i is biased at $0.5 V_{DD}$; $V_I = 0.5V_{DD}$ (p-p).

Table 12. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown; $V_{EE} = V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 5500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.2.1 Test circuits

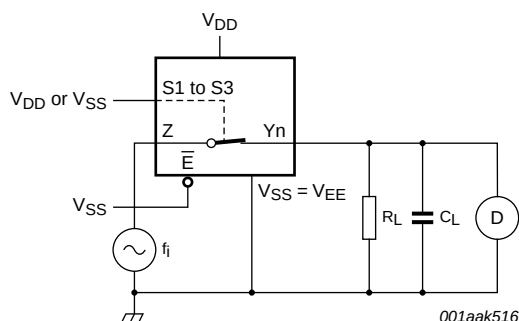


Fig 17. Test circuit for measuring total harmonic distortion

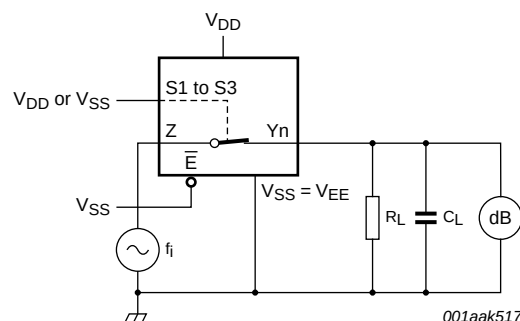


Fig 18. Test circuit for measuring frequency response

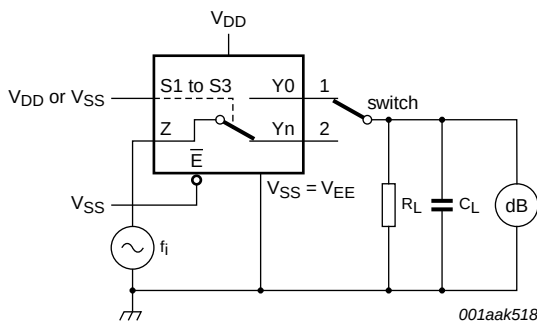
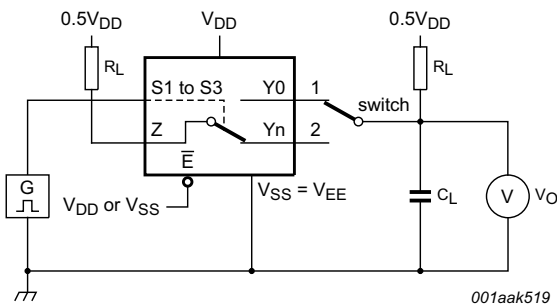
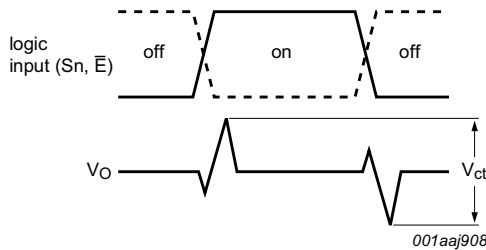


Fig 19. Test circuit for measuring isolation (OFF-state)

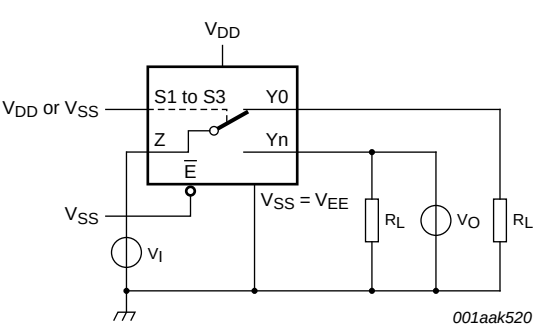


a. Test circuit

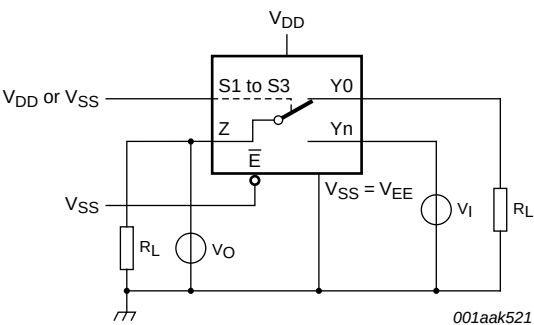


b. Input and output pulse definitions

Fig 20. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition



b. Switch open condition

Fig 21. Test circuit for measuring crosstalk between switches

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

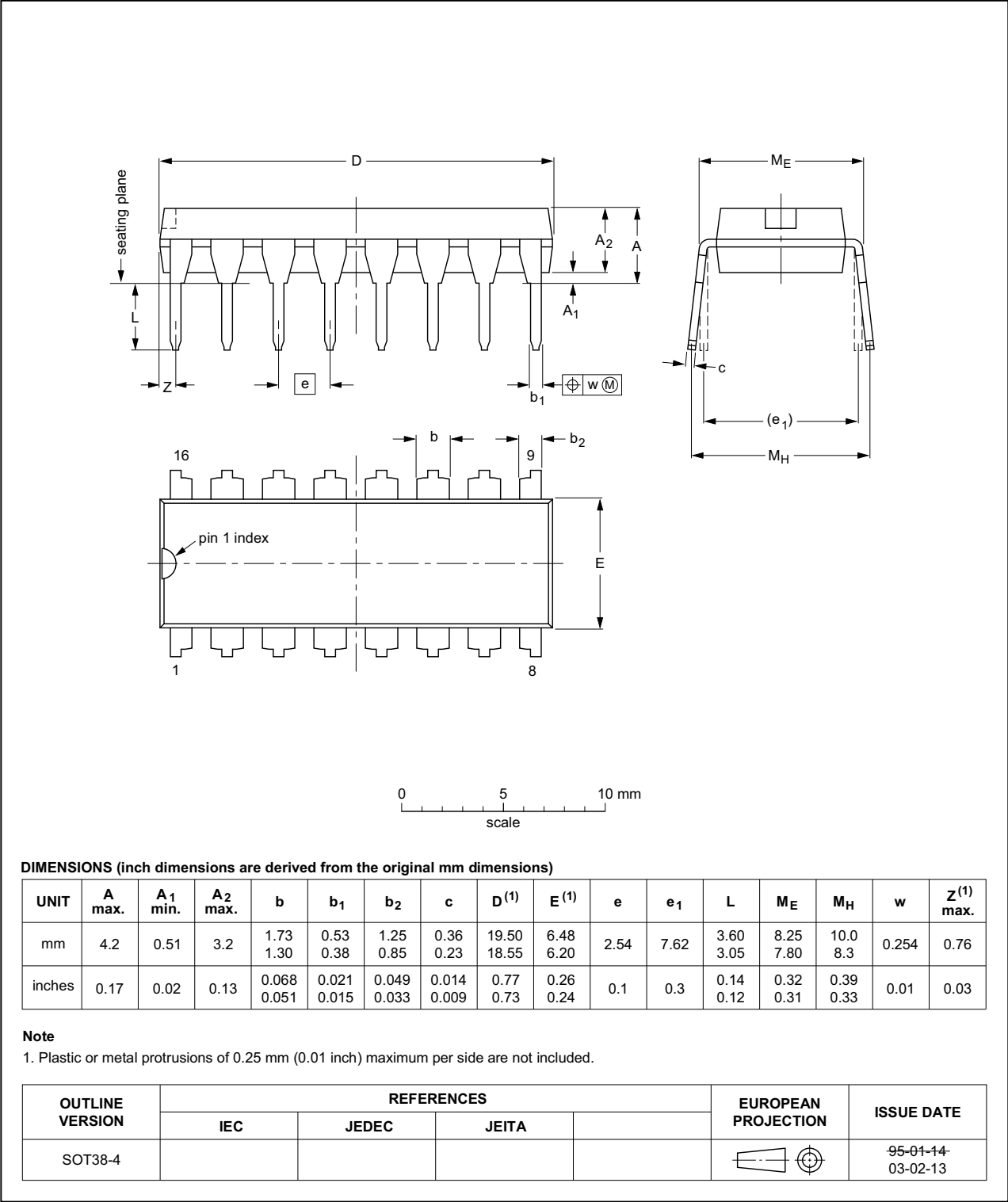
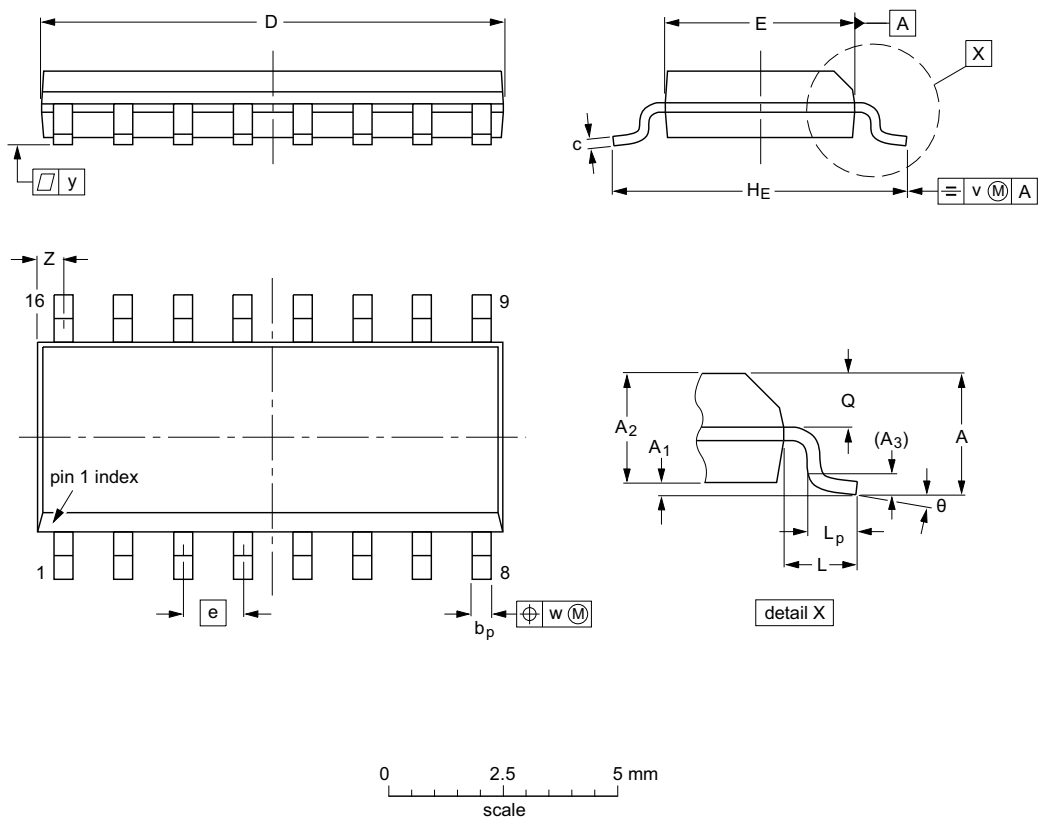


Fig 22. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 23. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

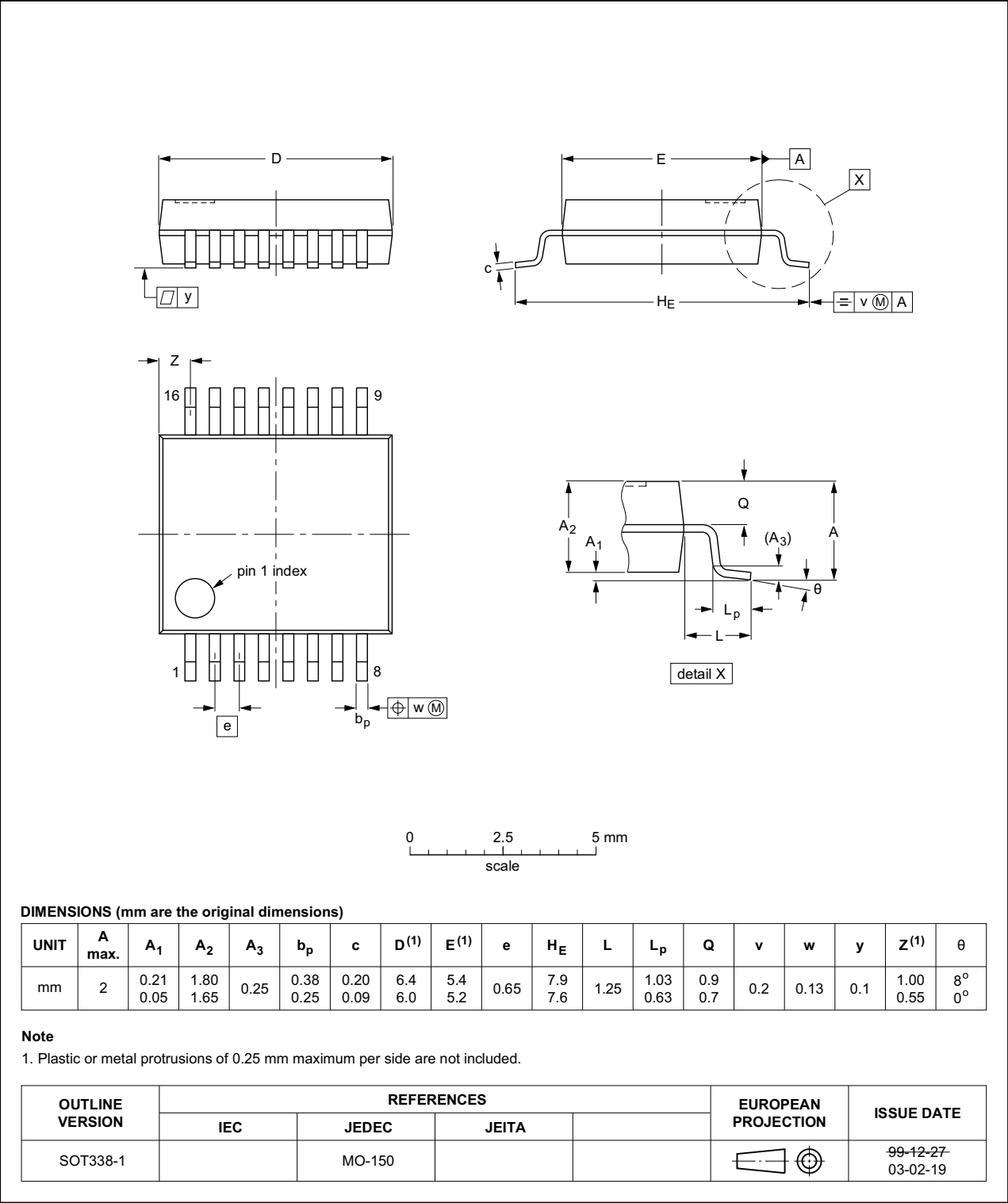


Fig 24. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

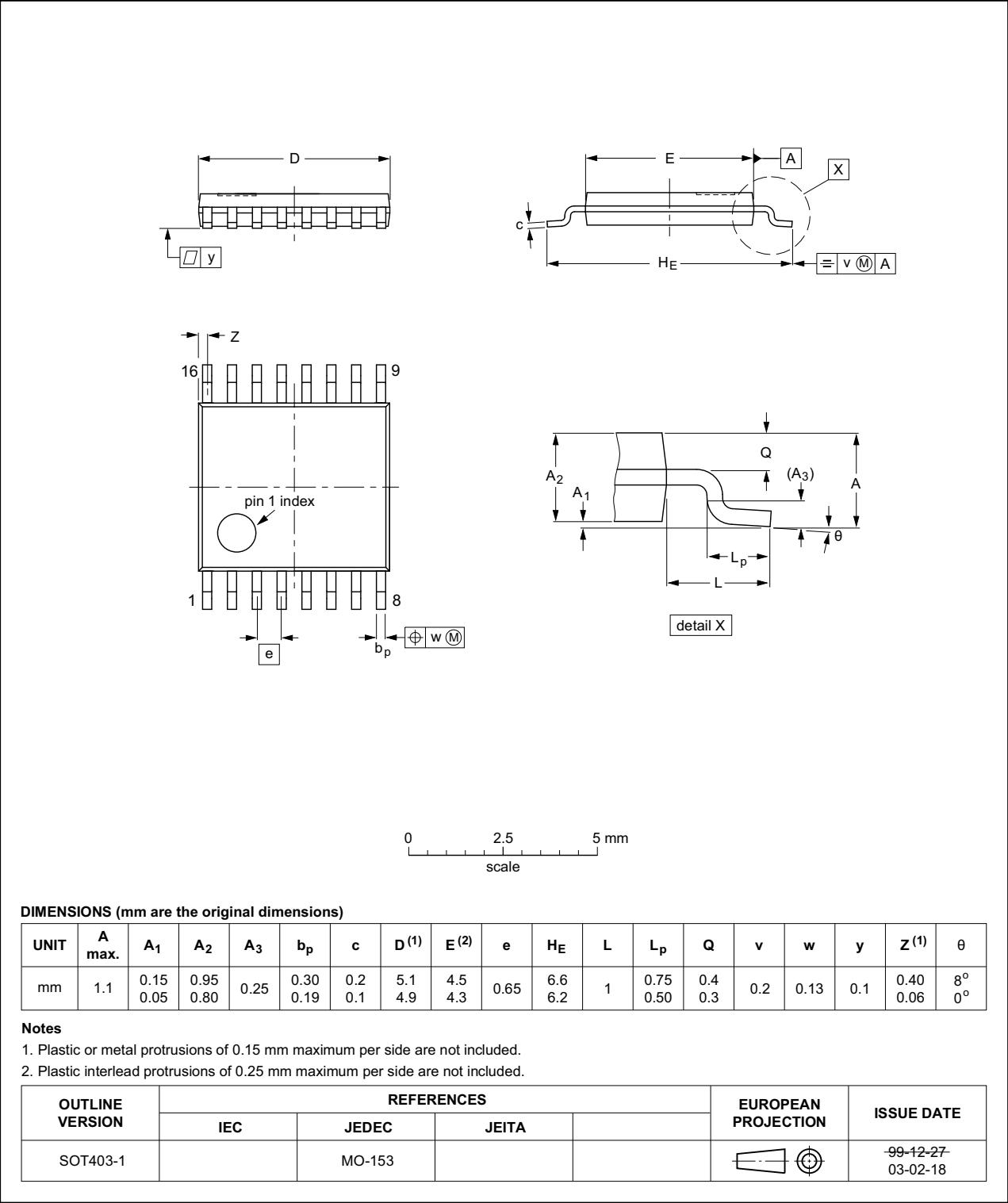


Fig 25. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
DUT	Device Under Test

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4051B v.11	20140911	Product data sheet	-	HEF4051B v.10
Modifications:	• Figure 20: Test circuit modified			
HEF4051B v.10	20111117	Product data sheet	-	HEF4051B v.9
Modifications:	• Legal pages updated. • Changes in “General description”, “Features and benefits” and “Applications”.			
HEF4051B v.9	20100325	Product data sheet	-	HEF4051B v.8
HEF4051B v.8	20100301	Product data sheet	-	HEF4051B v.7
HEF4051B v.7	20091127	Product data sheet	-	HEF4051B v.6
HEF4051B v.6	20090924	Product data sheet	-	HEF4051B v.5
HEF4051B v.5	20090826	Product data sheet	-	HEF4051B v.4
HEF4051B v.4	20050112	Product data sheet	-	HEF4051B_CNV v.3
HEF4051B_CNV v.3	19950101	Product specification	-	HEF4051B_CNV v.2
HEF4051B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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