

SN54HCT74, SN74HCT74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCLS169B – DECEMBER 1982 – REVISED MAY 1997

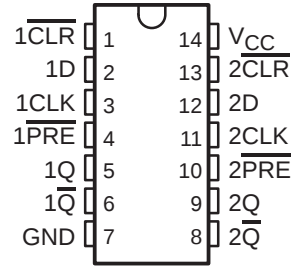
- Inputs Are TTL-Voltage Compatible
- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

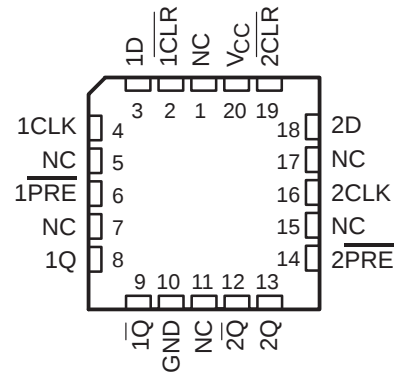
The 'HCT74 contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HCT74 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT74 is characterized for operation from -40°C to 85°C .

SN54HCT74 . . . J OR W PACKAGE
SN74HCT74 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	$\text{H}^{\dagger}$	$\text{H}^{\dagger}$
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	Q_0	Q_0

$\dagger$ This configuration is unstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SCLS169B – DECEMBER 1982 – REVISED MAY 1997

Timing diagram for the 74VHC163 4-bit binary counter. The diagram shows two clock inputs (1CLK, 2CLK), two data inputs (1D, 2D), two clear inputs (1CLR, 2CLR), and two preset inputs (1PRE, 2PRE). The outputs are 1Q, 1Q-bar, 2Q, and 2Q-bar. The counter is shown in a block with internal labels S, C1, 1D, and R. The timing shows that the counter increments on the rising edge of the clock inputs, and the clear inputs (1CLR, 2CLR) asynchronously reset the counter to 0. The preset inputs (1PRE, 2PRE) asynchronously set the counter to a specific value.

The logic diagram shows a 4-bit counter implemented with four T flip-flops (labeled 'TG') and various combinational logic gates. The inputs are PRE (preset), CLK (clock), D (data), and CLR (clear). The outputs are Q and $\overline{Q}$. The circuit uses a combination of inverters, AND gates, OR gates, and XOR gates to generate the clock and data signals for each flip-flop. The first flip-flop's clock is derived from the CLK input through a series of inverters. The data input D is connected to the first flip-flop's data input. The output of the first flip-flop is connected to the clock input of the second flip-flop. The output of the second flip-flop is connected to the clock input of the third flip-flop. The output of the third flip-flop is connected to the clock input of the fourth flip-flop. The output of the fourth flip-flop is connected to the clock input of the first flip-flop, forming a closed loop. The output of the first flip-flop is also connected to the data input of the second flip-flop. The output of the second flip-flop is connected to the data input of the third flip-flop. The output of the third flip-flop is connected to the data input of the fourth flip-flop. The output of the fourth flip-flop is connected to the data input of the first flip-flop, forming a closed loop. The output of the first flip-flop is also connected to the data input of the second flip-flop. The output of the second flip-flop is connected to the data input of the third flip-flop. The output of the third flip-flop is connected to the data input of the fourth flip-flop. The output of the fourth flip-flop is connected to the data input of the first flip-flop, forming a closed loop.

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	127°C/W
N package	78°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SN54HCT74, SN74HCT74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH CLEAR AND PRESET

SCLS169B – DECEMBER 1982 – REVISED MAY 1997

recommended operating conditions

			SN54HCT74			SN74HCT74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) time		0		500	0		500	ns
T _A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I _{OH} = –4 mA		3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA			0.17	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		5.5 V	±0.1	±100		±1000		±1000		nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		5.5 V			4		80		40	µA
ΔI _{CC} [†]	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}		5.5 V		1.4	2.4		3		2.9	mA
C _i			4.5 V to 5.5 V		3	10		10		10	pF

[†] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC}	T _A = 25°C		SN54HCT74		SN74HCT74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		4.5 V	0	27	0	18	0	22	MHz
			5.5 V	0	30	0	20	0	24	
t _w	Pulse duration	PRE or CLR low	4.5 V	16		24		20		ns
			5.5 V	14		21		18		
	CLK high or low		4.5 V	18		27		23		
			5.5 V	16		24		21		
t _{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	11		16		14		
	PRE or CLR inactive		4.5 V	0		0		0		
			5.5 V	0		0		0		
t _h	Hold time, data after CLK↑		4.5 V	0		0		0		ns
			5.5 V	0		0		0		

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54HCT74, SN74HCT74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

SCLS169B – DECEMBER 1982 – REVISED MAY 1997

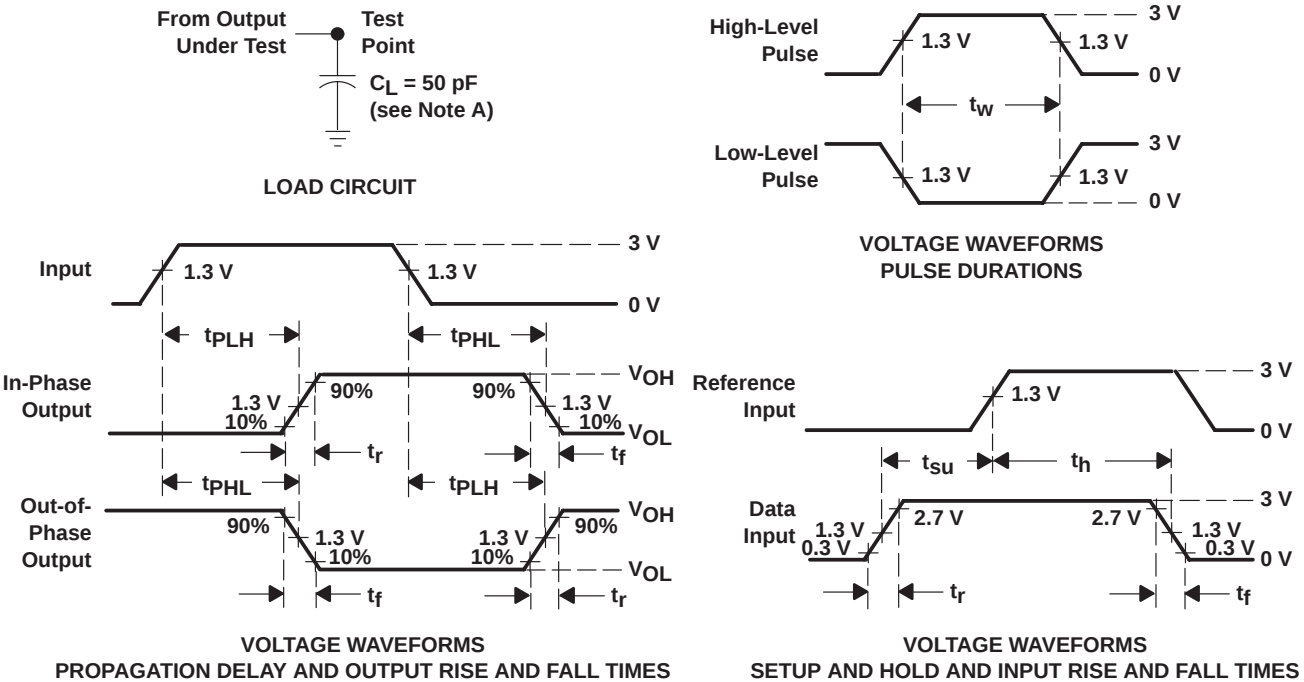
switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	27	40		18		22		MHz
			5.5 V	30	46		20		24		
t_{pd}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	4.5 V		21	35		53		44	ns
			5.5 V		17	31		48		40	
	CLK	Q or $\overline{Q}$	4.5 V		20	28		42		35	
			5.5 V		18	25		38		31	
t_t		Q or $\overline{Q}$	4.5 V		8	15		22		19	ns
			5.5 V		7	14		20		17	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.