30-V, N-Channel NexFET™ Power MOSFET

Check for Samples: CSD17483F4

FEATURES

- **Low On Resistance**
- **Low Q_g and Q_{gd}**
- **Low Threshold Voltage**
- **Ultra Small Footprint (0402 Case Size)**
  - **1.0 mm x 0.6 mm**
- **Ultra Low Profile**
  - **0.35 mm Height**
- **Integrated ESD Protection Diode**
  - **Rated > 4kV HBM**
  - **Rated > 2kV CDM**
- **Pb and Halogen Free**
- **RoHS Compliant**

APPLICATIONS

- **Optimized for Load Switch Applications**
- **Optimized for General Purpose Switching Applications**
- **Single Cell Battery Applications**
- **Handheld and Mobile Applications**

DESCRIPTION

The FemtoFET™ MOSFET technology has been designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	1010		pC
Q_{gd}	Gate Charge Gate to Drain	130		pC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 1.8V	370	mΩ
		V_{GS} = 2.5V	240	
		V_{GS} = 4.5V	200	
$V_{GS(th)}$	Threshold Voltage	0.85		V

ORDERING INFORMATION

Device	Qty	Media	Package	Ship
CSD17483F4	3,000	7-Inch Reel	Femto(0402) 1.0mm x 0.6mm SMD Lead Less	Tape and Reel
CSD17483F4R	18,000	13-Inch Reel		

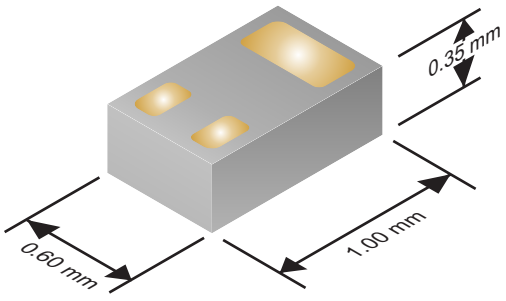
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	12	V
I_D	Continuous Drain Current, T_A = 25°C(1)	1.5	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	5	A
P_D	Power Dissipation(1)	500	mW
ESD Rating	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 7.4A, L = 0.1mH, R_G = 25Ω	2.7	mJ

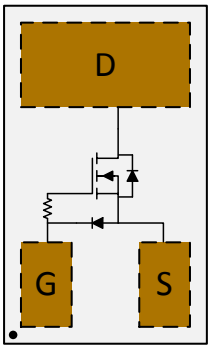
(1) Typical $R_{\theta JA}$ = 90°C/W on 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300µs, duty cycle ≤2%

Typical Part Dimensions



Top View



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = 250µA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 10V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250µA	0.65	0.85	1.10	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 1.8V, I_{DS} =0.5A		370	550	mΩ
		V_{GS} = 2.5V, I_{DS} =0.5A		240	310	mΩ
		V_{GS} = 4.5V, I_{DS} = 0.5A		200	260	mΩ
		V_{GS} = 8V, I_{DS} =0.5A		185	240	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_{DS} = 0.5A		2.4		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		145	190	pF
C_{oss}	Output Capacitance			42	55	pF
C_{rss}	Reverse Transfer Capacitance			2	3	pF
R_G	Series Gate Resistance			23		Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_{DS} = 0.5A		1010	1300	pC
Q_{gd}	Gate Charge Gate to Drain			130		pC
Q_{gs}	Gate Charge Gate to Source			220		pC
$Q_{g(th)}$	Gate Charge at Vth			145		pC
Q_{oss}	Output Charge	V_{DS} = 15V, V_{GS} = 0V		1095		pC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 0V, V_{GS} = 4.5V, I_{DS} = 0.5A,R_G = 2Ω		3.3		ns
t_r	Rise Time			1.3		ns
$t_{d(off)}$	Turn Off Delay Time			10.6		ns
t_f	Fall Time			3.4		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 0.5A, V_{GS} = 0V		0.73	0.9	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 15V, I_F = 0.5A, di/dt = 300A/µs		1475		pC
t_{rr}	Reverse Recovery Time			5.5		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		Typical Values	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)	90	°C/W
	Thermal Resistance Junction to Ambient(2)	250	°C/W

(1) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

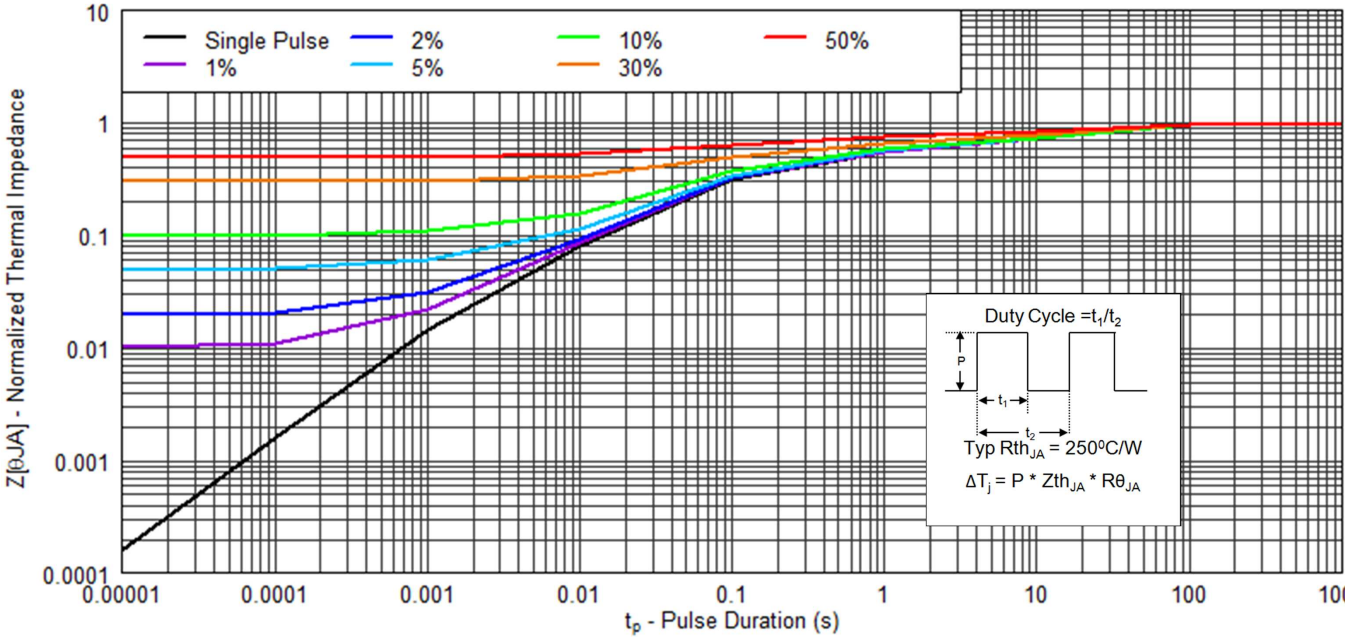


Figure 1. Transient Thermal Impedance

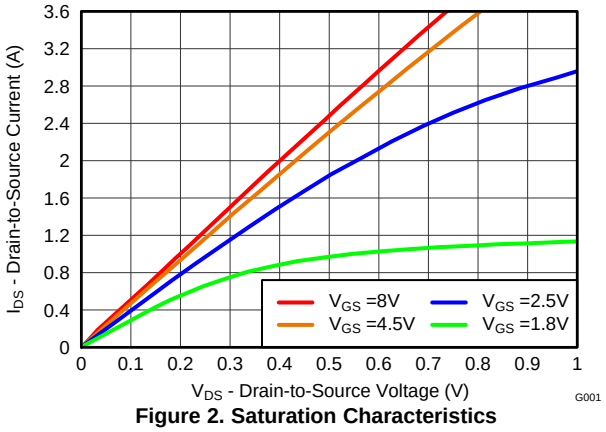


Figure 2. Saturation Characteristics

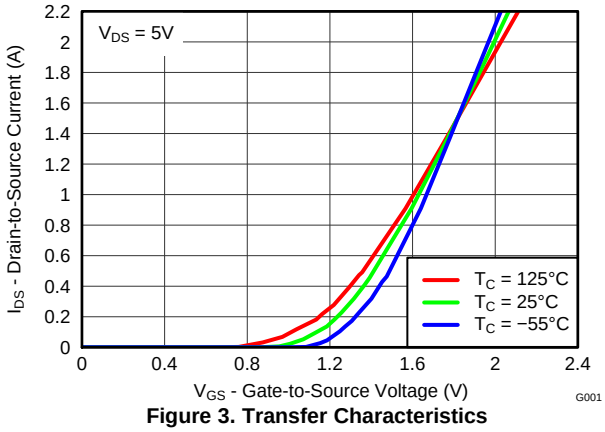


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

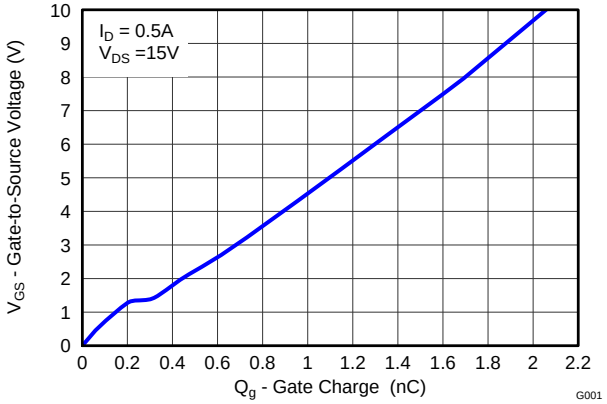


Figure 4. Gate Charge

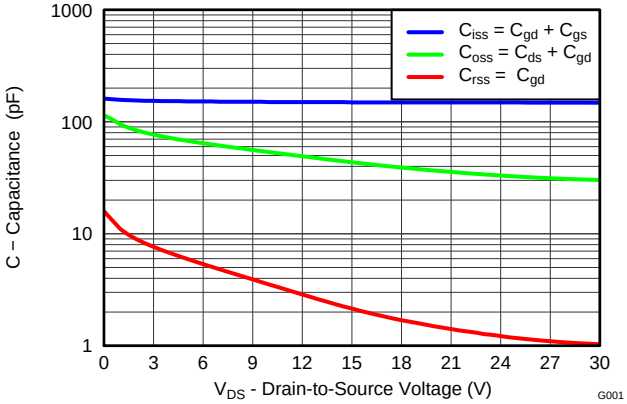


Figure 5. Capacitance

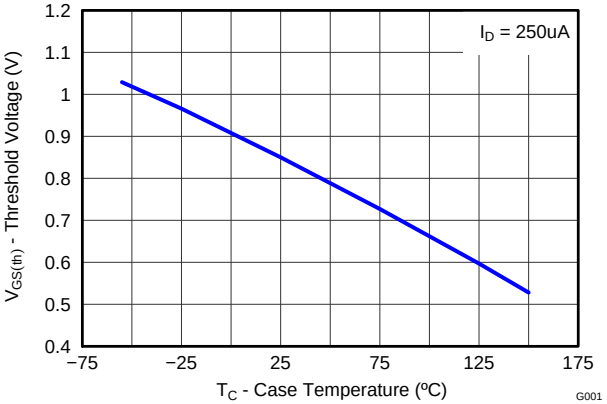


Figure 6. Threshold Voltage vs. Temperature

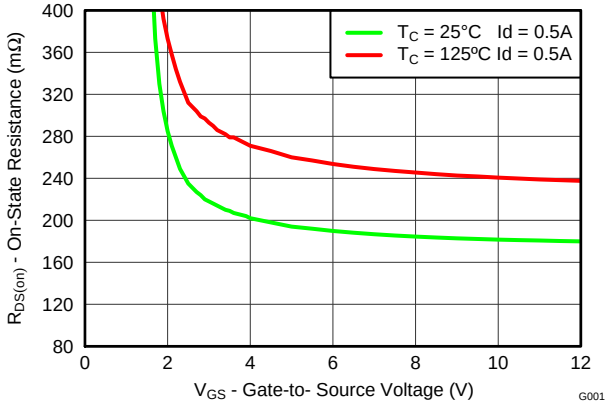


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

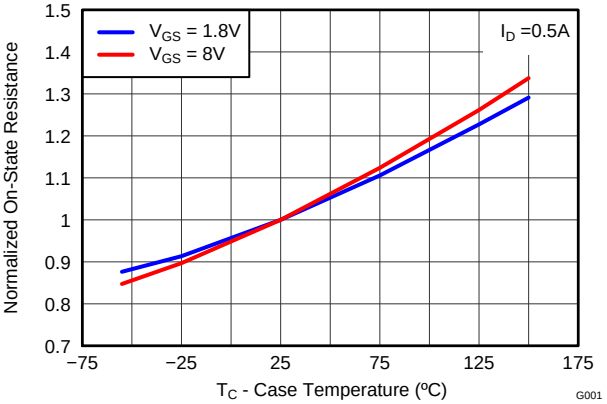


Figure 8. Normalized On-State Resistance vs. Temperature

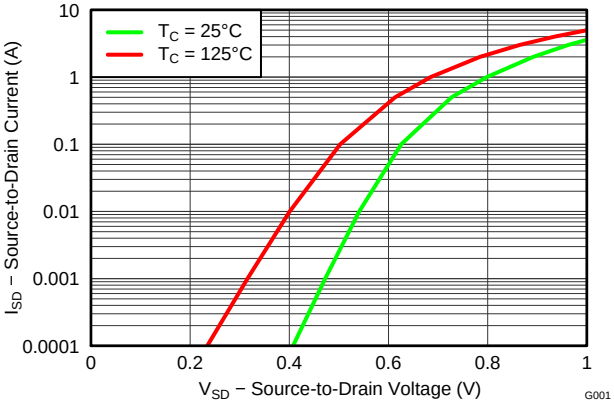


Figure 9. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

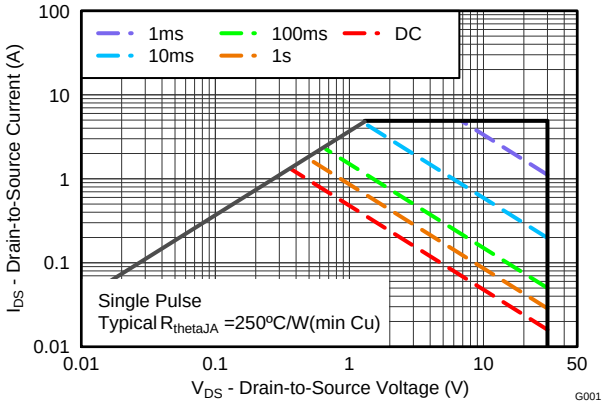


Figure 10. Maximum Safe Operating Area

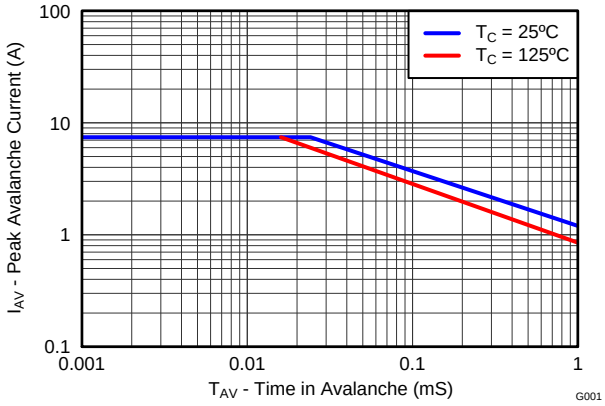


Figure 11. Single Pulse Unclamped Inductive Switching

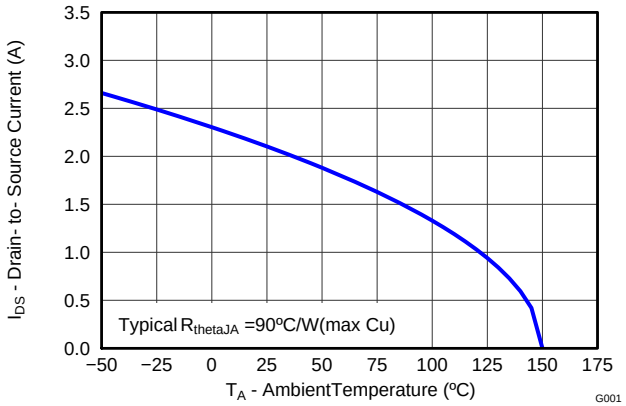
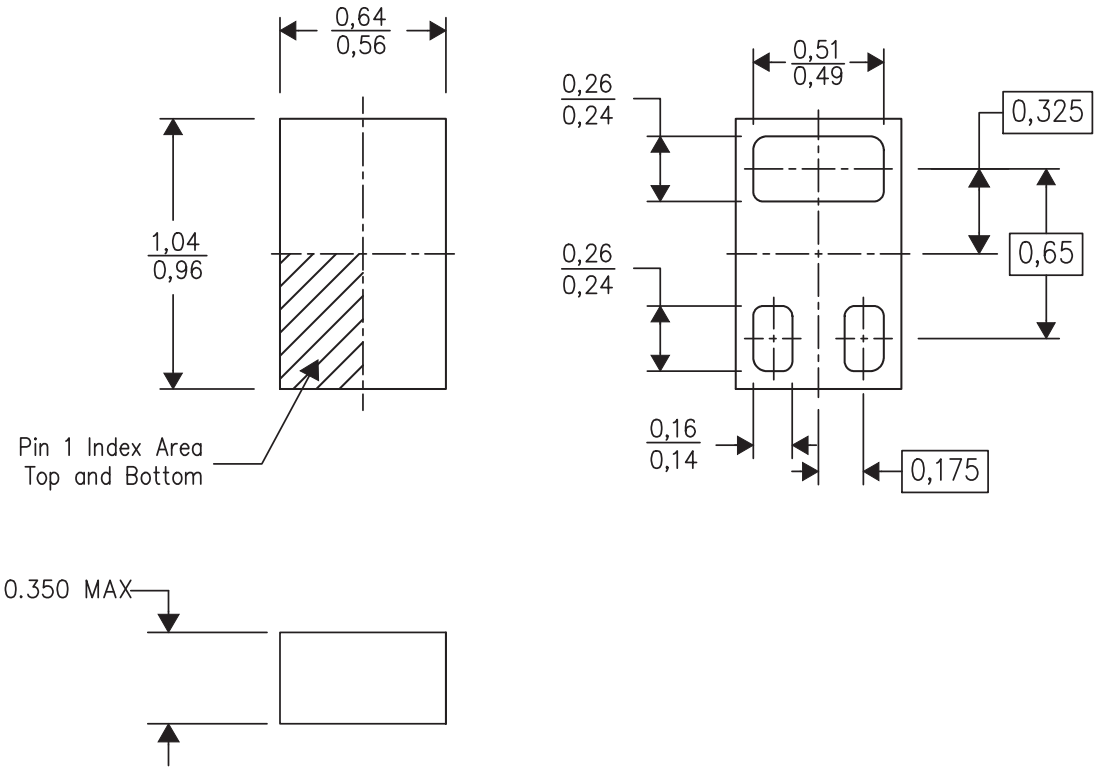


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

0402 Mechanical Dimensions

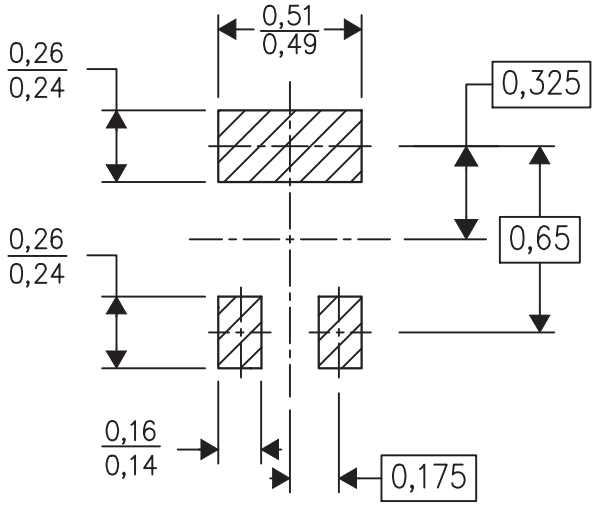


(1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994)

(2) This drawing is subject to change without notice

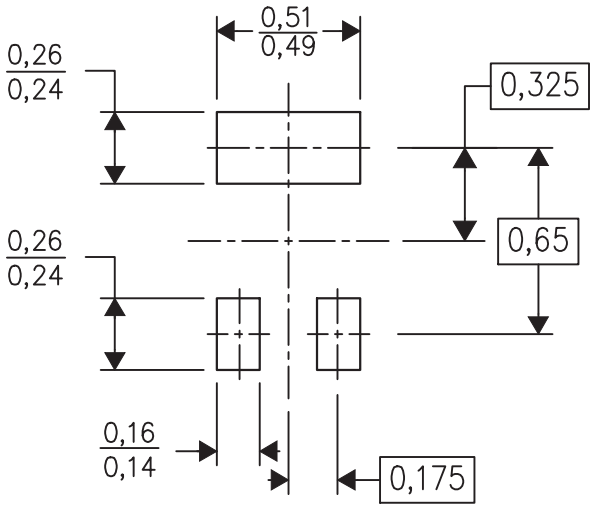
(3) This package is a PB-Free solder land design

Recommended Minimum PCB Layout



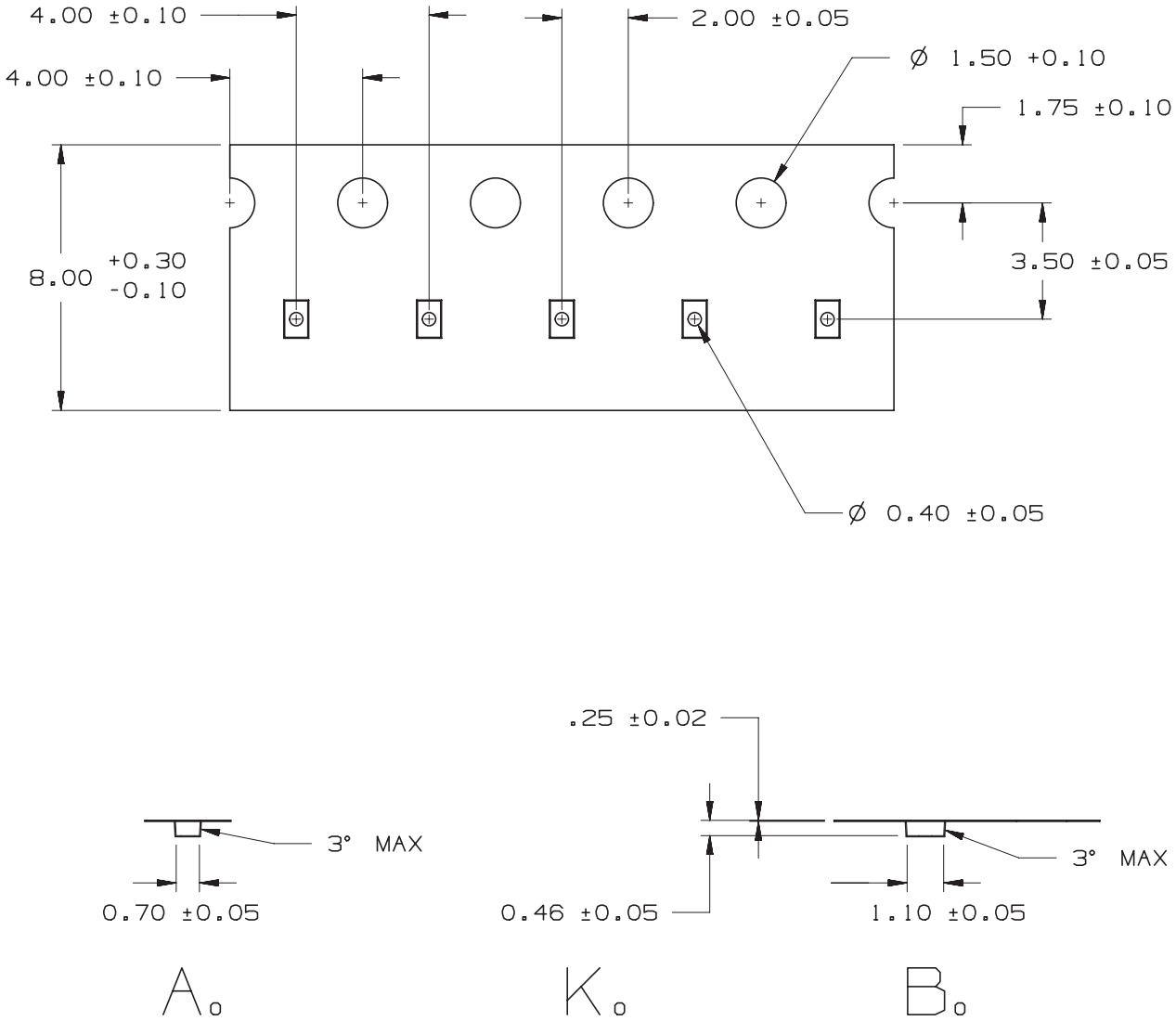
(1) All dimensions are in millimeters.

Recommended Stencil Pattern



(1) All dimensions are in millimeters.

CSD17483F4 Embossed Carrier Tape Dimensions



(1) Pin 1 will be oriented in the top right quadrant of the tape enclosure (Quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17483F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-250C-UNLIM	-55 to 150	DP	Samples
CSD17483F4R	PREVIEW	PICOSTAR	YJC	3	18000	TBD	Call TI	Call TI	-55 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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