

TPS61175EVM-326

This user's guide describes the characteristics, operation, and use of the TPS61175EVM-326 evaluation module (EVM). This EVM contains the Texas Instruments TPS61175 high-efficiency boost converter that is configured to provide a regulated 24-V output voltage from an input voltage ranging from 5.0 V to 12 V. This user's guide includes a schematic diagram, board layout, bill of materials and test data.

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1 Introduction

This section contains background information for the TPS61175EVM-326 evaluation module.

1.1 Background

This TPS61175EVM-326 is designed to boost 5.0 V to 12.0 V input voltages to a 24-V output. The goal of the EVM is to facilitate evaluation of the TPS61175 power supply solution. The EVM uses the TPS61175 adjustable output boost converter, external schottky diode, input and output capacitors, inductor, and the appropriate feedback and compensation components to provide a regulated 24V.

1.2 Performance Specification Summary

Table 1 provides a summary of the TPS61175EVM-326 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary for $V_{IN} = 5.0\text{ V}$

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage			5		V
$I_{IN(AVG)}$	Average input current	$I_O = 450\text{ mA}$			2.6	A
f_{SW}	Switching frequency			750		kHz
OUTPUT CHARACTERISTICS						
V_O	Output voltage		23 ⁽¹⁾	24	25 ⁽¹⁾	V
	Line regulation	$4.5\text{ V} < V_{IN} < 5.5\text{ V}$ at $I_O = 400\text{ mA}$			1%	$\Delta V_O / \Delta V_{IN}$
	Load regulation	$V_{IN} = 5\text{ V}$, $1\text{ mA} < I_O < 450\text{ mA}$			1%	$\Delta V_O / \Delta I_O$
$\Delta V_{O(PP)}$	Output voltage ripple	$I_O = 450\text{ mA}$			75	mV _{PP}
I_O	Output current		1		450	mA
TRANSIENT RESPONSE						
ΔI_O	Load step			0.35		A
$\Delta I_O / \Delta T$	Load slew rate			9		A/ μs
ΔV_O	V_O undershoot			1.1		V
t_S	Settling time			280		μs

⁽¹⁾ Minimum and maximum values include 1% resistor tolerance as well as IC feedback reference voltage tolerance.

Table 2. Performance Specification Summary for $V_{IN} = 12.0\text{ V}$

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input Voltage			12		V
$I_{IN(AVG)}$	Average Input Current				2.6	A
f_{SW}	Switching Frequency			750		kHz
OUTPUT CHARACTERISTICS						
V_O	Output Voltage		23 ⁽¹⁾	24	25 ⁽¹⁾	V
	Line Regulation	$11\text{ V} < V_{IN} < 13\text{ V}$ at $I_O = 1.1\text{ A}$			1%	$\Delta V_O / \Delta V_{IN}$
	Load Regulation	$V_{IN} = 12\text{ V}$, $1\text{ mA} < I_O < 1.2\text{ A}$			1%	$\Delta V_O / \Delta I_O$
$\Delta V_{O(PP)}$	Output Voltage Ripple	$I_O = 1.2\text{ A}$			250	mV _{PP}
I_O	Output Current		1		1.2	A
TRANSIENT RESPONSE						
ΔI_{TRAN}	Load Step			0.35		A
$\Delta I_O / \Delta T$	Load slew rate			9		A/ μs
ΔV_{TRAN}	V_O undershoot			480		mV
t_S	Settling time			300		μs

⁽¹⁾ Minimum and maximum values include 1% resistor tolerance as well as IC feedback reference voltage tolerance.

1.3 Design Example

The following example illustrates the design process and component selection for a 12-V to 24-V non-synchronous boost regulator using the TPS61175 converter.

1. Determining the duty cycle.

$$D_{(MIN)} = \frac{V_{OUT} + V_D - V_{IN(MIN)}}{V_{OUT} + V_D} = \frac{24\text{ V} + 0.5\text{ V} - 12\text{ V}}{24\text{ V} + 0.5\text{ V}} = 51\% \quad (1)$$

2. Computing the maximum output current.

Assuming $\eta_{\text{est}} = 90\%$ at $V_{\text{IN}} = 12\text{ V}$ and $\text{RPL}\% = 20\%$, datasheet equation 6 gives

$$I_{\text{OUT(max)}} = \frac{V_{\text{IN}} \times I_{\text{LIM}} \times (1 - \text{RPL}\%/2) \times \eta_{\text{est}}}{V_{\text{OUT}}} = \frac{12\text{ V} \times 3\text{ A} \times (1 - 20\%/2) \times 90\%}{24} = 1.2\text{ A} \quad (2)$$

3. Selecting the inductor.

The designer chose $\text{RPL}\% = 20\%$ and $f_{\text{SW}} = 750\text{ kHz}$ and assumed $\eta_{\text{est}} = 90\%$ for use in datasheet equation 5.

$$L \geq \frac{\eta_{\text{est}} \times V_{\text{IN}}}{\left[f_{\text{SW}} \times \left(\frac{1}{V_{\text{OUT}} + V_{\text{D}} - V_{\text{IN}}} + \frac{1}{V_{\text{IN}}} \right) \right] \times \text{RPL}\% \times P_{\text{OUT}}} \\ = \frac{90\% \times 12\text{ V}}{750\text{ kHz} \times \left(\frac{1}{24\text{ V} + 0.5\text{ V} - 12\text{ V}} + \frac{1}{12\text{ V}} \right) \times 20\% \times 1.2\text{ A} \times 24\text{ V}} = 15.3\text{ }\mu\text{H} \rightarrow 22\text{ }\mu\text{H} \quad (3)$$

4. Setting the output voltage.

Selecting $R_2 = 16.2\text{ k}\Omega$ gives

$$R_1 = R_2 \times \left(\frac{V_{\text{OUT}}}{1.229\text{ V}} - 1 \right) = 16.2\text{ k}\Omega \times \left(\frac{24}{1.229\text{ V}} - 1 \right) = 300\text{ k}\Omega \rightarrow 301\text{ k}\Omega \quad (4)$$

5. Setting the switching frequency

Using datasheet Table 1 and Figure 13 as well as some bench testing results, the designer selected a $143\text{ k}\Omega$ resistor to set the 750 kHz switching frequency.

6. Selecting the soft start capacitor

The designer selected the datasheet recommended value of $0.047\text{ }\mu\text{F}$.

7. Selecting the Schottky diode

The designer selected a 40-V rated diode to accommodate user modifications of higher output voltages to the power supply. With $1.2\text{ A} \times 0.45\text{ V} = 540\text{ mW}$ potential power dissipation and $T_{\text{Amax}} = 25^\circ\text{C}$, the designer choose the SMA package diode, which will experience a rise in junction temperature to $T_{\text{J}} = 25^\circ\text{C} + 81^\circ\text{C/W} \times 540\text{ mW} = 69^\circ\text{C}$. In a real application, a larger packaged diode is recommended.

8. Selecting the output capacitance:

The output capacitance needs to be the larger of

$$C_{\text{OUT}} = \frac{(V_{\text{OUT}} - V_{\text{IN}}) \times I_{\text{OUT}}}{V_{\text{OUT}} \times f_{\text{SW}} \times \Delta V_{\text{RIP}}} = \frac{(24\text{ V} - 12\text{ V}) \times 1.2\text{ A}}{24\text{ V} \times 750\text{ kHz} \times 300\text{ mV}} = 2.7\text{ }\mu\text{F} \quad (5)$$

to meet the ripple specification or

$$C_{\text{OUT}} = \frac{\Delta I_{\text{TRAN}}}{2 \times \pi \times f_{\text{LOOP-BW}} \times \Delta V_{\text{TRAN}}} = \frac{350\text{ mA}}{2 \times \pi \times 10\text{ kHz} \times 500\text{ mV}} = 11\text{ }\mu\text{F} \quad (6)$$

to meet the transient specification. The designer selected $3 \times 4.7\text{ }\mu\text{F}$, 50 V capacitors to give close to $15\text{ }\mu\text{F}$ of output capacitance.

9. Compensating the control loop.

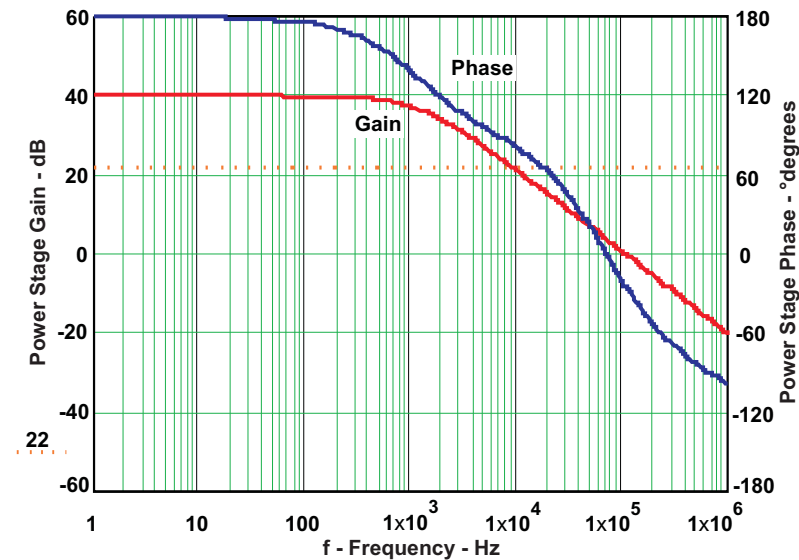
Using MathCAD to plot data sheet equation 10 with

$R_{\text{OUT}} = 24\text{ V}/1.2\text{ A} = 20\text{ }\Omega$, $R_{\text{SENSE}} = 40\text{ m}\Omega$

$$f_{\text{P}} = \frac{2}{2\pi \times R_{\text{O}} \times C_2} = \frac{2}{2\pi \times 20\text{ }\Omega \times 3 \times 4.7\text{ }\mu\text{F}} = 1.1\text{ kHz} \quad (7)$$

$$f_{\text{RHPZ}} = \frac{R_{\text{O}}}{2\pi \times L} \times \left(\frac{V_{\text{in}}}{V_{\text{out}}} \right)^2 = \frac{20\text{ }\Omega}{2\pi \times 22\text{ }\mu\text{H}} \times \left(\frac{12}{24} \right)^2 = 36.2\text{ kHz} \quad (8)$$

and neglecting the ESR zero produce by the ceramic output capacitors gives



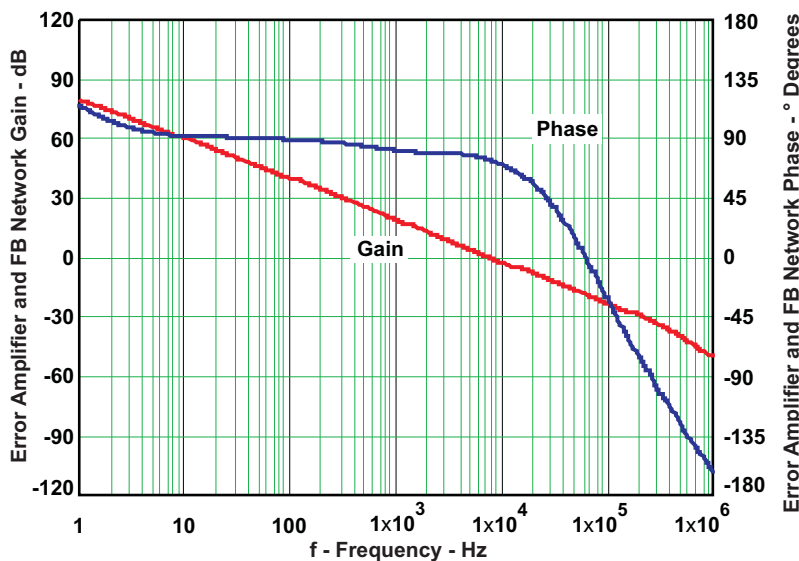
The designer chose $f_C = 10\text{kHz}$ which means $K_{COMP}(f_C) = -22\text{dB}$. With $R_1 = 16.2\text{k}$ and $R_2 = 301\text{k}$ $G_{EAmax} = 440\mu\text{mho}$, solving the equation on datasheet page 17 for R_3 gives

$$R_3 \cong \frac{10^{\frac{K_{COMP}(f_C)}{20\text{dB}}}}{G_{EA} \times \frac{R_2}{R_2+R_1}} = \frac{10^{\frac{-22\text{dB}}{20\text{dB}}}}{340\mu\text{mho} \times \frac{16.2\text{k}\Omega}{301\text{k}\Omega + 16.2\text{k}\Omega}} = 4.57\text{k}\Omega \rightarrow 4.53\text{k}\Omega \quad (9)$$

Solving datasheet equation 20 for C_4 and setting $f_Z \cong f_C/10 = 1\text{kHz}$ gives

$$C_4 \cong \frac{1}{2\pi \times R_3 \times f_Z} = \frac{1}{2\pi \times 4.57\text{k}\Omega \times 1\text{kHz}} = 35\text{nF} \rightarrow 33\text{nF} \quad (10)$$

The designer used bench measurements to set $R_3 = 3.09\text{k}\Omega$ in order to get closer to the desired 60 degrees phase margin. Using MathCAD to plot $T(s) = G_{PW}(s) \times H_{EA}(s)$ from the datasheet gives



1.4 Modifications

Because the primary goal of the EVM is to demonstrate the flexibility of the TPS61175 power supply solution, the selected capacitors and inductors are not optimized for either a 5-V or a 12-V to 24-V conversion.

The TPS61175 integrated circuit (IC) has a maximum input voltage of 18 V and can boost its input voltage up to 38 V. Changes to this EVM's recommended input and output voltage likely requires changing one or more of the following components: schottky diode, input or output capacitors, inductor, feedback resistors, or error amplifier compensation components. Consult the data sheet (link to datasheet **TBD**) and/or design tools for assistance in selecting these components for your application. Changing components could improve or degrade EVM performance.

2 Setup and Test Results

This section describes how to properly connect, set up, and use the TPS61175EVM-326.

2.1 Input/Output Connections

The connection points are described in the following paragraphs.

2.1.1 J1 - V_{IN}

This header is the positive connection to the input power supply used for lower ($< 1A$) input currents. Twist the leads to the input supply, and keep them as short as possible.

2.1.2 J2 - V_{OUT}

This header is the positive output for the device used for lower ($< 1A$) output currents. Connect the positive lead of the load and/or output multimeter to this point.

2.1.3 J3 - GND

This header is the return connection for the input power supply used for lower ($< 1A$) input currents.

2.1.4 J4 - GND

This header is the return connection for the load and/or output multimeter used for lower ($< 1A$) output currents.

2.1.5 J5 pin 1 - SYNC

This pin is available for the application of an external clock synchronization signal. Make sure that the frequency of the clock signal is within the range in [Table 1](#). This pin cannot be left floating so use a shorting jumper to short the SYNC pin to GND if not used.

2.1.6 J5 pin 2 - GND

This pin is the return connection for the external synchronization signal.

2.1.7 J6 pin 1 - V_{IN}

This is the positive connection for the input power supply used for higher ($> 1A$) input currents.

2.1.8 J6 pin 2 - GND

This is the return connection to the input power supply used for higher ($> 1A$) input currents. Twist the leads to the input supply, and keep them as short as possible.

2.1.9 J7 pin 1 - GND

This is the return connection for the load used for higher ($> 1A$) output currents.

2.1.10 J7 pin 2 - V_{OUT}

This is the positive connection for the load used for higher ($> 1A$) output currents.

2.1.11 JP1 - ENABLE

Installing this jumper ties the enable pin to either the input voltage (on) or ground (off). If left unconnected, the enable pin's internal pull down resistor disables the IC.

2.1.12 TP1 - SW Node

Test point for the switch node of the boost converter.

2.1.13 TP2 - Loop Response

Test point for control loop response measurements.

2.1.14 TP3 - Comp Pin

Test point for the compensation network.

2.1.15 TP4 & TP5 - Output Ripple

Test points for measuring the output ripple voltage.

2.2 Test Results

The following section shows the test results of the TPS61175EVM-326.

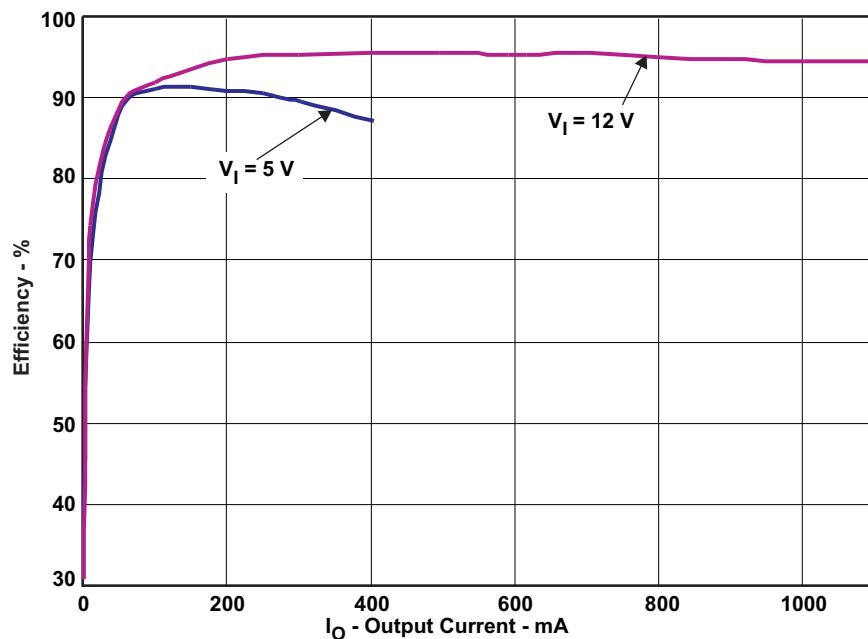


Figure 1. TPS61175EVM-326 Efficiency

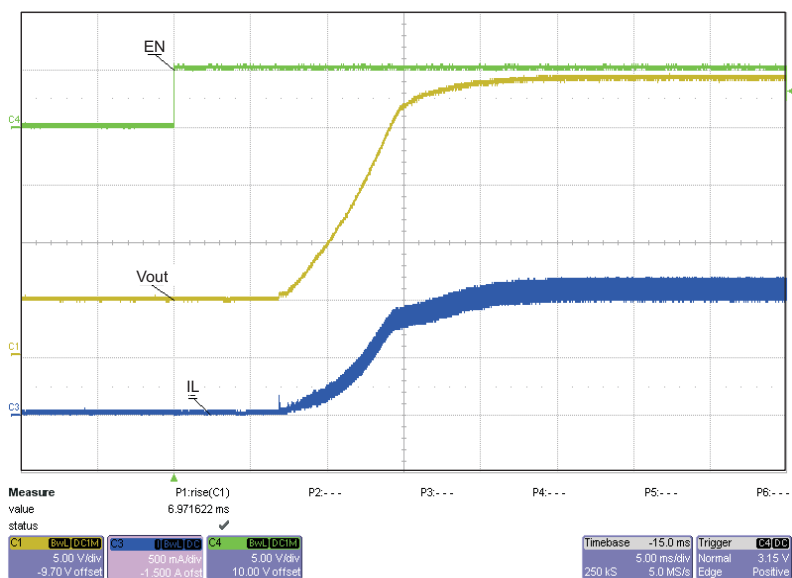


Figure 2. Start-Up With $V_{IN} = 5V$ and $I_{OUT} = 100\text{ mA}$

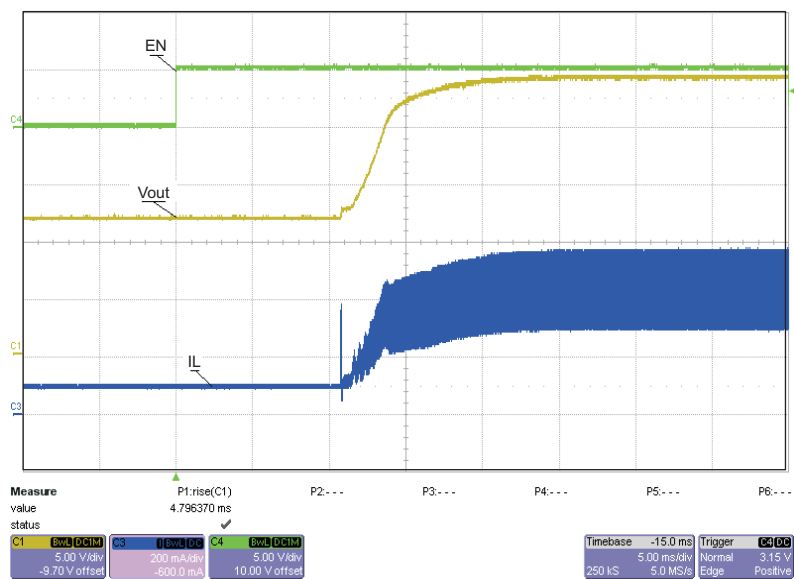


Figure 3. Start-Up With $V_{IN} = 12V$ and $I_{OUT} = 100\text{ mA}$

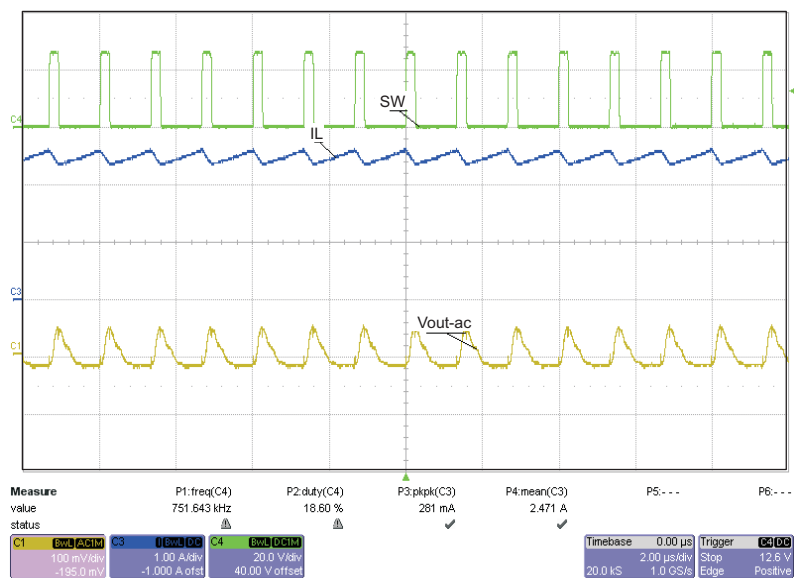


Figure 4. PWM Operation at 450 mA With $V_{IN} = 5V$

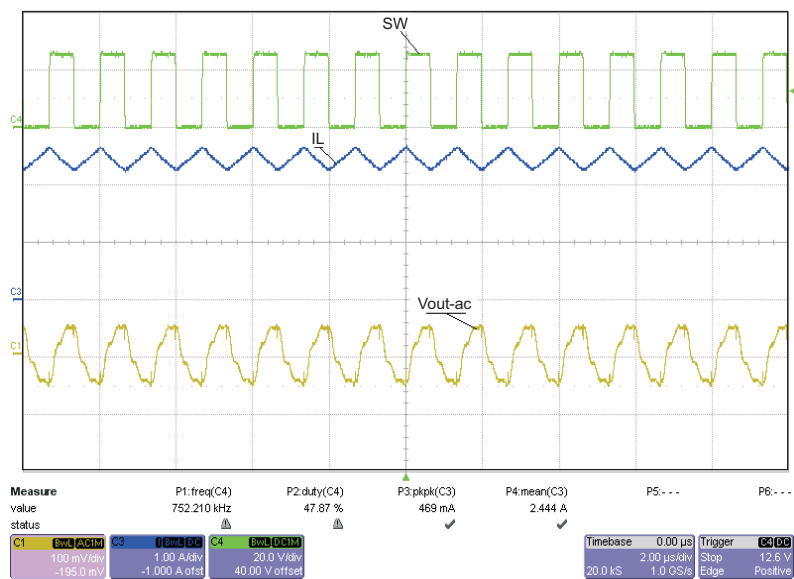


Figure 5. PWM Operation at 1.2 A With $V_{IN} = 12V$

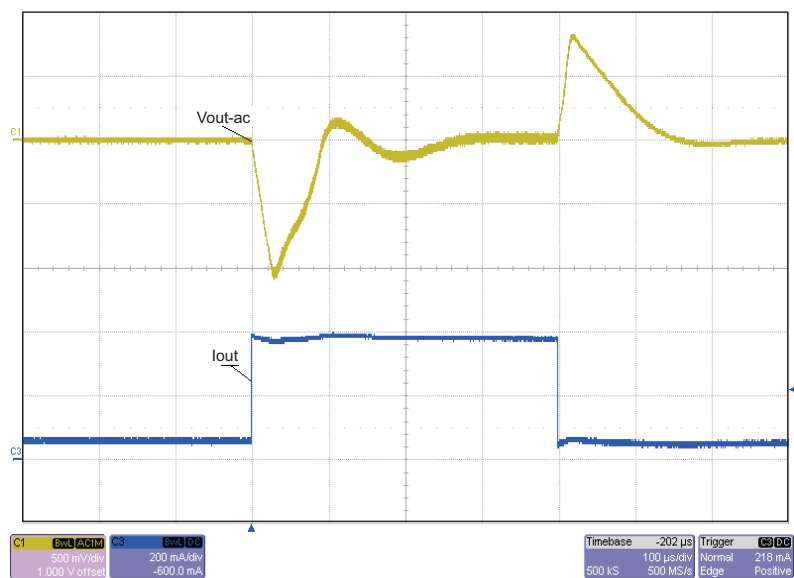


Figure 6. Load Transient Response From 45 mA to 400 mA With $V_{IN} = 5V$

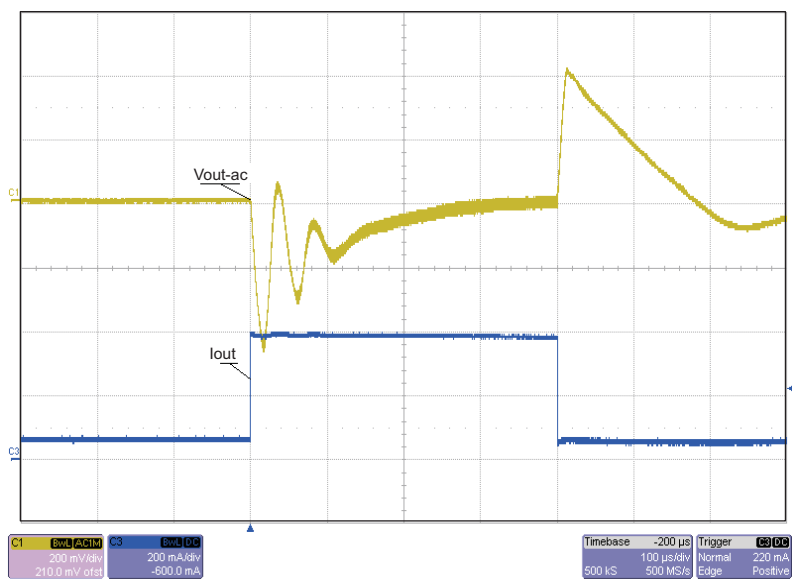


Figure 7. Load Transient Response From 45 mA to 400 mA With $V_{IN} = 12V$

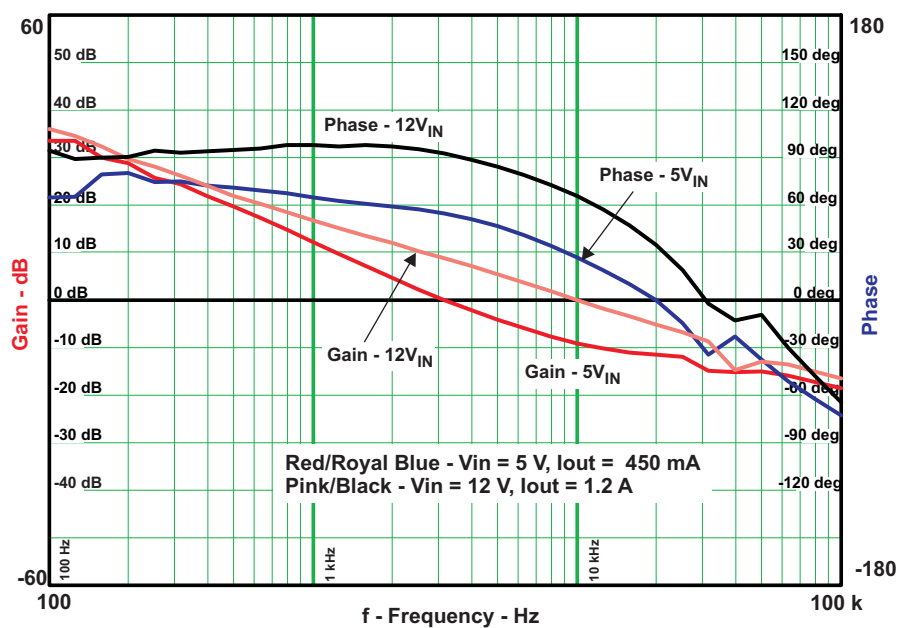


Figure 8. Loop Gain and Phase

3 Board Layout

This section provides the TPS61175EVM-326 board layout and illustrations.

3.1 Layout

Board layout is critical for all switch-mode power supplies. [Figure 9](#) through [Figure 13](#) show the board layout for the HPA326 printed-circuit board. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry. Careful attention has been given to the routing of high-frequency current loops. See the data sheet ([SLVS892](#)) for further layout recommendations.

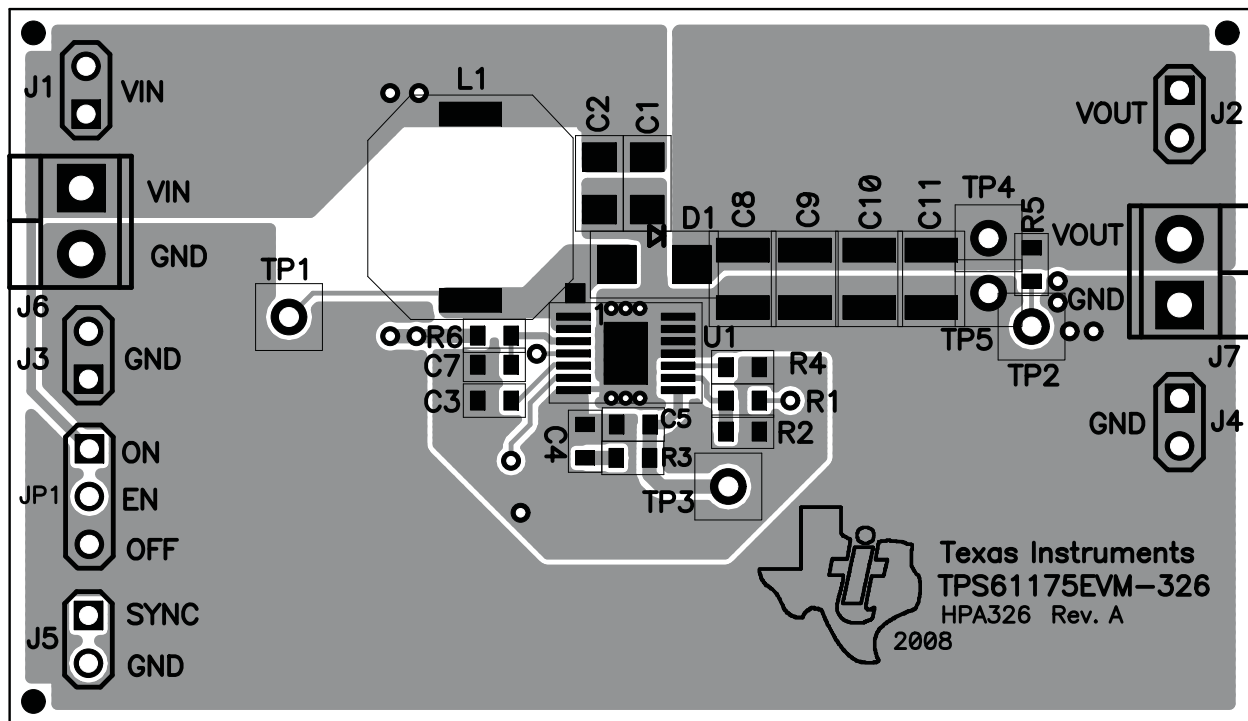


Figure 9. Top Assembly Layer

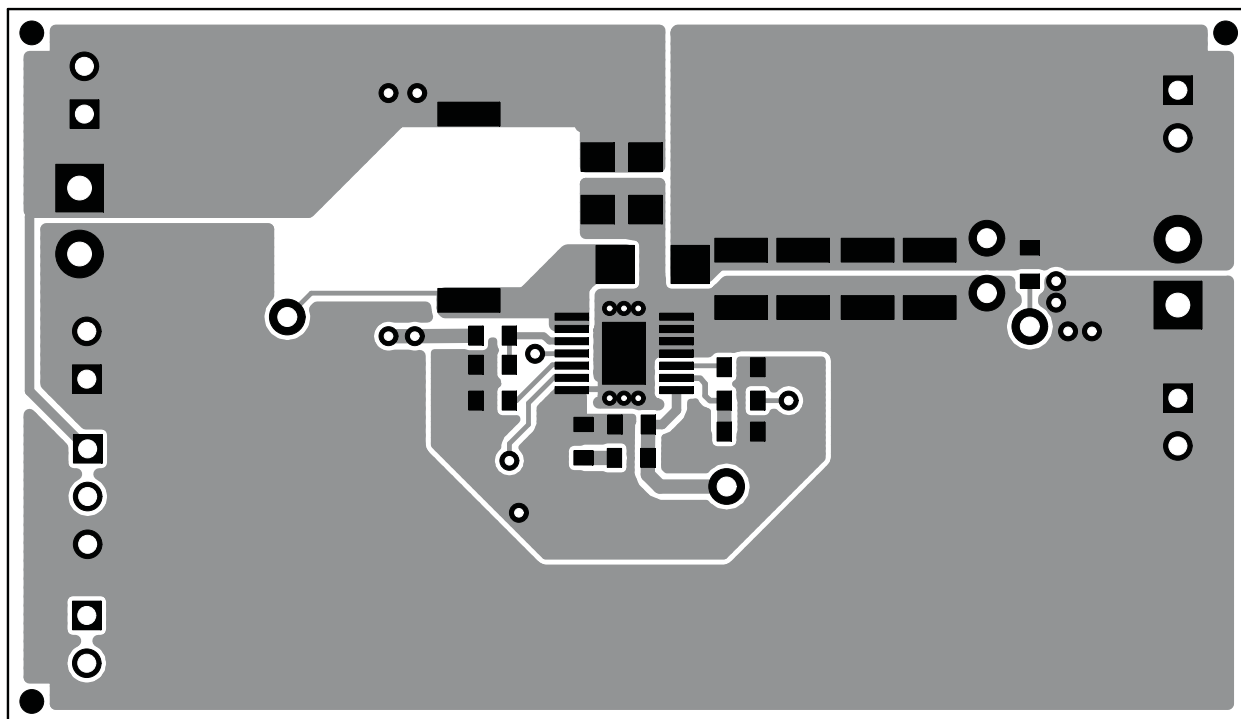


Figure 10. Top Layer Routing

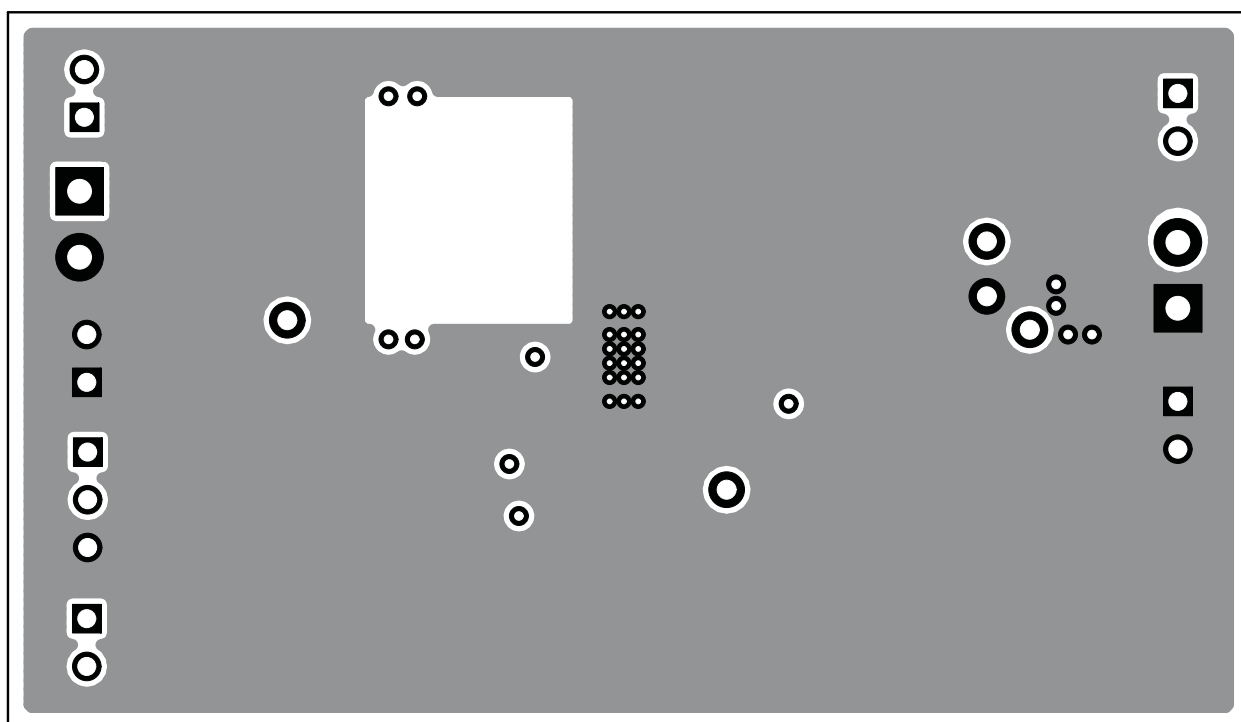


Figure 11. Internal Layer 1

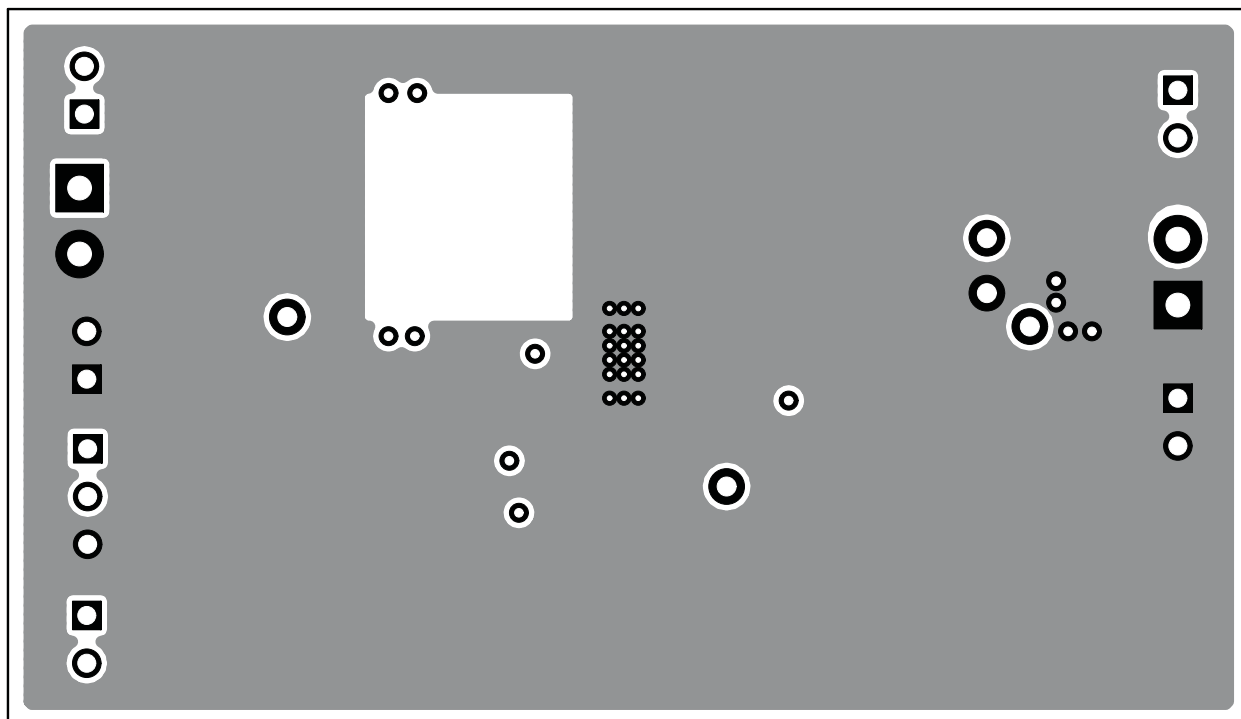


Figure 12. Internal Layer 2

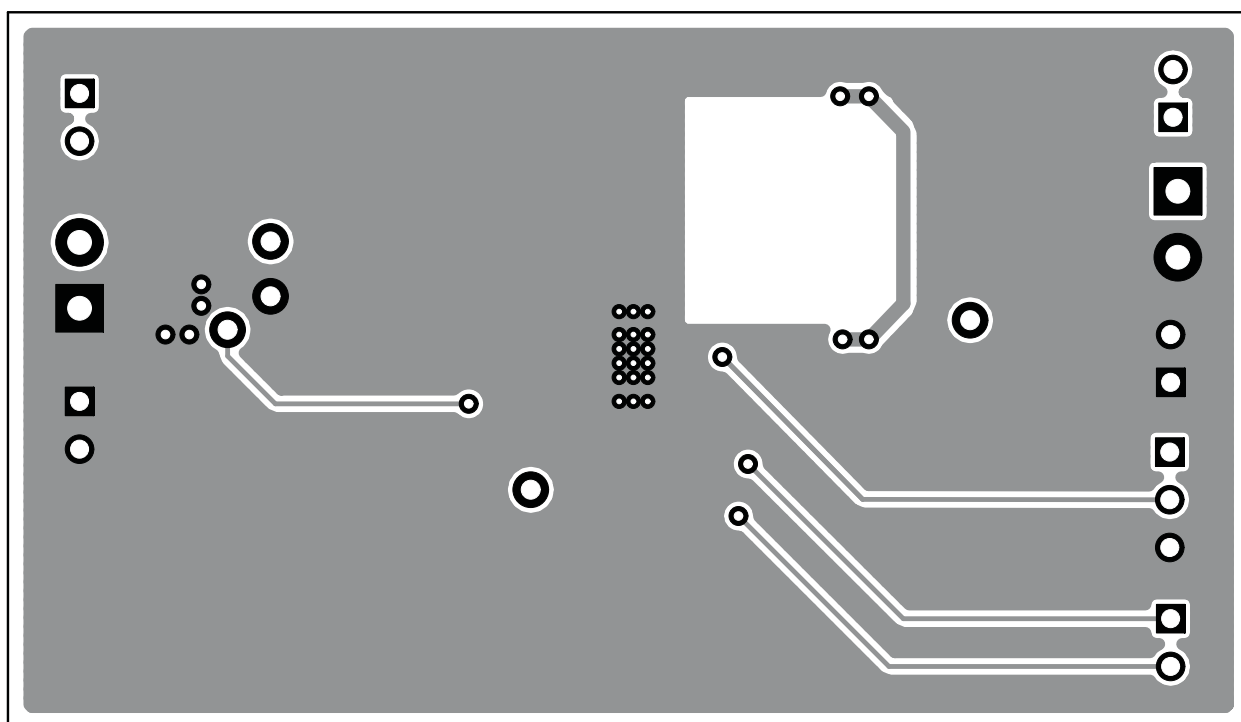


Figure 13. Bottom-Side Layer

4 Bill of Materials and Schematic

This section provides the TPS61175EVM-326 bill of materials and schematic.

4.1 Bill of Materials

Table 3. HPA326 Bill of Materials

RefDes	Value	Description	Size	Part Number	MFR
C1	10 μ F	Capacitor, Ceramic, 25V, X5R, 20%	1206	STD	STD
C10	Open	Capacitor, Ceramic, 50V, X7R, 10%	1210	STD	STD
C2	Open	Capacitor, Ceramic, 25V, X5R, 20%	1206	STD	STD
C3	0.047 μ F	Capacitor, Ceramic, 10V, X5R, 10%	0603	STD	STD
C4	33 nF	Capacitor, Ceramic, 10V, X5R, 10%	0603	STD	STD
C5	Open	Capacitor, Ceramic, 10V, X5R, 10%	0603	STD	STD
C7	0.1 μ F	Capacitor, Ceramic, 25V, X5R, 20%	0603	STD	STD
C8, C9, C11	4.7 μ F	Capacitor, Ceramic, 50V, X7R, 10%	1210	STD	STD
D1	MBRA340	Diode, Schottky, 3A, 40V	SMA	MBRA340	On Semi
J1– J5	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch $\times$ 2	PTC36SAAN	Sullins
J6, J7	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 $\times$ 0.25 inch	ED555/2DS	OST
JP1	PTC36SAAN	Header, Male 3-pin, 100mil spacing, (36-pin strip)	0.100 inch $\times$ 3	PTC36SAAN	Sullins
L1	22 μ H	Inductor, SMT, 2.9A, 47milliohm	0.402 sq inch	CDRH105RNP-220N	Sumida
R1	301k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R2	16.2k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3	3.09k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	143k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R5	50	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R6	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
TP1–TP4	5000	Test Point, Red, Thru Hole Color Keyed	0.100 $\times$ 0.100 inch	5000	Keystone
TP5	5001	Test Point, Black, Thru Hole Color Keyed	0.100 $\times$ 0.100 inch	5001	Keystone
U1	TPS61175PWP	IC, High Voltage/Current Boost Converter	HTSSOP-14	TPS61175PWP	TI
—		Shunt, 100-mil, Black	0.100	929950-00	3M
		PCB, 1.5" $\times$ 2.6" $\times$ 0.062"		HPA326	Any

4.2 Schematic

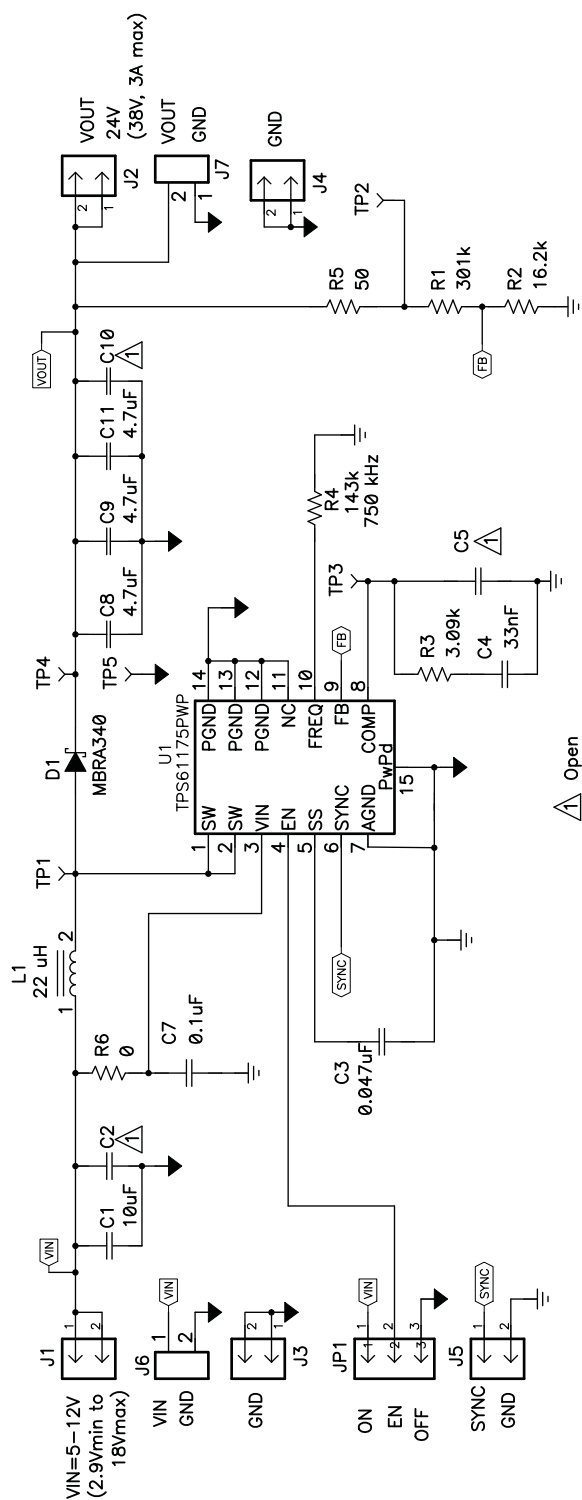


Figure 14. TPS61175EVM-326 Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 18 V and the output voltage range of 38V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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