Product data sheet

1. General description

The HEF4011B is a quad 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of $V_{\rm CC}$.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- · High noise immunity
- · Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- · Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

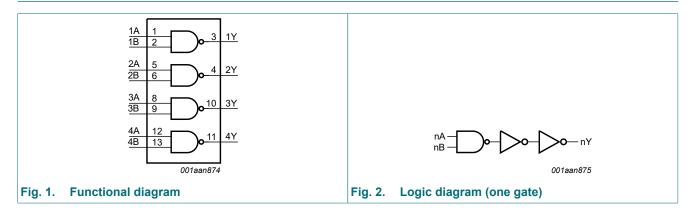
Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
HEF4011BT	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			



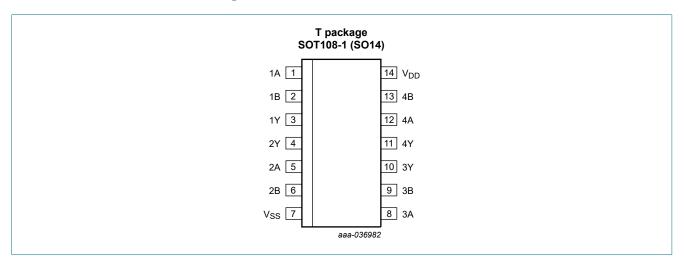
Quad 2-input NAND gate

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 5, 8, 12	input
1B, 2B, 3B, 4B	2, 6, 9, 13	input
1Y, 2Y, 3Y, 4Y	3, 4, 10, 11	output
V _{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

Quad 2-input NAND gate

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Input	Output	
nA	nB	nY
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0 \text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
VI	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to} + 125 ^{\circ}\text{C}$ [1]	-	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Table of Recommended operating conditions								
Parameter	Conditions	Min	Тур	Max	Unit			
supply voltage		3	-	15	V			
input voltage		0	-	V_{DD}	V			
ambient temperature	in free air	-40	-	+125	°C			
input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	µs/V			
	V _{DD} = 10 V	-	-	0.5	μs/V			
	V _{DD} = 15 V	-	-	0.08	μs/V			
	supply voltage input voltage ambient temperature	supply voltage input voltage ambient temperature in free air input transition rise and fall rate $V_{DD} = 5 \text{ V}$ $V_{DD} = 10 \text{ V}$	supply voltage 3 input voltage 0 ambient temperature in free air -40 input transition rise and fall rate $V_{DD} = 5 \text{ V}$ - $V_{DD} = 10 \text{ V}$ -	supply voltage3-input voltage0-ambient temperaturein free air-40-input transition rise and fall rate $V_{DD} = 5 V$ $V_{DD} = 10 V$	supply voltage3-15input voltage0- V_{DD} ambient temperaturein free air-40-+125input transition rise and fall rate $V_{DD} = 5 \text{ V}$ 3.75 $V_{DD} = 10 \text{ V}$ 0.5			

Quad 2-input NAND gate

9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0 \ V$; $V_{I} = V_{SS} \ or \ V_{DD}$; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		T _{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
	voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
	voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level	I _O < 1 µA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
	output current	V _O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I _{OL}	LOW-level	V _O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
	output current	V _O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V _O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{DD}	supply current	all valid input	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
		combinations;	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
		I _O = 0 A	15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
Cı	input capacitance			-	-	-	7.5	-	-	-	-	pF

Quad 2-input NAND gate

10. Dynamic characteristics

Table 7. Dynamic characteristics

 T_{amb} = 25 °C unless otherwise specified; for waveforms see Fig. 3; for test circuit see Fig. 4.

Symbol	Parameter	Extrapolation formula [1]	V_{DD}	Min	Тур	Max	Unit
t _{pd}	propagation delay [2]	28 + 0.55 × C _L	5 V	-	55	110	ns
		14 + 0.23 × C _L	10 V	-	25	45	ns
		12 + 0.16 × C _L	15 V	-	20	35	ns
=	HIGH to LOW output	10 + 1.00 × C _L	5 V	-	60	120	ns
		9 + 0.42 × C _L	10 V	-	30	60	ns
		6 + 0.28 × C _L	15 V	-	20	40	ns
t _{TLH}	LOW to HIGH output	10 + 1.00 × C _L	5 V	-	60	120	ns
	transition time	9 + 0.42 × C _L	10 V	-	30	60	ns
		6 + 0.28 × C _L	15 V	-	20	40	ns

^[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 8. Dynamic power dissipation

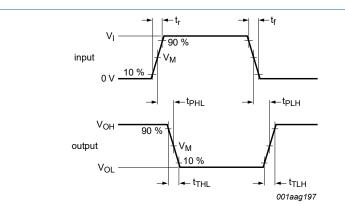
 $V_{SS} = 0 \ V; \ t_r = t_f \le 20 \ ns; \ T_{amb} = 25 \ ^{\circ}C.$

Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic	5 V	. (5 2) 22 (1)	f _i = input frequency in MHz;
	power dissipation	10 V	FD = 0000	f _o = output frequency in MHz; C _L = output load capacitance in pF;
	alcolpation	15 V	D 00400 (E/(0))/ // \AN	$\Sigma(f_o \times C_L)$ = sum of the outputs;
				V _{DD} = supply voltage in V.

^[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

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10.1. Waveforms and test circuit



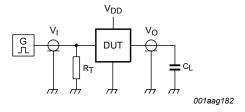
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. Propagation delay, output transition time

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V _M	V _M
5 V to 15 V	$0.5 \times V_{DD}$	0.5 × V _{DD}



Test data is given in Table 10.

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance;

 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 4. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load	
V_{DD}	V _I	t _r , t _f	C _L
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

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11. Package outline

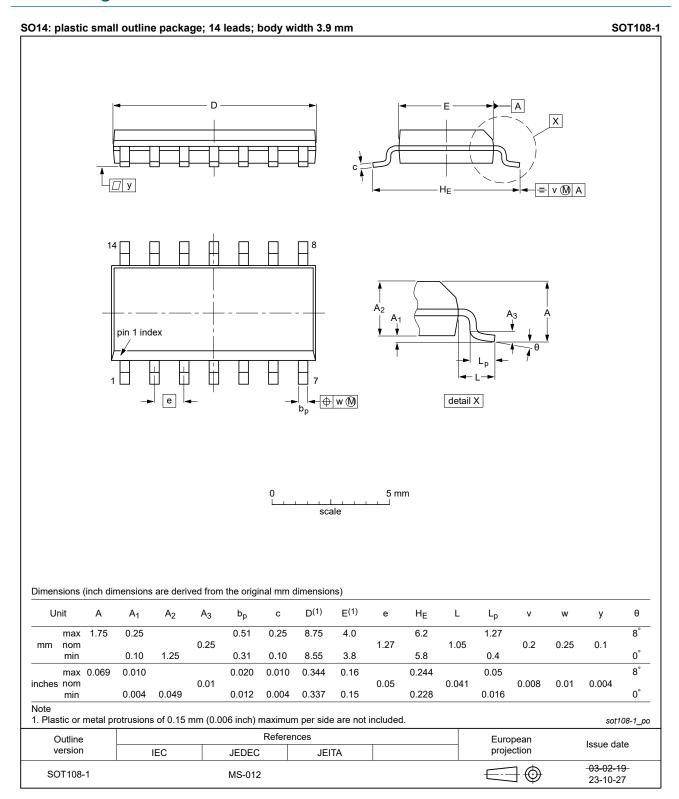


Fig. 5. Package outline SOT108-1 (SO14)

Quad 2-input NAND gate

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
НВМ	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
HEF4011B v.7	20240723	Product data sheet	-	HEF4011B v.6			
Modifications:	Nexperia. Legal texts have Section 2: ESI Table 4: Derati	this data sheet has been redest we been adapted to the new co D specification updated accord ng values for P _{tot} total power of SO package outline drawing to	ompany name where ing to the latest JED lissipation updated.	appropriate.			
HEF4011B v.6	20151210	Product data sheet	-	HEF4011B v.5			
Modifications:	Type number I	HEF4011BP (SOT27-1) remove	ed.				
HEF4011B v.5	20111121	Product data sheet	-	HEF4011B v.4			
Modifications:	 Legal pages updated. Changes in "General description" and "Features and benefits". Section "Applications" removed. 						
HEF4011B v.4	20110330	Product data sheet	-	HEF4011B_CNV v.3			
HEF4011B_CNV v.3	19950101	Product specification	-	HEF4011B_CNV v.2			
HEF4011B_CNV v.2	19950101	Product specification	-	-			

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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