

MICRON
TECHNOLOGY, INC.
MT4C4001J
1 MEG x 4 DRAM

DRAM

1 MEG x 4 DRAM

FAST PAGE MODE

T-46-23-18

DRAM

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V $\pm 10\%$ power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{\text{RAS}}$ -ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle

OPTIONS

- Timing
- 60ns access
- 70ns access
- 80ns access

MARKING

- Packages
- Plastic SOJ (300 mil) **DJ**
- Plastic TSOP (300 mil)* **TG**
- Plastic ZIP (350 mil) **Z**

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

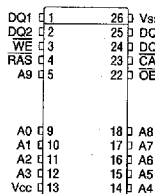
- Operating Temperature, T_A
- Commercial (0°C to +70°C) **None**
- Industrial (-40°C to +85°C) **IT**
- Part Number Example: MT4C4001JDJ-6

GENERAL DESCRIPTION

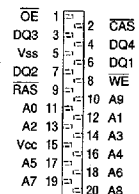
The MT4C4001J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin(s), the Qs are activated and retain the selected cell data as long as $\overline{\text{CAS}}$ remains low

PIN ASSIGNMENT (Top View)

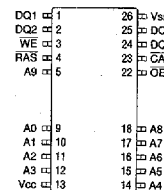
20-Pin SOJ (N-2)



20-Pin ZIP (O-1)



20-Pin TSOP (R-1)



*Consult factory on availability of reverse pinout TSOP packages

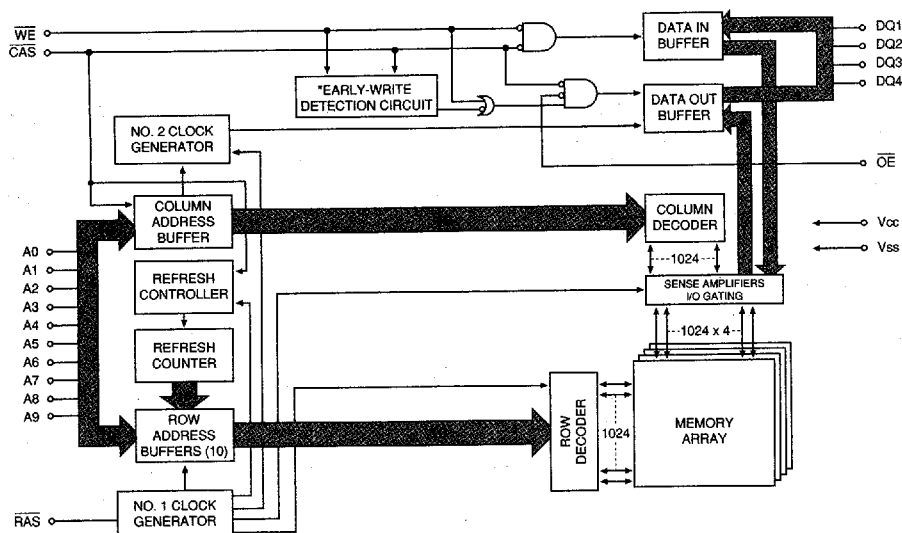
(regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$ followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ -ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR) or HIDDEN refresh) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{\text{RAS}}$ addressing.

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FUNCTIONAL BLOCK DIAGRAM **FAST PAGE MODE**



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
 $\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA IN/OUT
						R	C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z


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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} -1V to +7V
 Operating Temperature, T_A (Ambient) 0°C to +70°C
 Storage Temperature (Plastic) -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ 6.5V (All other pins not under test = 0V)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) (R _{AS} = C _{AS} = V _{IH})	I _{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) (R _{AS} = C _{AS} = Other Inputs = V _{CC} - 0.2V)	I _{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (R _{AS} = V _{IL} , C _{AS} , Address Cycling: t _{PC} = t _{PC} (MIN))	I _{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: R _{AS} -ONLY Average power supply current (R _{AS} Cycling, C _{AS} = V _{IH} : t _{RC} = t _{RC} (MIN))	I _{CC5}	110	100	90	mA	3
REFRESH CURRENT: C _{AS} -BEFORE-R _{AS} Average power supply current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC6}	110	100	90	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C _{i1}		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C _{i2}		7	pF	2
Input/Output Capacitance: DQ	C _{io}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{cc} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	'RC	110		130		150		ns	
READ-WRITE cycle time	'RWC	145		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	'PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	'PRWC	90		95		100		ns	
Access time from RAS	'RAC		60		70		80	ns	14
Access time from CAS	'CAC		15		20		20	ns	15
Output Enable	'OE		15		20		20	ns	23
Access time from column address	'AA		30		35		40	ns	
Access time from CAS precharge	'CPA		35		40		45	ns	
RAS pulse width	'RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	'RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	'RSH	15		20		20		ns	
RAS precharge time	'RP	40		50		60		ns	
CAS pulse width	'CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	'CSH	60		70		80		ns	
CAS precharge time	'CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	'CP	10		10		10		ns	
RAS to CAS delay time	'RCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	'CRP	10		10		10		ns	
Row address setup time	'ASR	0		0		0		ns	
Row address hold time	'RAH	10		10		10		ns	
RAS to column address delay time	'RAD	15	30	15	35	15	40	ns	18
Column address setup time	'ASC	0		0		0		ns	
Column address hold time	'CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	'AR	50		55		60		ns	
Column address to RAS lead time	'RAL	30		35		40		ns	
Read command setup time	'RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	'RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	'RRH	0		0		0		ns	19
CAS to output in Low-Z	'CLZ	0		0		0		ns	
Output buffer turn-off delay	'OFF	0	15	0	20	0	20	ns	20

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		-8		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
WE command setup time	t_{WCS}	0		0		0		ns	21, 27
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time (referenced to RAS)	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to RAS lead time	t_{RWL}	15		20		20		ns	
Write command to CAS lead time	t_{CWL}	15		20		20		ns	
Data-in setup time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	10		15		15		ns	22
Data-in hold time (referenced to RAS)	t_{DHR}	45		55		60		ns	
RAS to WE delay time	t_{RWD}	85		100		110		ns	21
Column address to WE delay time	t_{AWD}	60		65		70		ns	21
CAS to WE delay time	t_{CWD}	45		50		50		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	t_{REF}		16		16		16	ms	
RAS to CAS precharge time	t_{RPC}	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	t_{CSR}	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	t_{CHR}	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	t_{WRH}	10		10		10		ns	25, 28
WE setup time (CAS-BEFORE-RAS refresh)	t_{WRP}	10		10		10		ns	25, 28
WE hold time (WCBR test cycle)	t_{WTH}	10		10		10		ns	25, 28
WE setup time (WCBR test cycle)	t_{WTS}	10		10		10		ns	25, 28
OE setup prior to RAS during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		ns	
Output disable	t_{OD}		15		20		20	ns	27
OE hold time from WE during READ-MODIFY-WRITE cycle	t_{OEH}	15		20		20		ns	26

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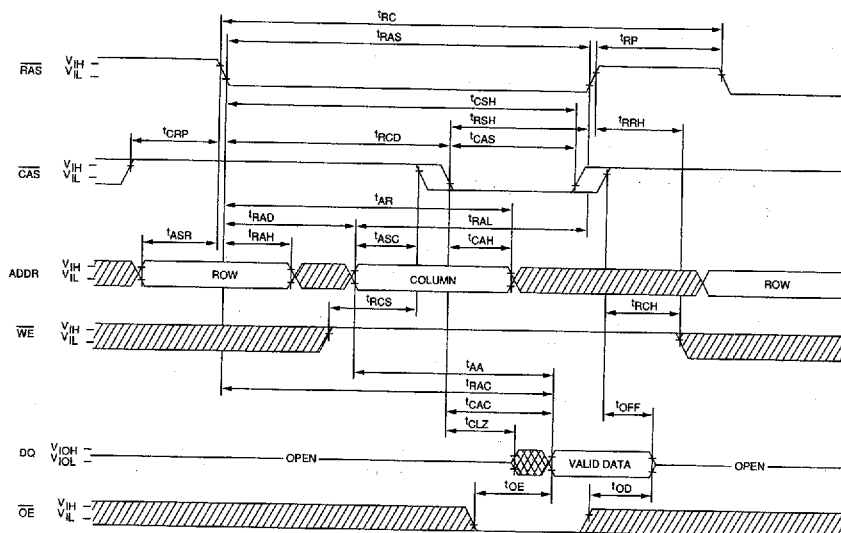
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, $f = 1 \text{ MHz}$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100 μ s is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ -ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-up should be repeated any time the $\overline{\text{REF}}$ refresh requirement is exceeded.
8. AC characteristics assume $T = 5\text{ns}$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}} = V_{IH}$, data output is High-Z.
12. If $\overline{\text{CAS}} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $\overline{\text{RCD}} < \overline{\text{RCD}} (\text{MAX})$. If $\overline{\text{RCD}}$ is greater than the maximum recommended value shown in this table, $\overline{\text{RAC}}$ will increase by the amount that $\overline{\text{RCD}}$ exceeds the value shown.
15. Assumes that $\overline{\text{RCD}} \geq \overline{\text{RCD}} (\text{MAX})$.
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for $\overline{\text{CPN}}$.
17. Operation within the $\overline{\text{RCD}} (\text{MAX})$ limit ensures that $\overline{\text{RAC}} (\text{MAX})$ can be met. $\overline{\text{RCD}} (\text{MAX})$ is specified as a reference point only; if $\overline{\text{RCD}}$ is greater than the specified $\overline{\text{RCD}} (\text{MAX})$ limit, then access time is controlled exclusively by $\overline{\text{CAC}}$.
18. Operation within the $\overline{\text{RAD}} (\text{MAX})$ limit ensures that $\overline{\text{RAC}} (\text{MIN})$ and $\overline{\text{CAC}} (\text{MIN})$ can be met. $\overline{\text{RAD}} (\text{MAX})$ is specified as a reference point only; if $\overline{\text{RAD}}$ is greater than the specified $\overline{\text{RAD}} (\text{MAX})$ limit, then access time is controlled exclusively by $\overline{\text{AA}}$.
19. Either $\overline{\text{RCH}}$ or $\overline{\text{RRH}}$ must be satisfied for a READ cycle.
20. $\overline{\text{OFF}} (\text{MAX})$ defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL} .
21. $\overline{\text{WCS}}$, $\overline{\text{RWD}}$, $\overline{\text{AWD}}$ and $\overline{\text{CWD}}$ are not restrictive operating parameters. $\overline{\text{WCS}}$ applies to EARLY-WRITE cycles. $\overline{\text{RWD}}$, $\overline{\text{AWD}}$ and $\overline{\text{CWD}}$ apply to READ-MODIFY-WRITE cycles. If $\overline{\text{WCS}} \geq \overline{\text{WCS}} (\text{MIN})$, the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $\overline{\text{RWD}} \geq \overline{\text{RWD}} (\text{MIN})$, $\overline{\text{AWD}} \geq \overline{\text{AWD}} (\text{MIN})$ and $\overline{\text{CWD}} \geq \overline{\text{CWD}} (\text{MIN})$, the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE-WRITE ($\overline{\text{OE}}$ controlled) cycle. $\overline{\text{WCS}}$, $\overline{\text{RWD}}$, $\overline{\text{CWD}}$ and $\overline{\text{AWD}}$ are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}} = \text{LOW}$ and $\overline{\text{OE}} = \text{HIGH}$.
25. $\overline{\text{WTS}}$ and $\overline{\text{WTH}}$ are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of $\overline{\text{WRP}}$ and $\overline{\text{WRH}}$ in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both $\overline{\text{OD}}$ and $\overline{\text{OE}}$ met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back LOW after $\overline{\text{OE}}$ is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once $\overline{\text{OD}}$ or $\overline{\text{OFF}}$ occur. If $\overline{\text{CAS}}$ goes HIGH first, $\overline{\text{OE}}$ becomes a "don't care." If $\overline{\text{OE}}$ goes HIGH and $\overline{\text{CAS}}$ stays LOW, $\overline{\text{OE}}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{\text{OE}}$ is taken back LOW (while $\overline{\text{CAS}}$ remains LOW).
28. JEDEC test version only.

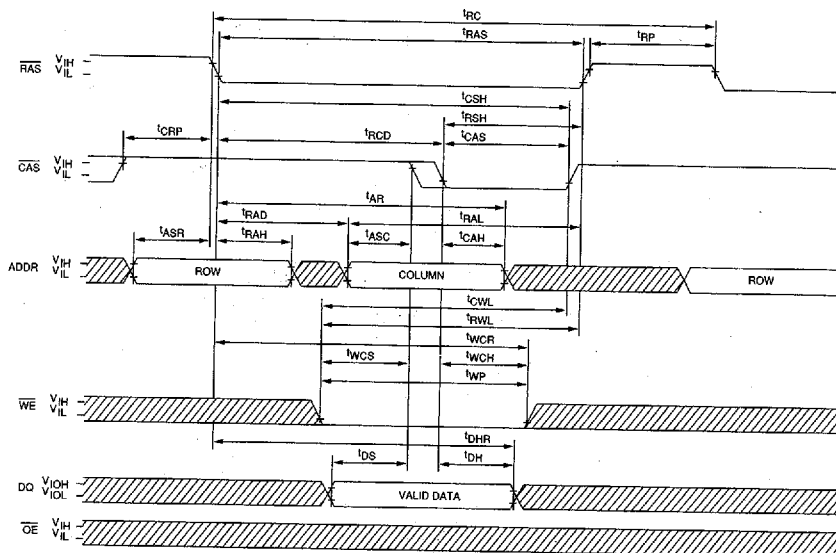
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READ CYCLE

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EARLY-WRITE CYCLE



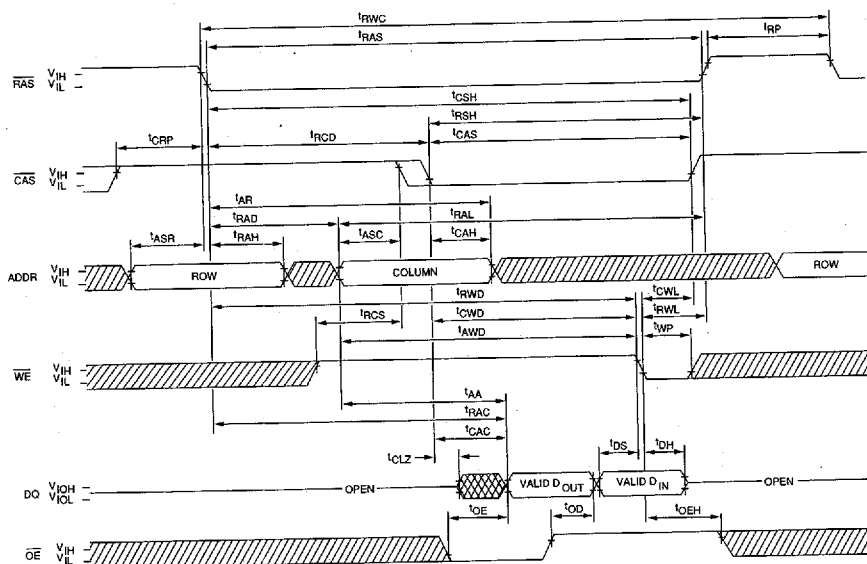
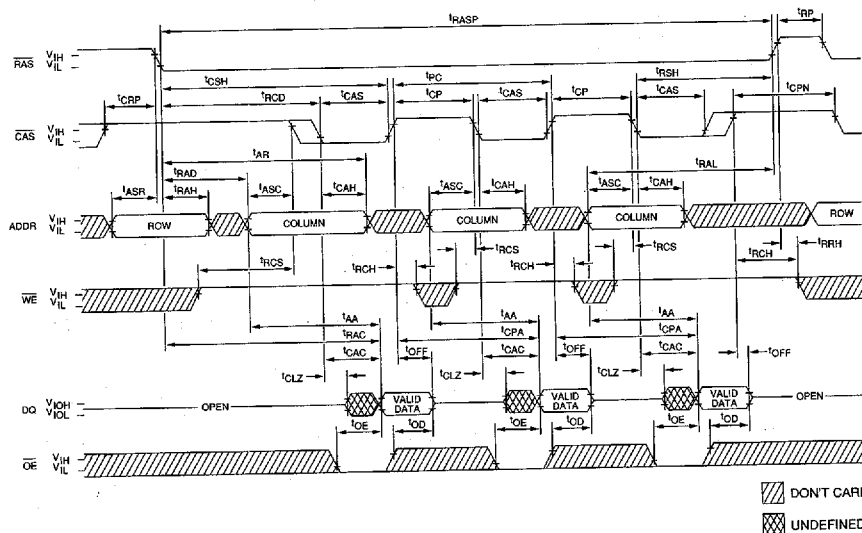
DON'T CARE

UNDEFINED

DRAM

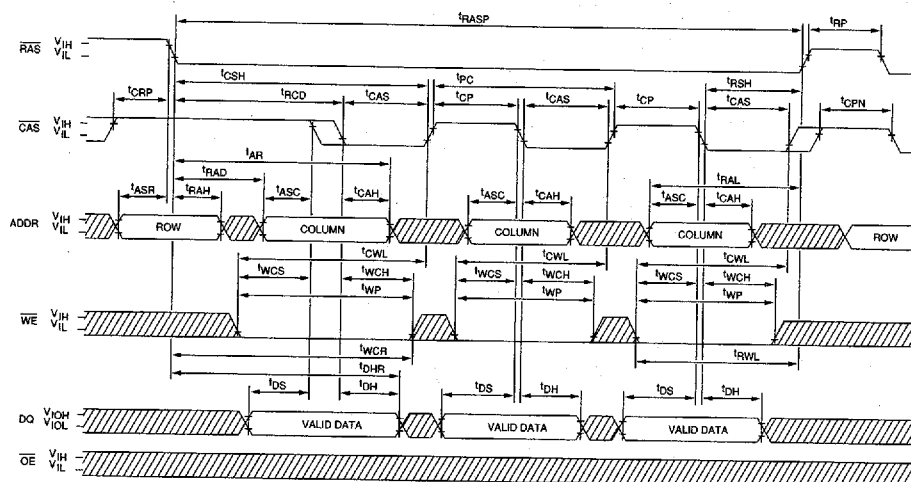
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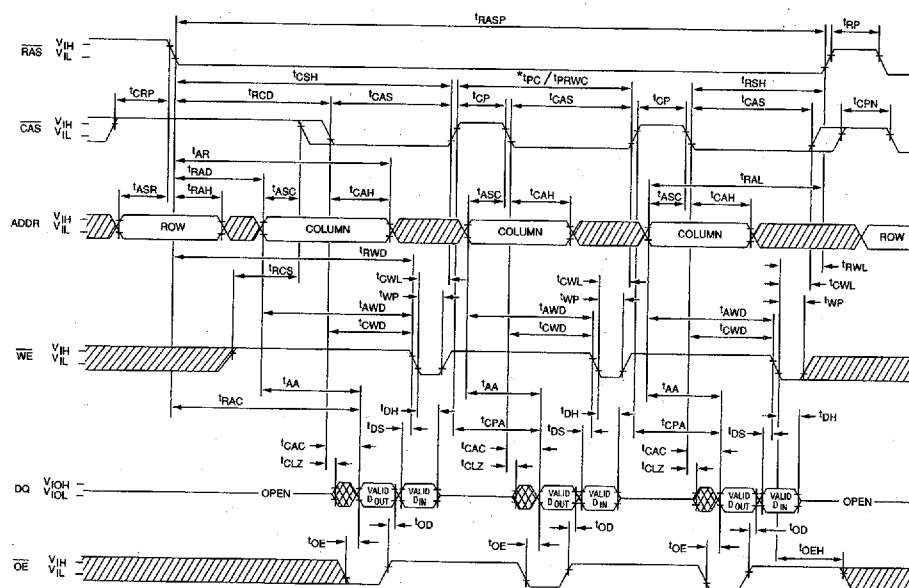
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)**FAST-PAGE-MODE READ CYCLE**

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FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE-WRITE only.

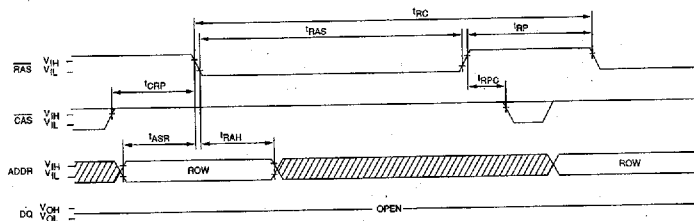
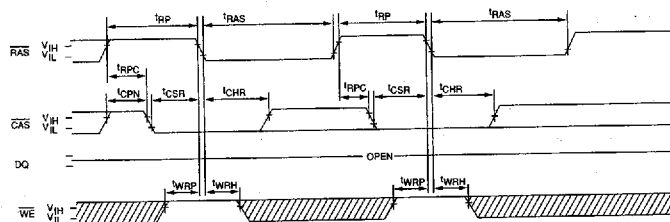
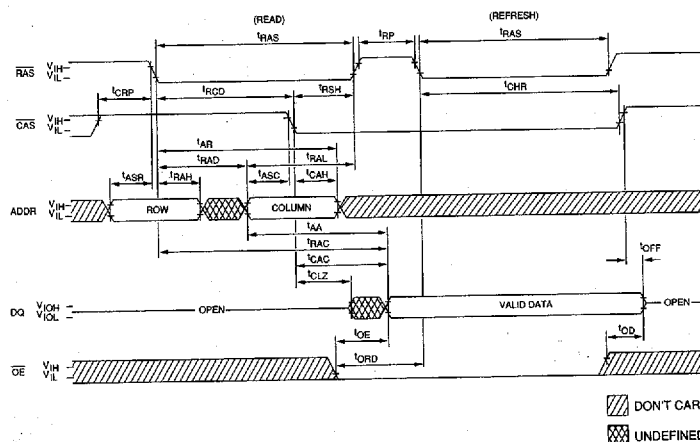
 DON'T CARE

 UNDEFINED

DRAW

MICRON
TECHNOLOGY INC**MT4C4001J**
1 MEG x 4 DRAM**RAS-ONLY REFRESH CYCLE**
(ADDR = A0-A9; WE = DON'T CARE)

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**CAS-BEFORE-RAS REFRESH CYCLE**
(A0-A9, and OE = DON'T CARE)**HIDDEN REFRESH CYCLE²⁴**
(WE = HIGH; OE = LOW)


MT4C4001J
1 MEG x 4 DRAM

4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

A CBR cycle with $\overline{\text{WE}}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

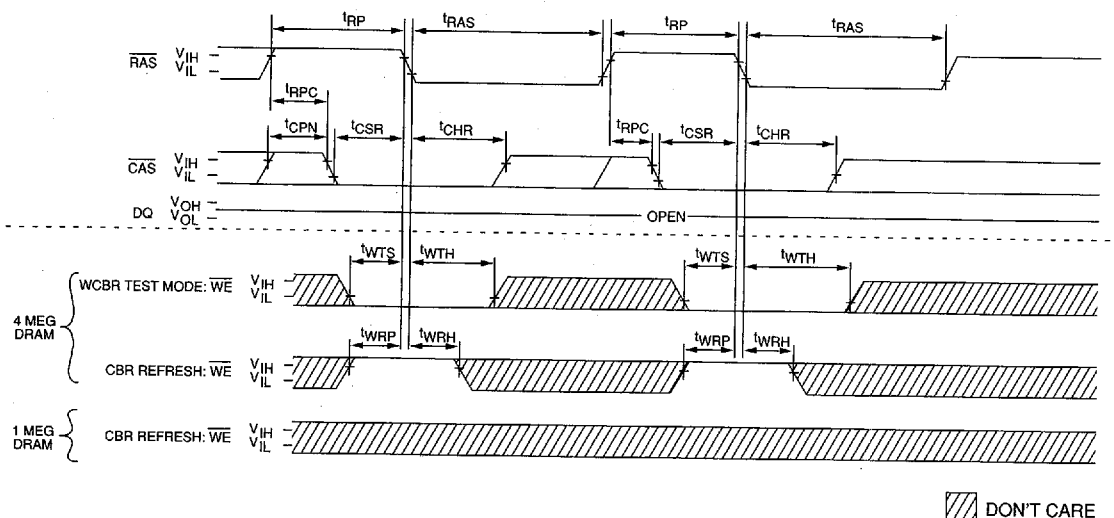
POWER-UP

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The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100 μ s delay followed by any eight $\overline{\text{RAS}}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight RAS-ONLY or CBR REFRESH ($\overline{\text{WE}}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{\text{RAS}}$ -ONLY or a CBR REFRESH cycle ($\overline{\text{WE}}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{\text{WE}}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{\text{WE}}$ to be HIGH.
2. The eight $\overline{\text{RAS}}$ wake-up cycles on the 1 Meg may be any valid $\overline{\text{RAS}}$ cycle while the 4 Meg may only use RAS-ONLY or CBR REFRESH cycles ($\overline{\text{WE}}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR